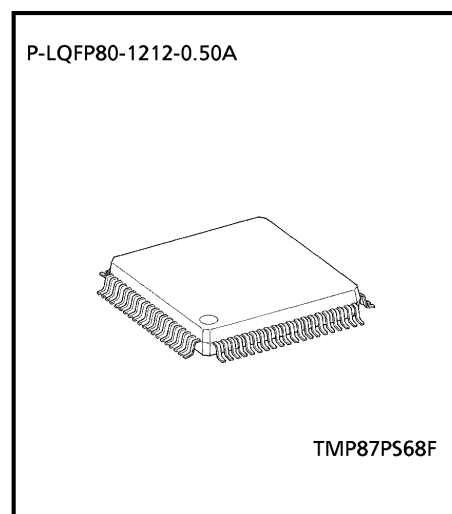CMOS 8-Bit Microcontroller

TMP87PS68DF

The 87PS68 is a One-Time PROM microcontroller with low-power 480 K bits electrically programmable read only memory for the 87CS68 system evaluation. The 87PS68 is pin compatible with the 87CS68. The operations possible with the 87CS68 can be performed by writing programs to PROM. The 87PS68 can write and verify in the same way as the TC571000D using an adaptor socket BM11105 and an EPROM programmer.

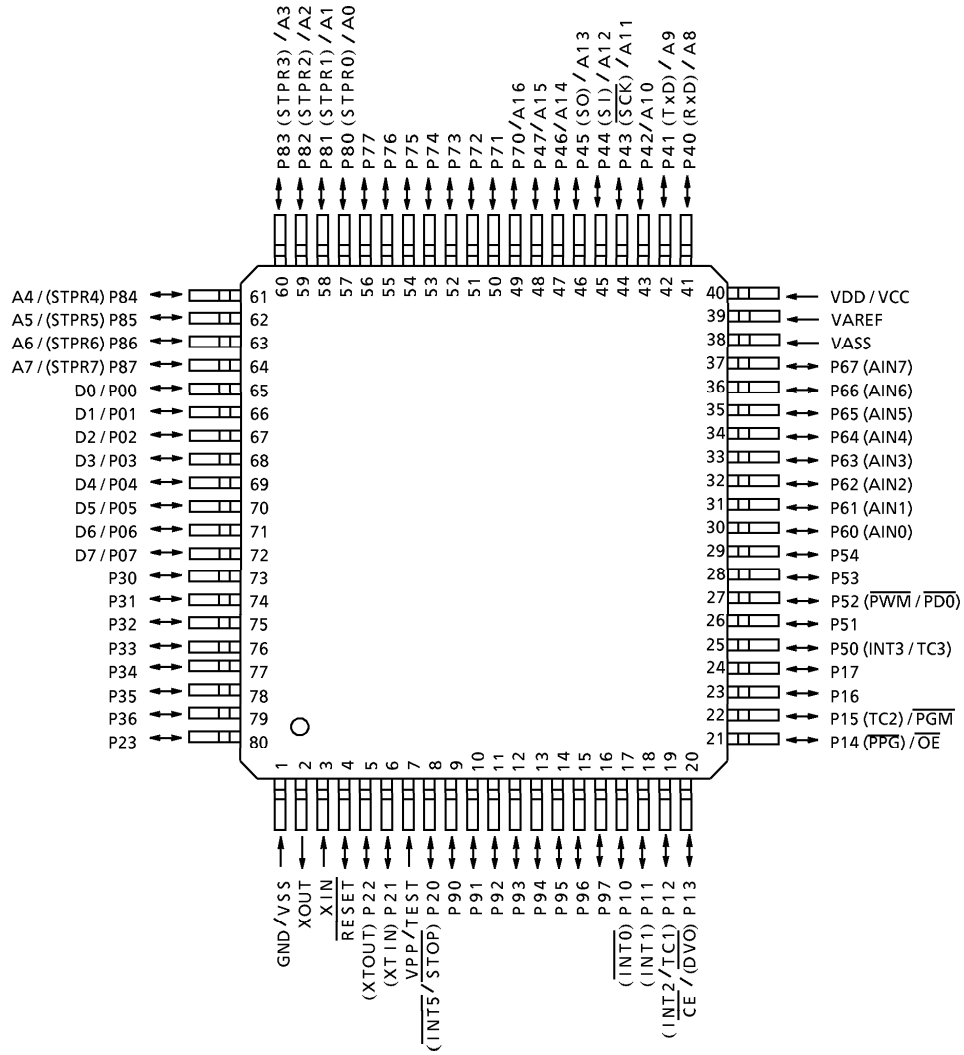| Part No.	OTP	RAM	Package	OTP Adapter
TMP87PS68F	61184 bytes (60 Kbyte-256 byte)	2 K × 8-bit	P-LQFP80-1212-0.50A	BM11105

P-LQFP80-1212-0.50A

TMP87PS68F

980910EBP1

● For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
● The products described in this document are subject to the foreign exchange and foreign trade laws.
● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
● The information contained herein is subject to change without notice.

Pin Assignments (Top View)

P-LQFP80-1212-0.50A

Top-side pins (left to right, 60–41):
P83 (STPR3) / A3
P82 (STPR2) / A2
P81 (STPR1) / A1
P80 (STPR0) / A0
P77
P76
P75
P74
P73
P72
P71
P70 / A16
P47 / A15
P46 / A14
P45 (SO) / A13
P44 (SI) / A12
P43 (SCK) / A11
P42 / A10
P41 (TxD) / A9
P40 (RxD) / A8

Left-side pins (61–80):
A4 / (STPR4) P84 — 61
A5 / (STPR5) P85 — 62
A6 / (STPR6) P86 — 63
A7 / (STPR7) P87 — 64
D0 / P00 — 65
D1 / P01 — 66
D2 / P02 — 67
D3 / P03 — 68
D4 / P04 — 69
D5 / P05 — 70
D6 / P06 — 71
D7 / P07 — 72
P30 — 73
P31 — 74
P32 — 75
P33 — 76
P34 — 77
P35 — 78
P36 — 79
P23 — 80

Right-side pins (40–21):
40 — VDD / VCC
39 — VAREF
38 — VASS
37 — P67 (AIN7)
36 — P66 (AIN6)
35 — P65 (AIN5)
34 — P64 (AIN4)
33 — P63 (AIN3)
32 — P62 (AIN2)
31 — P61 (AIN1)
30 — P60 (AIN0)
29 — P54
28 — P53
27 — P52 ($\overline{\text{PWM}}$ / $\overline{\text{PD0}}$)
26 — P51
25 — P50 (INT3 / TC3)
24 — P17
23 — P16
22 — P15 (TC2) / $\overline{\text{PGM}}$
21 — P14 ($\overline{\text{PPG}}$) / $\overline{\text{OE}}$

Bottom-side pins (left to right, 1–20):
GND / VSS
XOUT
XIN
RESET
(XTOUT) P22
(XT IN) P21
VPP / TEST
($\overline{\text{INT5}}$ / $\overline{\text{STOP}}$) P20
P90
P91
P92
P93
P94
P95
P96
P97
($\overline{\text{INT0}}$) P10
($\overline{\text{INT1}}$) P11
($\overline{\text{INT2}}$ / $\overline{\text{TC1}}$) P12
CE / ($\overline{\text{DVO}}$) P13

Pin Function

The 87PS68 has two modes: MCU and PROM.

(1) MCU mode
In this mode, the 87PS68 is pin compatible with the 87CS68 (fix the TEST pin at low level.)

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16	Input	PROM address inputs	P70
A15 to A8			P47 to P40
A7 to A0			P87 to P80
D7 to D0	I/O	PROM data input/outputs	P07 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
$\overline{PGM}$		Program mode signal input	P15
VPP	Power supply	+ 12.75 V / 5 V (Program supply voltage)	TEST
VCC		+ 6.25 V / 5 V	VDD
GND		0 V	VSS
P36 to P30	I/O	Pull-up with resistance for input processing.	
P54 to P50			
P67 to P60			
P77 to P72			
P11		PROM mode setting pin. Be fixed at high level.	
P21			
P71			
P17, P16, P12, P10 P22, P20		PROM mode setting pin. Be fixed at low level.	
$\overline{RESET}$			
XIN	Input	Connect an 8MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF	Power supply	0 V (GND)	
VASS			

Operational Description

The following explains the 87PS68 hardware configuration and operation. The configuration and functions of the 87PS68 are the same as 87CS68, except in that a one-time PROM is used instead of an on-chip mask ROM.

The 87PS68 is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1.   Operating Mode

The 87PS68 has two modes: MCU and PROM.

1.1   MCU Mode

The MCU mode is activated by fixing the TEST / VPP pin at low level.

In the MCU mode, operation is the same as with the 87CS68 (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The 87PS68 has a 60K × 8-bit (addresses 1100_H-$FFFF_H$ in the MCU mode, addresses 11100_H-$1FFFF_H$ in the PROM mode) of program memory (OTP).

When the 87PS68 is used as a system evaluation of the 87CS68, the data is written to the program storage area shown in Figure 1-1.
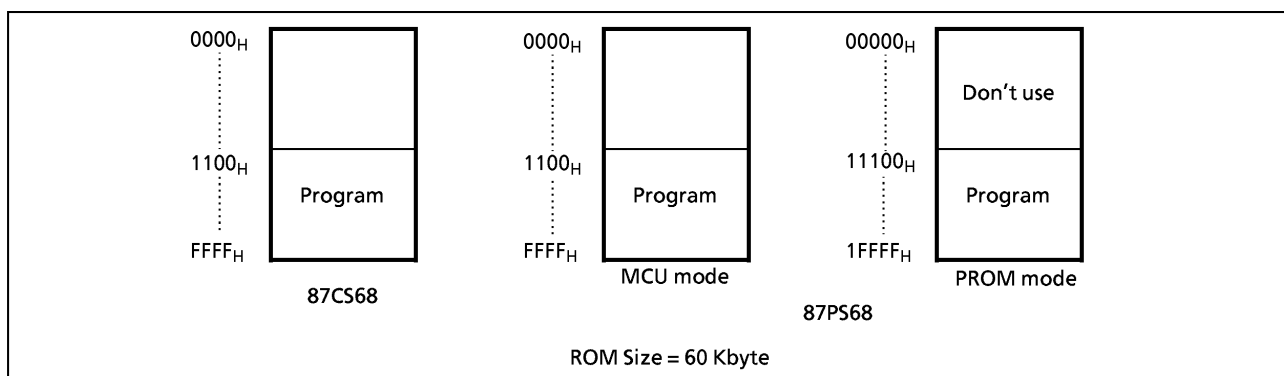

Figure 1.1   Program Memory Area

Note : Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

1.1.2   Data Memory

The 87PS68 has an on-chip 2K × 8-bit data memory (static RAM).

1.1.3   Input/Output Circuitry

(1)   Control pins
The control pins of the 87PS68 are the same as 87CS68 except that the TEST pin has no built-in pull-down resistance.
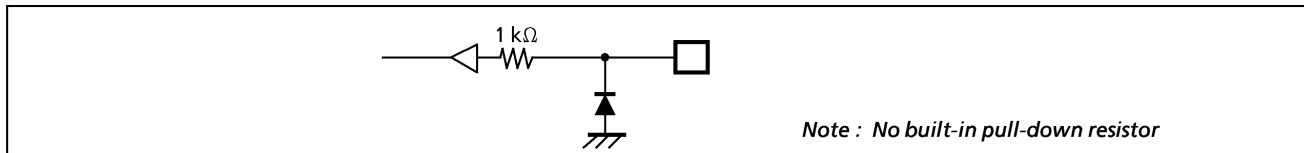

Note : No built-in pull-down resistor

Figure 1-2.   TEST pin

(2)   I/O ports
The I/O circuits of 87PS68 I/O ports the are the same I/O circuitries of the 87CS68.

1.2 PROM Mode

The PROM mode is activated by setting the TEST, $\overline{\text{RESET}}$ pin and the ports P17 to P10, P22 to P20 and P71, as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

> *Note :* *The high-speed programming mode can be used for program operation.*
> *The 87PS68 is not supported an electric signature mode, so the ROM type must be set to TC571000D. (The settings may differ depending on the type of PROM programmer is use. Refer to the PROM programmer operation manual.*
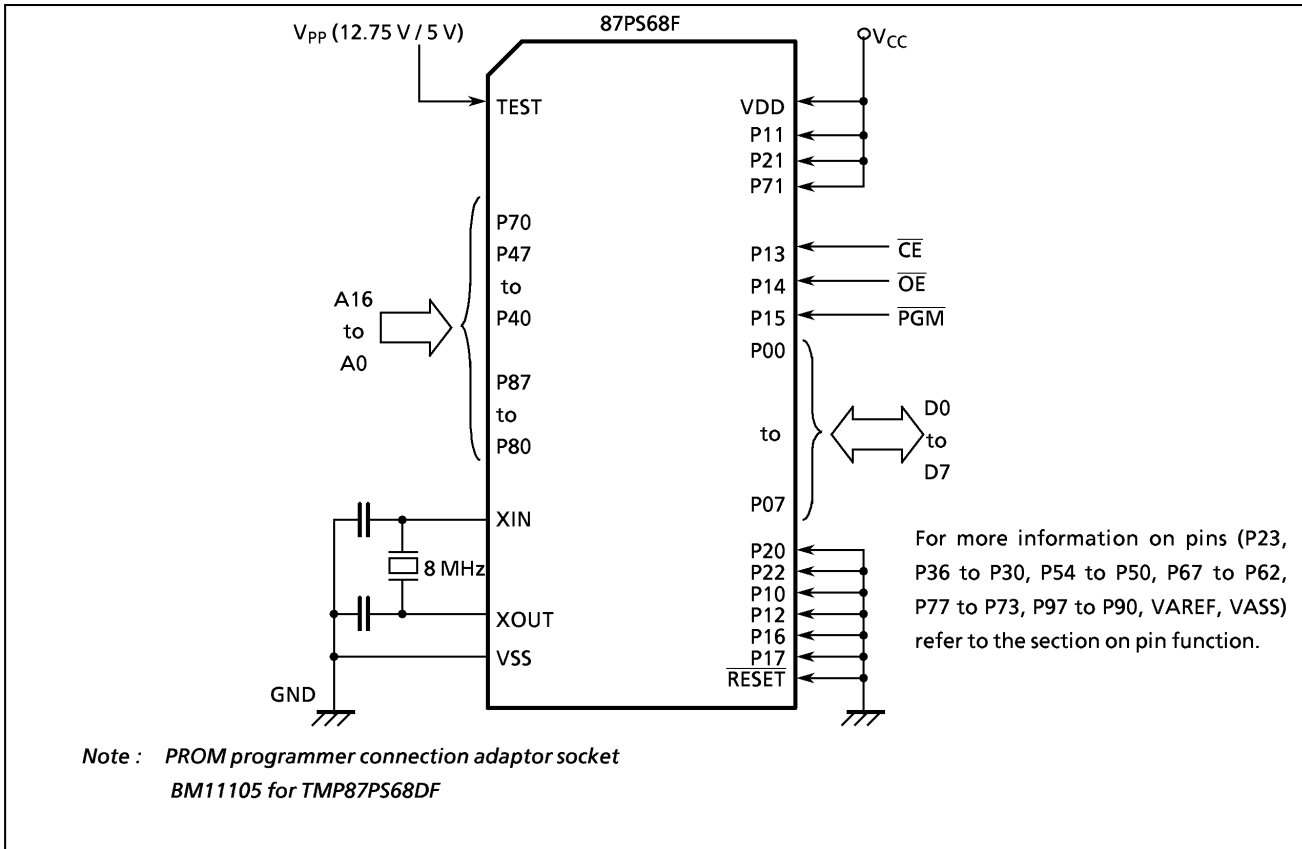

Figure 1-3. Setting for PROM Mode

1.2.1   Programming Flowchart (High-speed Programming Mode)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the VPP pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{PGM}$ input. The programmed data is verified. If incorrect, another 0.1 ms program pulse is applied. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.
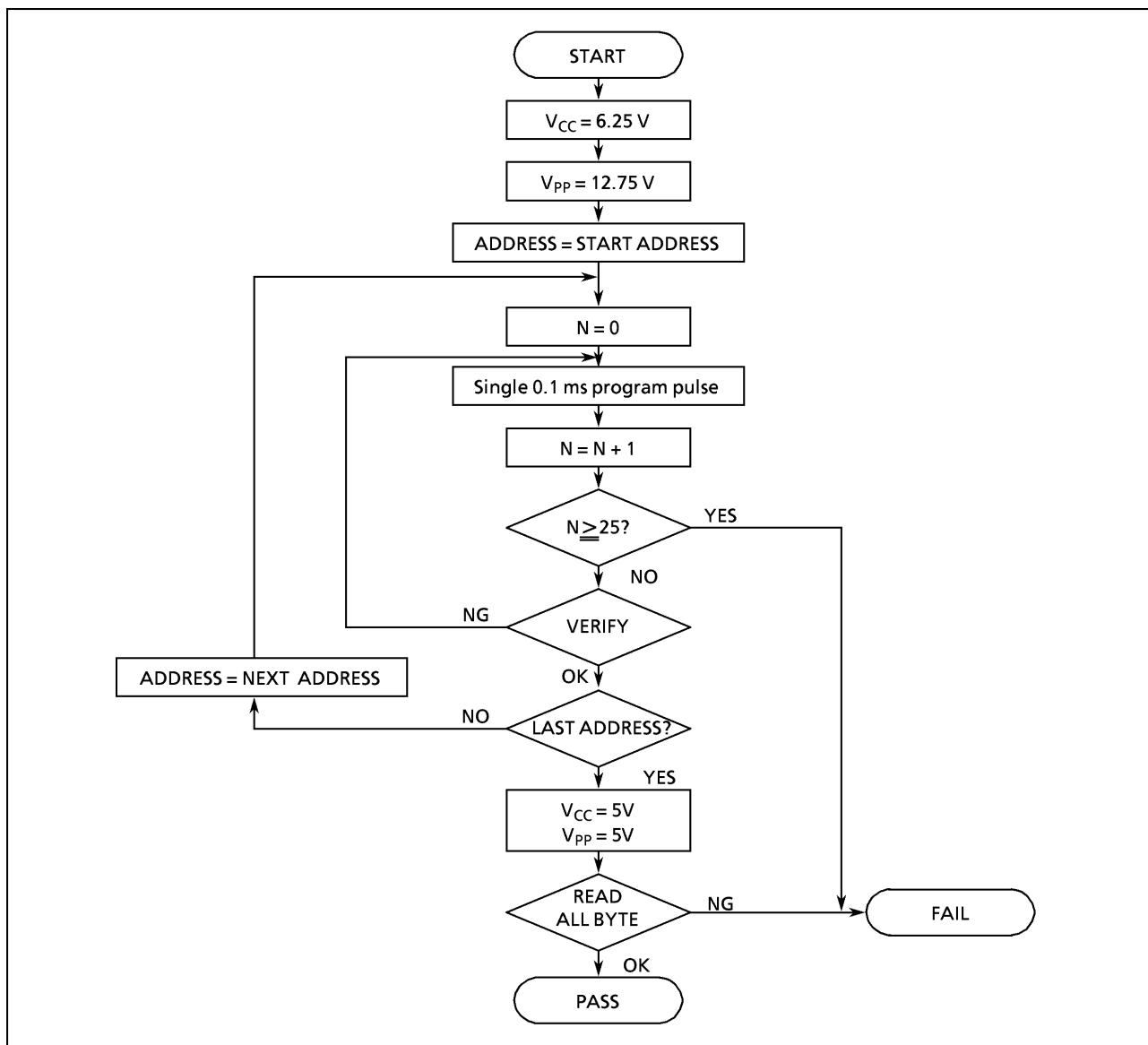

Figure 1-4.   Flow Chart of High-speed Programming

1.2.2   Writing Method for General-purpose PROM Program

(1)   Adapters
     BM11105 : TMP87PS68DF

(2)   Adapter setting
     Switch (SW1) is set to side N.

(3)   PROM programmer specifying
   i)   PROM type is specified to TC571000D.
        Writing voltage：   12.75 V (high-speed program mode)

   ii)   Data transfer (copy) (note 1)
        In the TMP87PS68, EPROM is within the addresses 11100_H to $1FFFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

        Ex. In the block transfer (copy) mode, executed as below.
        ROM capacity of 60KB : transferred addresses 01100_H to $0FFFF_H$ to addresses 11100 to $1FFFF_H$

   iii) Writing address is specified. (note 1)
        Start address : 11100_H
        End address : $1FFFF_H$

(4)   Writing
     Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1 :   The specifying method is referred to the PROM programmer description. Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area. Note 2 :   When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged. Note 3 :   The TMP87PS68 does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12 V ± 0.5 V to the address pin 9 (A9). The signature must not be used.

Input / Output Circuitry

(1) Control pins

The input / output circuitries of the 87PS68 control pins are shown below.

Control Pin	I/O	Input / Output Circuitry and Code	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency) $R_f = 1.2\ M\Omega$ (typ.) $R_O = 1.5\ k\Omega$ (typ.)
XTIN (P21) XTOUT (P22)	Input Output	NM1 Refer to port P2 — NM2	Resonator connecting pins (low-frequency) $R_f = 6\ M\Omega$ (typ.) $R_O = 220\ k\Omega$ (typ.) In only dual-clock mode
$\overline{RESET}$	I/O		Sink open drain output Hysteresis input Pull-up resistor $R_{IN} = 220\ k\Omega$ (typ.) $R = 1\ k\Omega$ (typ.)
$\overline{STOP}/\overline{INT5}$ (P20)	Input		Hysteresis input $R = 1\ k\Omega$ (typ.)
TEST	Input		$R = 1\ k\Omega$ (typ.)

Note1 : *The TEST pin of the 87PS68 does not have a pull-down resistor. Be sure to fix the TEST pin to low in MCU mode.*
Note2 : *The 87PS68 is placed in the single-clock mode during reset. (NM1)*

(2) Input/output ports

The input/output circuitries of the 87PS68 input/output ports are shown below.

Port	I/O	Input/Output Circuitry	Remarks
P0 P6	I/O	initial "Hi-Z" / disable	Tri-state I/O $R = 1k\Omega$ (typ.)
P1	I/O	initial "Hi-Z" / disable	Tri-state I/O Hysteresis input $R = 1k\Omega$ (typ.)
P2	I/O	**P20, P23** — initial "Hi-Z" **P21, P22** — initial "Hi-Z"	Sink open drain output Hysteresis input $R = 1k\Omega$ (typ.)
P3	I/O	initial "Hi-Z"	Sink open drain output High current output $R = 1k\Omega$ (typ.)
P4 P5	I/O	initial "Hi-Z" / p-ch Control / disable	Sink open drain or Tri-state I/O (Programable port option) Hysterisis input $R = 1k\Omega$ (typ.)
P7 P9	I/O	initial "Hi-Z" / p-ch Control / disable	Sink open drain or Tri-state I/O (Programable port option) $R = 1k\Omega$ (typ.)
P8	I/O	initial "Hi-Z" / disable / P.U Control / R_{IN}	Tri-state I/O Programable Pull-up resistor $R_{IN} = 70k\Omega$ (typ.) $R = 1k\Omega$ (typ.) Hysterisis input

Electrical Characteristics

(1) 87PS68

Absolute Maximum Ratings	($V_{SS} = 0$ V)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			– 0.3 to 6.5	V
Input Voltage	V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9		3.2	mA
	I_{OUT2}	Port P3		30	
Output Current (Total)	$\Sigma\ I_{OUT1}$	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9		160	mA
	$\Sigma\ I_{OUT2}$	Port P3		120	
Power Dissipation [Topr = 70°C]	PD			350	mW
Soldering Temperature (time)	Tsld			260 (10 s)	°C
Storage Temperature	Tstg			– 55 to 125	°C
Operating Temperature	Topr			– 30 to 70	°C

> *Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.*

Recommended Operating Conditions	($V_{SS} = 0$ V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc ≦ 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V	gear ratio / fc 0.4 / fc/2 0.8		8.0	MHz
			V_{DD} = 2.7 to 5.5 V	fc/4 1.6 / fc/8 3.2		4.19	
	fs	XTIN, XTOUT			30.0	34.0	kHz

> *Note 1: The recommended operating Conditions for a device are operating Conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating Conditions other than the recommended operating Conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating Conditions for the device are always adhered to.*
> *Note2: Clock frequency fc: The supply voltage range of the conditions shows the value in NORMAL1, 2 modes and·IDLE 1,2 modes.*

D.C. Characteristics

($V_{SS} = 0$ V, Topr = − 30 to 70 °C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	$V_{DD} = 5.5$ V $V_{IN} = 5.5$ V / 0 V	–	–	± 2	μA
	I_{IN2}	Sink open drain port and tri-state port					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
	R_{IN}	P8 pull-up resistor		30	70	150	
Output Leakage Current	I_{LO}	Sink open drain port and tri-state port	$V_{DD} = 5.5$ V, $V_{OUT} = 5.5$ V	–	–	2	μA
Output High Voltage	V_{OH2}	Tri-state port	$V_{DD} = 4.5$ V, $I_{OH} = − 0.7$ mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P3	$V_{DD} = 4.5$ V, $I_{OL} = 1.6$ mA	–	–	0.4	V
Output Low Current	I_{OL3}	Port P3	$V_{DD} = 4.5$ V, $V_{OL} = 1.0$ V	–	20	–	mA
Supply Current in NORMAL 1, 2 mode	I_{DD}		$V_{DD} = 5.5$ V $V_{IN} = 5.3$ V / 0.2 V fc = 8 MHz fs = 32.768 kHz	–	9	12	mA
Supply Currnt in IDLE 1, 2 mode				–	4.5	6.5	
Supply Currnt in NORMAL 1, 2 mode			$V_{DD} = 3.0$ V $V_{IN} = 2.8$ V / 0.2 V fc = 4.2 MHz fs = 32.768 kHz	–	T.B.D	T.B.D	
Supply Currnt in IDLE 1, 2 mode				–	T.B.D	T.B.D	
Supply Current in SLOW mode	I_{DD}		$V_{DD} = 3.0$ V $V_{IN} = 2.8$ V / 0.2 V fs = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	μA
Supply Current in STOP mode			$V_{DD} = 5.5$ V $V_{IN} = 5.3$ V / 0.2 V	–	0.5	10	μA

Note 1: *Typical values show those at Topr = 25°C, V_{DD} = 5V.*
Note 2: *Input current: The current through pull-up or pull-down resistor is not included.*

A / D Conversion Characteristics

($V_{SS} = 0$ V, $V_{DD} = 4.5$ to 5.5 V, Topr = − 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} − V_{ASS} \geqq 2.5$V	2.7	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Input Voltage	V_{AIN}	$V_{DD} = V_{AREF} = 5.0$ V $V_{SS} = V_{ASS} = 0.0$ V	V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}	$V_{AREF} = 5.5$ V, $V_{ASS} = 0.0$ V	—	0.5	1.0	V
Nonlinearity Error		$V_{DD} = 2.7$ to 5.5 V $V_{SS} = 0.0$ V $V_{AREF} = 2.700$ V, 5.000 V $V_{ASS} = 0.000$ V	—	—	± 1	mA
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	LSB
Total Error			—	—	± 2	

Note: *Total Error = total number of each type error excluding guantization error*

| A.C. Characteristics | | (V$_{SS}$ = 0 V, V$_{DD}$ = 4.5 to 5.5 V, Topr = − 30 to 70 °C) | | | | | |

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Machine Cycle Time	t$_{cy}$	In NORMAL1, 2 mode (gear ratio)		0.5 (1/1)	−	10 (1/8)	μs
		In IDLE1, 2 mode (gear ratio)					
		In SLOW mode		117.6		133.3	
		In SLEEP mode					
High Level Clock Pulse Width	t$_{WCH}$	For external clock operation (XIN input) fc = 8 MHz		50	−	−	ns
Low Level Clock Pulse Width	t$_{WCL}$						
High Level Clock Pulse Width	t$_{WSH}$	For external clock operation (XTIN input) fs = 32.768 kHz		14.7	−	−	μs
Low Level Clock Pulse Width	t$_{WSL}$						

Recommended Oscillating Condition

Parameter	Oscillator	Frequency	Recommended Oscillator	Recommended Condition	
				C$_1$	C$_2$
High-frequency	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA KBR4.0MS		
			MURATA CSA4.00MG		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK MX-38T	15 pF	15 pF

(1) High-frequency   (2) Low-frequency
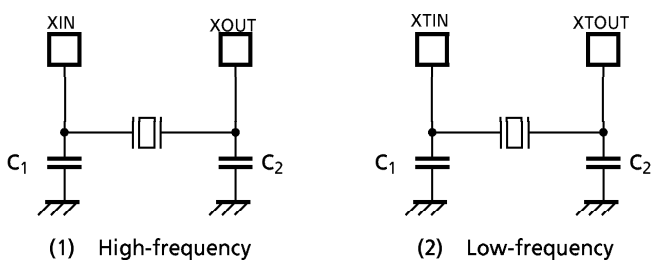
Note: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations

Note: To obtain an accurate oscillating frequency the condenser capacity must be adjusted on the sct.

| D.C./A.C. Characteristics (PROM mode) | (V_{SS} = 0 V)

(1) Read Operation

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		2.2	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	0.8	V
Power Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Program Power Supply Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	1.5tcyc + 300	–	ns

Note: tcyc = 500 ns at 8 MHz

A16 to A0

$\overline{CE}$

$\overline{OE}$

$\overline{PGM}$

t_{ACC}

D7 to D0   Hi-Z   Data outputs
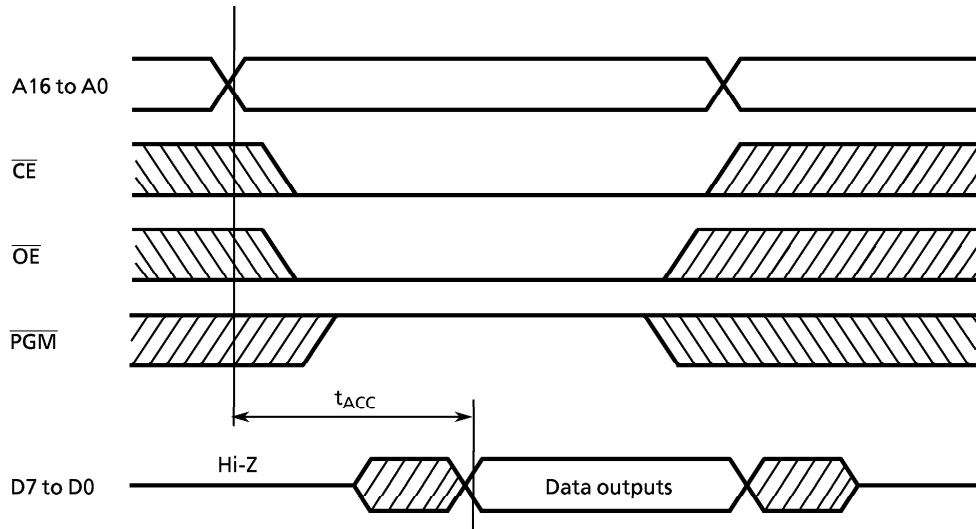
(2) High-Speed Programming Operation (Topr = 25 ± 5 °C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		2.2	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	0.8	V
Power Supply Voltage	V_{CC}		6.0	6.25	6.5	V
Program Power Supply Voltage	V_{PP}		12.5	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V	0.095	0.1	0.105	ms
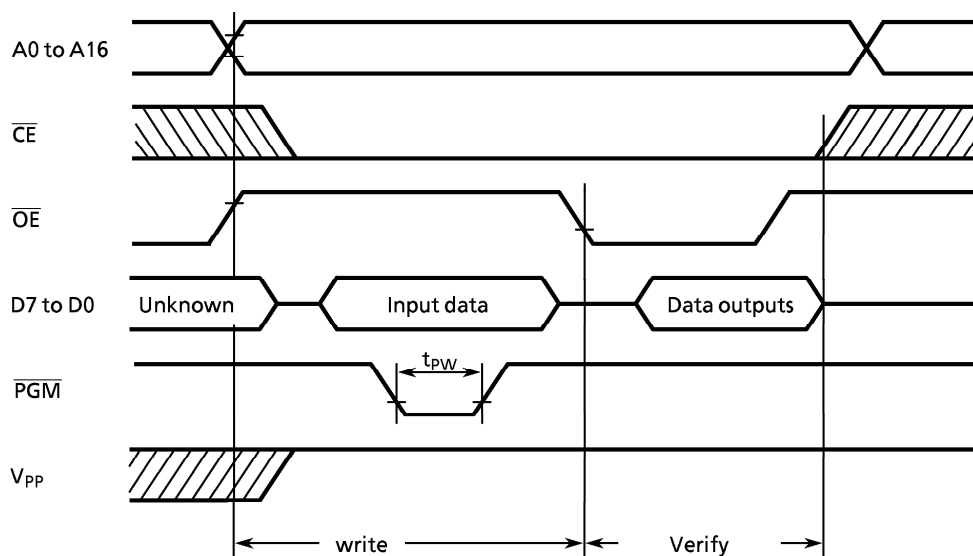
Note1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
        When V_{cc} power supply is turned off or before, V_{pp} must be increased.
Note2: The device must not be set to the EPROM programmer or picked op from it under applying the
        program voltage (12.5 V ± 0.5 V = V) to the V_{pp} pin as the device is damaged.
Note3: Be sure to execute the recommended programing mode with the recommended programing
        adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.