BLF571

HF / VHF power LDMOS transistor

Rev. 01 — 11 December 2008 Preliminary data sheet

1. Product profile

1.1 General description

A 20 W LDMOS RF transistor for broadcast applications and industrial applications in the HF and VHF band.

Table 1. Production test performance

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW	225	50	20	27.5	70

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical CW performance at frequency of 225 MHz, a supply voltage of 50 V and an I_{Dq} of 50 mA:
  - Average output power = 20 W
  - Power gain = 27.5 dB
  - Efficiency = 70 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

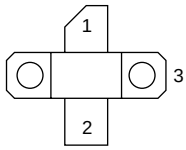
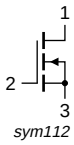
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

NXP founded by Philips

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF571	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT467C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	3.6	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 20 W	2.9	K/W

© NXP B.V. 2008. All rights reserved.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified

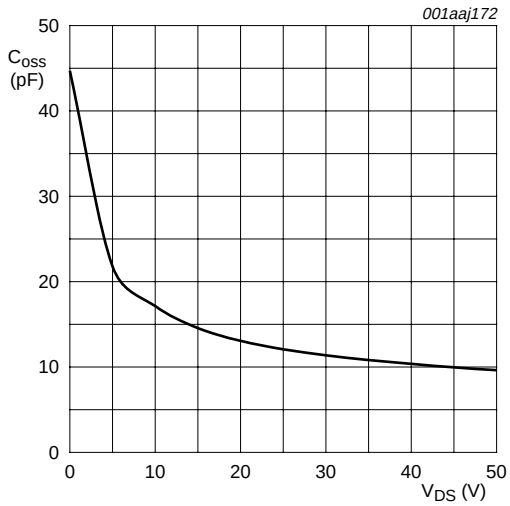
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 25 mA	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 50 mA	1.25	1.75	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	3.0	3.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1.25 A	-	1.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 833 mA	-	1.34	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.18	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	22.9	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	9.64	-	pF

Table 7. RF characteristics

Mode of operation: CW; f = 225 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 50 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 20 W	25.5	27.5	29.5	dB
RL_{in}	input return loss	P_L = 20 W	10	13	-	dB
η_D	drain efficiency	P_L = 20 W	67	70	-	%

© NXP B.V. 2008. All rights reserved.



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; capacitance value without internal matching

6.1 Ruggedness in class-AB operation

The BLF571 is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA; P_L = 20 W; f = 225 MHz.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Simulated Z_S and Z_L test circuit impedances.

f	Z_S	Z_L
MHz	Ω	Ω
225	9.7 + j31.5	31.7 + j29.3

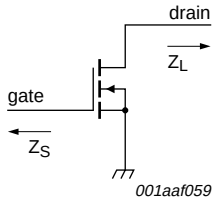
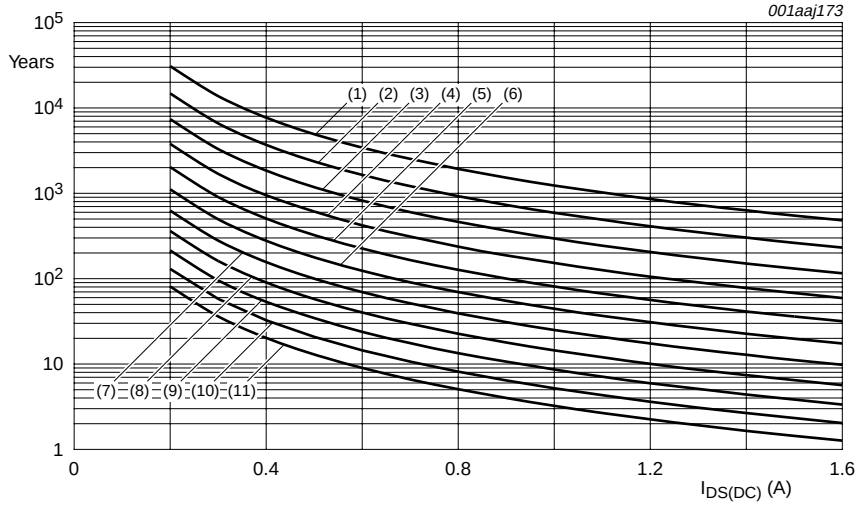


Fig 2. Definition of transistor impedance

© NXP B.V. 2008. All rights reserved.

7.2 Reliability



TTF (0.1 % failure fraction).

(1) T_j = 100 °C
(2) T_j = 110 °C
(3) T_j = 120 °C
(4) T_j = 130 °C
(5) T_j = 140 °C
(6) T_j = 150 °C
(7) T_j = 160 °C
(8) T_j = 170 °C
(9) T_j = 180 °C
(10) T_j = 190 °C
(11) T_j = 200 °C

Fig 3. BLF571 electromigration

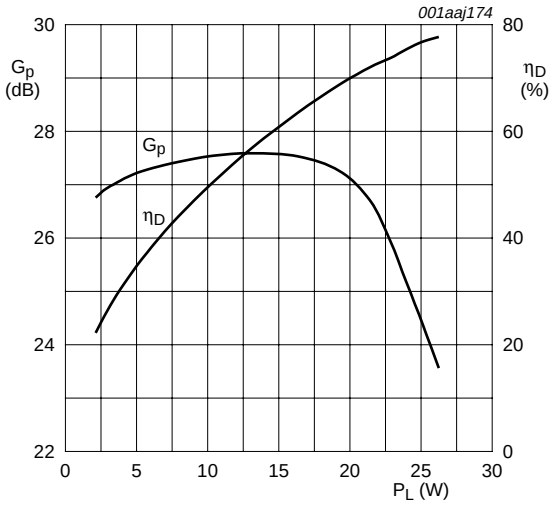
© NXP B.V. 2008. All rights reserved.

8. Test information

8.1 RF performance

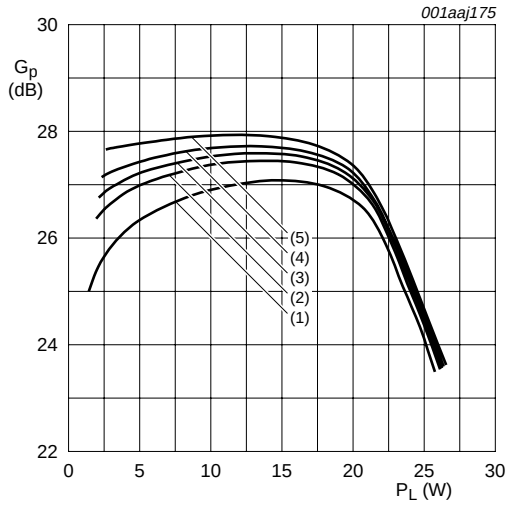
The following figures are measured in a class-AB production test circuit.

8.1.1 1-Tone CW



V_{DS} = 50 V; I_{Dq} = 50 mA; f = 225 MHz.

Fig 4. Power gain and drain efficiency as function of load power; typical values

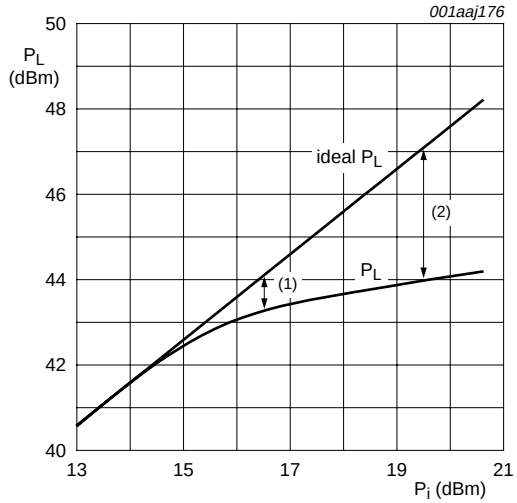


V_{DS} = 50 V; f = 225 MHz.

(1) I_{Dq} = 20 mA
(2) I_{Dq} = 40 mA
(3) I_{Dq} = 50 mA
(4) I_{Dq} = 60 mA
(5) I_{Dq} = 80 mA

Fig 5. power gain as a function of load power; typical values

© NXP B.V. 2008. All rights reserved.



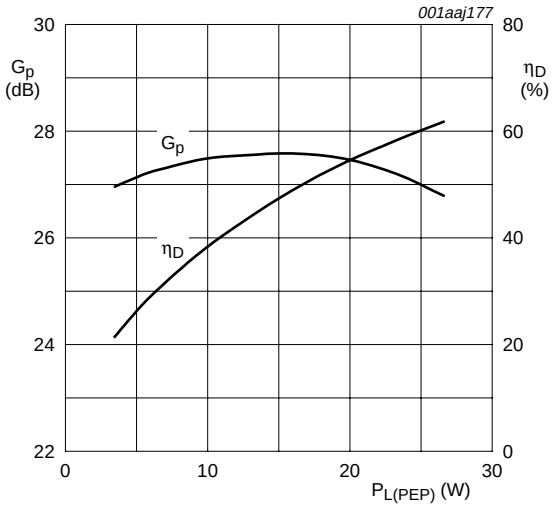
V_{DS} = 50 V; I_{Dq} = 50 mA; f = 225 MHz.

(1) $P_{L(1dB)}$ = 43.3 dBm (21.4 W)

(2) $P_{L(3dB)}$ = 44 dBm (25.1 W)

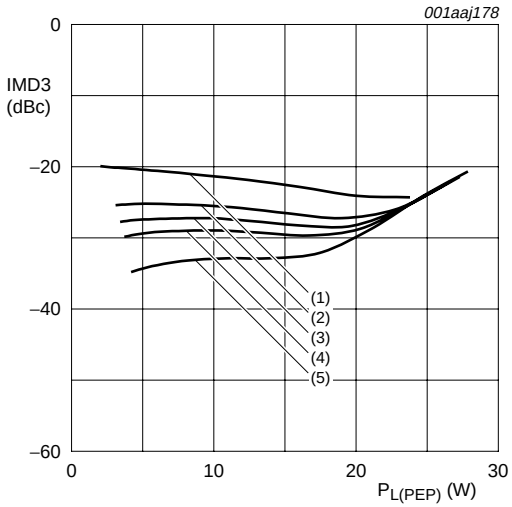
Fig 6. Load power as function of input power; typical values

8.1.2 2-Tone CW



V_{DS} = 50 V; I_{Dq} = 50 mA; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

Fig 7. Power gain and drain efficiency as function of peak envelope load power; typical values



V_{DS} = 50 V; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

(1) I_{Dq} = 20 mA

(2) I_{Dq} = 40 mA

(3) I_{Dq} = 50 mA

(4) I_{Dq} = 60 mA

(5) I_{Dq} = 80 mA

Fig 8. Third order intermodulation distortion as a function of peak envelope load power; typical values

© NXP B.V. 2008. All rights reserved.

8.2 Test circuit

Table 9. List of components

All capacitors should be soldered vertically. For test circuit, see Figure 9 and Figure 10.

Component	Description	Value		Remarks
C1, C3, C4, C5, C14	multilayer ceramic chip capacitor	100 pF	[1]	
C2	multilayer ceramic chip capacitor	39 pF	[1]	
C6	multilayer ceramic chip capacitor	68 pF	[1]	
C7, C9	multilayer ceramic chip capacitor	1 nF	[1]	
C8	multilayer ceramic chip capacitor	4.7 F		TDK C4532X7R1E475MT020U or equivalent
C10	multilayer ceramic chip capacitor	8.2 pF	[1]	
C11	electrolytic capacitor	470 F		
C12	multilayer ceramic chip capacitor	33 pF	[1]	
C13	multilayer ceramic chip capacitor	15 pF	[1]	
L1	1 turn enamelled copper wire	D = 5.5 mm; d = 1 mm; length = 1 mm		
L2	2 turns enamelled copper wire	D = 3.5 mm; d = 1 mm; length = 3 mm		
L3	5 turns enamelled copper wire	D = 6 mm; d = 1 mm; length = 5 mm		
L4	3.3 turns enamelled copper wire	D = 3 mm; d = 1 mm; length = 4 mm		
L5	3 turns enamelled copper wire	D = 3 mm; d = 1 mm; length = 3 mm		
L6	stripline	-	[2]	(L × W) 16.5 mm × 2.4 mm
L7, L8, L10, L11, L17, L19, L20	stripline	-	[2]	(L × W) 3.0 mm × 5.0 mm
L9	stripline	-	[2]	(L × W) 43.0 mm × 2.4 mm
L12, L15	stripline	-	[2]	(L × W) 3.5 mm × 2.4 mm
L13, L14	stripline	-	[2]	(L × W) 8.0 mm × 8.0 mm
L16	stripline	-	[2]	(L × W) 3.0 mm × 5.9 mm
L18	stripline	-	[2]	(L × W) 27.0 mm × 2.4 mm
L21	stripline	-	[2]	(L × W) 28.5 mm × 2.4 mm
R1	metal film resistor	1000 Ω; 0.6 W		

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.

© NXP B.V. 2008. All rights reserved.

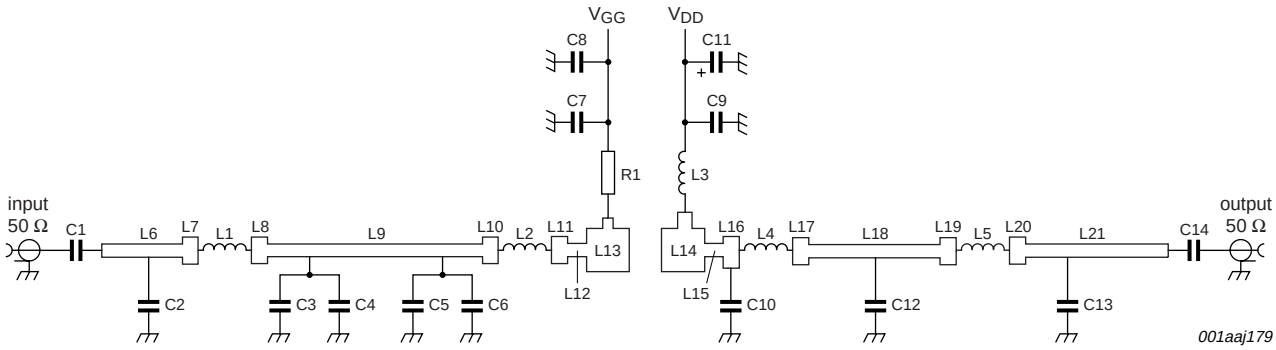


Fig 9. Class-AB common-source production test circuit

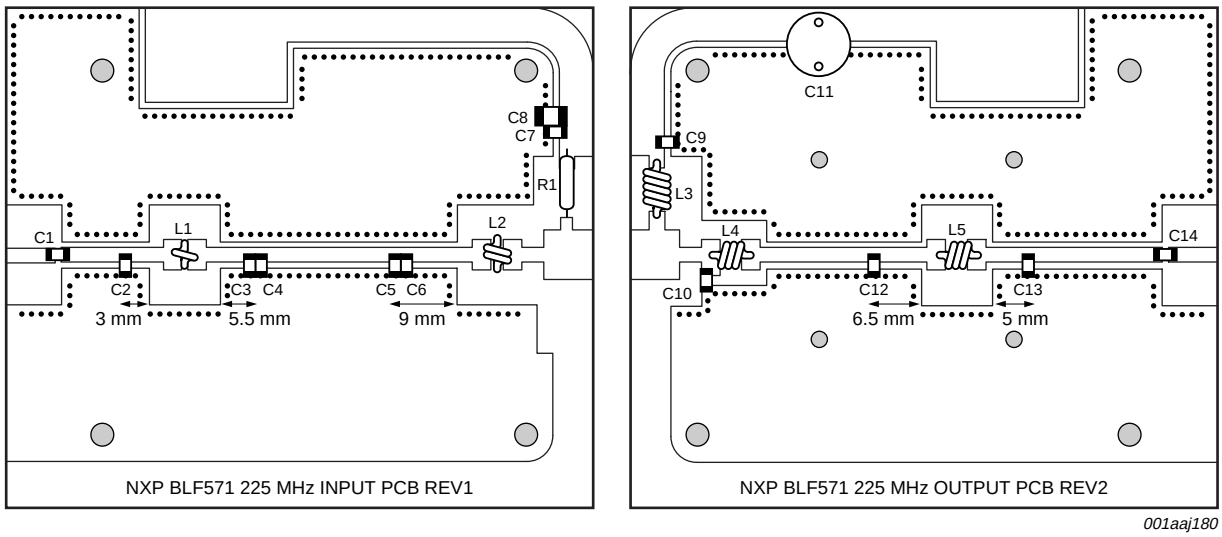
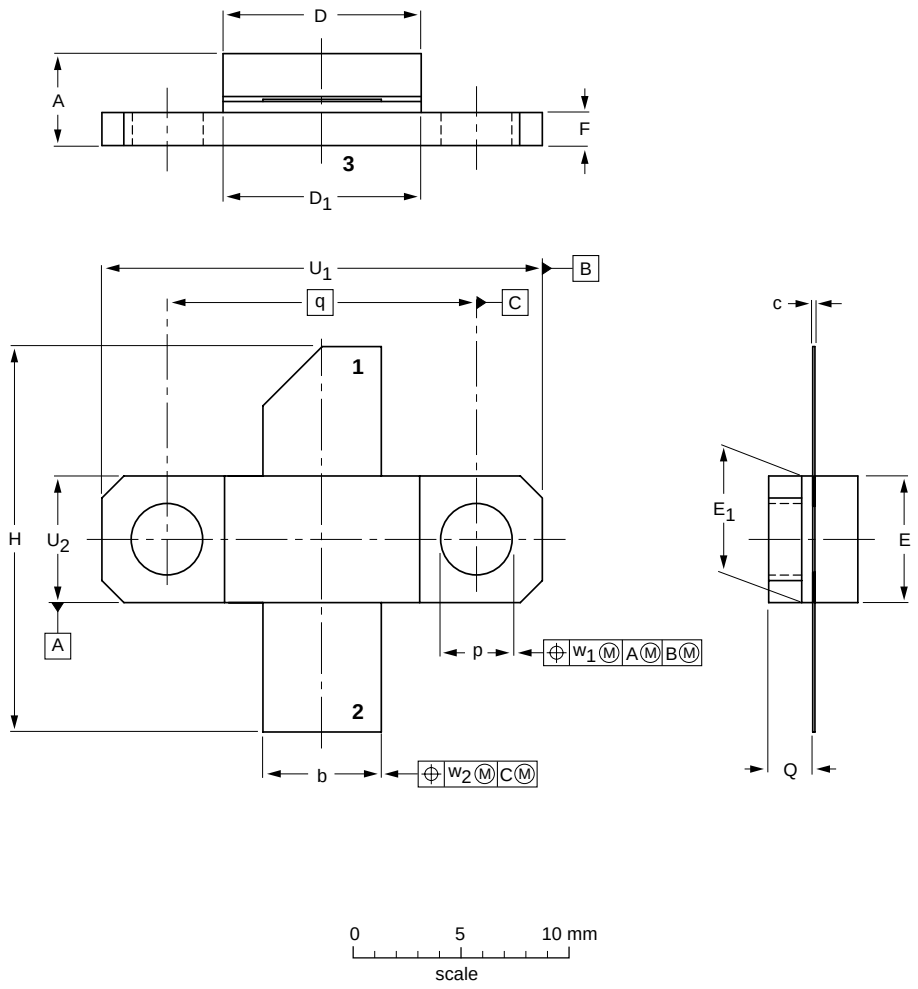


Fig 10. Component layout for class-AB production test circuit

© NXP B.V. 2008. All rights reserved.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT467C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-06~~ 99-12-28

Fig 11. Package outline SOT467C

© NXP B.V. 2008. All rights reserved.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
TTF	Time To Failure
VHF	Very High Frequency
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF571_1	20081211	Preliminary data sheet	-	-

© NXP B.V. 2008. All rights reserved.

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

12.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2008. All rights reserved.

14. Contents

1	**Product profile**	**1**
1.1	General description	1
1.2	Features	1
1.3	Applications	1
2	**Pinning information**	**2**
3	**Ordering information**	**2**
4	**Limiting values**	**2**
5	**Thermal characteristics**	**2**
6	**Characteristics**	**3**
6.1	Ruggedness in class-AB operation	4
7	**Application information**	**4**
7.1	Impedance information	4
7.2	Reliability	5
8	**Test information**	**6**
8.1	RF performance	6
8.1.1	1-Tone CW	6
8.1.2	2-Tone CW	7
8.2	Test circuit	8
9	**Package outline**	**10**
10	**Abbreviations**	**11**
11	**Revision history**	**11**
12	**Legal information**	**12**
12.1	Data sheet status	12
12.2	Definitions	12
12.3	Disclaimers	12
12.4	Trademarks	12
13	**Contact information**	**12**
14	**Contents**	**13**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 December 2008
Document identifier: BLF571_1

founded by

PHILIPS