2.5V or 3.3V, 200-MHz, 12-Output Zero Delay Buffer

Features

- Output frequency range: 8.3MHz to 125MHz
- Input frequency range: 4.2MHz to 62.5MHz
- 2.5V or 3.3V operation
- Split 2.5V/3.3V outputs
- 14 Clock outputs: Drive up to 28 clock lines
- 1 Feedback clock output
- 2 LVCMOS reference clock inputs
- 150pS max output-output skew
- PLL bypass mode
- 'SpreadTrak'
- Output enable/disable
- Pin compatible with MPC9774 and CY29774
- Industrial temperature range: -40°C to +85°C
- 52Pin 1.0mm TQFP package
- RoHS Compliance

Functional Description

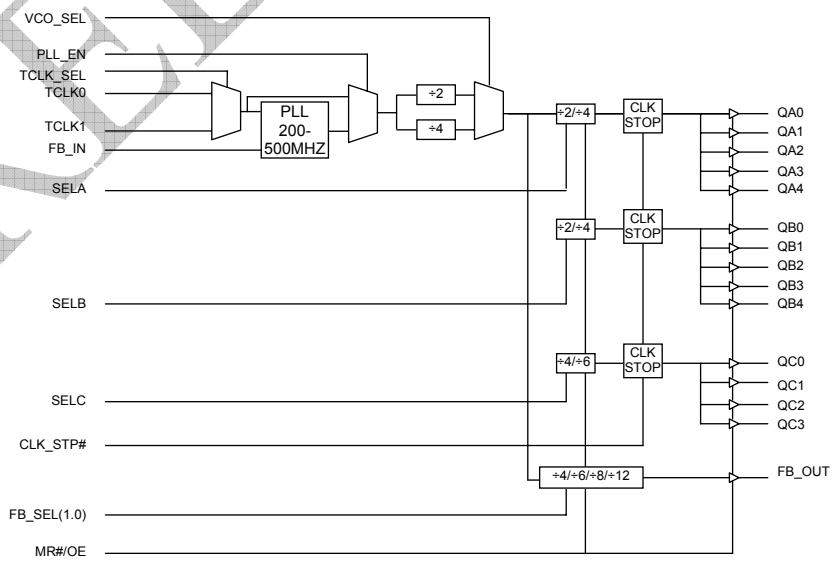
The PCS5I9774 is a low-voltage high-performance 125MHz PLL-based zero delay buffer designed for high-speed clock distribution applications.

The PCS5I9774 features two reference clock inputs and provides 14 outputs partitioned in 3 banks of 5, 5, and 4 outputs. Bank A and Bank B divide the VCO output by 4 or 8 while Bank C divides by 8 or 12 per SEL(A:C) settings, see Functional Table. These dividers allow output to input ratios of 6:1, 4:1, 3:1, 2:1, 3:2, 4:3, 1:1, and 2:3. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:28.

The PLL is ensured stable given that the VCO is configured to run between 200MHz to 500MHz. This allows a wide range of output frequencies from 8.3MHz to 125MHz. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see Frequency Table.

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Block Diagram

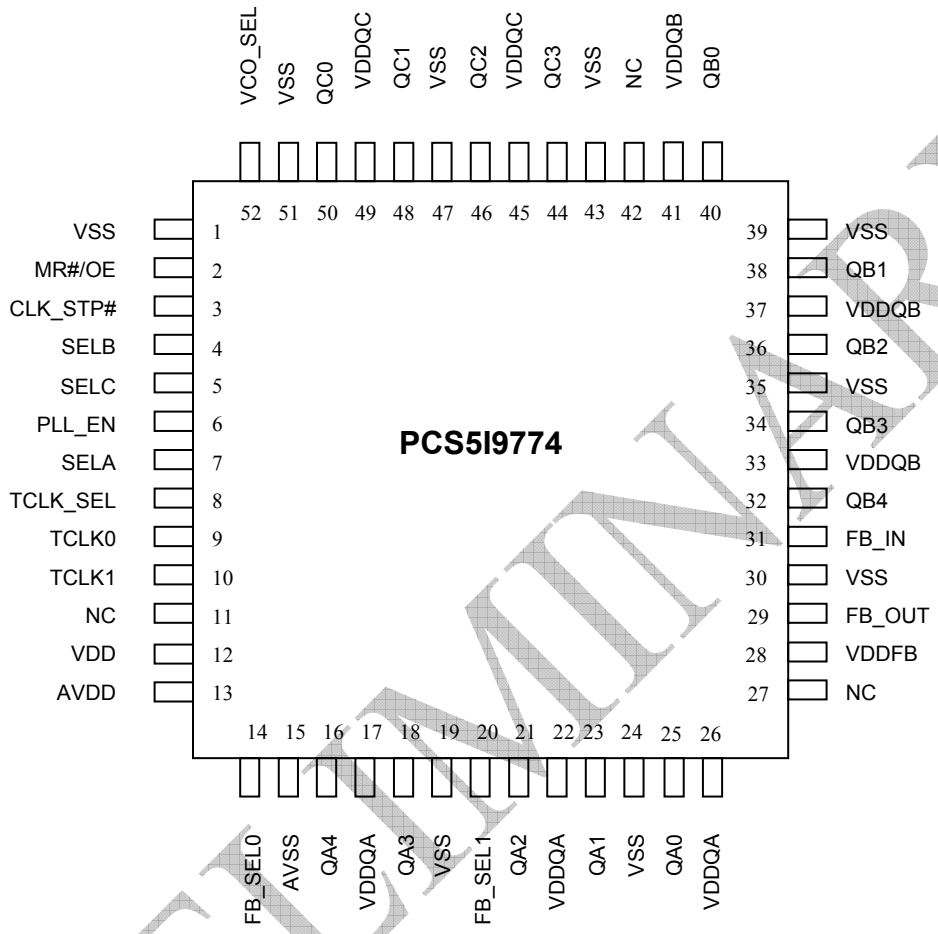


PRELIMINARY

PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200, Campbell, CA 95008 • Tel: 408-879-9077 • Fax: 408-879-9018
www.pulsecoresemi.com

Notice: The information in this document is subject to change without notice.

Pin Configuration



PRELIMINARY

Notice: The information in this document is subject to change without notice.

Pin Description[1]

Pin	Name	I/O	Type	Description
9	TCLK0	I, PD	LVCMOS	LVCMOS/LVTTL reference clock input
10	TCLK1	I, PU	LVCMOS	LVCMOS/LVTTL reference clock input
16, 18, 21, 23, 25	QA(4:0)	O	LVCMOS	Clock output bank A
32, 34, 36, 38, 40	QB(4:0)	O	LVCMOS	Clock output bank B
44, 46, 48, 50	QC(3:0)	O	LVCMOS	Clock output bank C
29	FB_OUT	O	LVCMOS	**Feedback clock output**. Connect to FB_IN for normal operation.
31	FB_IN	I, PU	LVCMOS	**Feedback clock input**. Connect to FB_OUT for normal operation. This input should be at the same voltage rail as input reference clock. See *Table 1*.
2	MR#/OE	I, PU	LVCMOS	**Output enable/disable input**. See *Table 2*.
3	CLK_STP#	I, PU	LVCMOS	**Clock stop enable/disable input**. See *Table 2*.
6	PLL_EN	I, PU	LVCMOS	**PLL enable/disable input**. See *Table 2*.
8	TCLK_SEL	I, PD	LVCMOS	**Reference select input**. See *Table 2*.
52	VCO_SEL	I, PD	LVCMOS	**VCO divider select input**. See *Table 2*.
7, 4, 5	SEL(A:C)	I, PD	LVCMOS	**Frequency select input, Bank (A:C)**. See *Table 3*.
20, 14	FB_SEL(1,0)	I, PD	LVCMOS	**Feedback dividers select input**. See *Table 4*.
17, 22, 26	VDDQA	Supply	VDD	2.5V or 3.3V Power supply for bank A output clocks[2,3]
33, 37, 41	VDDQB	Supply	VDD	2.5V or 3.3V Power supply for bank B output clocks[2,3]
45, 49	VDDQC	Supply	VDD	2.5V or 3.3V Power supply for bank C output clocks[2,3]
28	VDDFB	Supply	VDD	2.5V or 3.3V Power supply for feedback output clock[2,3]
13	AVDD	Supply	VDD	2.5V or 3.3V Power supply for PLL[2,3]
12	VDD	Supply	VDD	2.5V or 3.3V Power supply for core and inputs[2,3]
15	AVSS	Supply	Ground	Analog Ground
1, 19, 24, 30, 35, 39, 43, 47, 51	VSS	Supply	Ground	Common Ground
11, 27, 42	NC			No Connection

Note: 1.PU = Internal pull up, PD = Internal pull down.
2.A 0.1-µF bypass capacitor should be placed as close as possible to each positive power pin (<0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3.AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQA, VDDQB, VDDQC, and VDDFB power supply pins

PRELIMINARY

Notice: The information in this document is subject to change without notice.

'SpreadTrak'

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. PCS59774A is designed so as not to filter off the Spread Spectrum feature of the Reference Input, assuming it exists.

When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

Table 1. Frequency Table

Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
÷8	Input Clock * 8	25MHz to 62.5MHz	25MHz to 50MHz
÷12	Input Clock * 12	16.6MHz to 41.6MHz	16.6MHz to 33.3MHz
÷16	Input Clock * 16	12.5MHz to 31.25MHz	12.5MHz to 25MHz
÷24	Input Clock * 24	8.3MHz to 20.8MHz	8.3MHz to 16.6MHz
÷32	Input Clock * 32	6.25MHz to 15.625 MHz	6.25MHz to 12.5MHz
÷48	Input Clock * 48	4.2MHz to 10.4MHz	4.2MHz to 8.3MHz

Table 2. Function Table (configuration controls)

Control	Default	0	1
TCLK_SEL	0	TCLK0	TCLK1
VCO_SEL	0	VCO÷2 (high input frequency range)	VCO÷4 (low input frequency range)
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
MR#/OE	1	Outputs disabled (three-state) and reset of the device. During reset/output disable the PLL feedback loop is open and the VCO running at its minimum frequency. The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled
CLK_STP#	1	QA, QB, and QC outputs disabled in LOW state. FB_OUT is not affected by CLK_STP#.	Outputs enabled

Table 3. Function Table (Bank A, B and C)

VCO_SEL	SELA	QA(4:0)	SELB	QB(4:0)	SELC	QC(3:0)
0	0	÷4	0	÷4	0	÷8
0	1	÷8	1	÷8	1	÷12
1	0	÷8	0	÷8	0	÷16
1	1	÷16	1	÷16	1	÷24

PRELIMINARY

Notice: The information in this document is subject to change without notice.

Table 4. Function Table (FB_OUT)

VCO_SEL	FB_SEL1	FB_SEL0	FB_OUT
0	0	0	÷8
0	0	1	÷16
0	1	0	÷12
0	1	1	÷24
1	0	0	÷16
1	0	1	÷32
1	1	0	÷24
1	1	1	÷48

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
VDD	DC Supply Voltage		-0.3	5.5	V
VDD	DC Operating Voltage	Functional	2.375	3.465	V
V_{IN}	DC Input Voltage	Relative to VSS	-0.3	VDD+ 0.3	V
V_{OUT}	DC Output Voltage	Relative to VSS	-0.3	VDD+ 0.3	V
V_{TT}	Output termination Voltage			VDD ÷2	V
LU	Latch Up Immunity	Functional	200		mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100kHz		150	mVp-p
T_S	Temperature, Storage	Non Functional	-65	+150	°C
T_A	Temperature, Operating Ambient	Functional	-40	+85	°C
T_J	Temperature, Junction	Functional		150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional		23	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	Functional		55	°C/W
ESD_H	ESD Protection (Human Body Model)		2000		Volts
FIT	Failure in Time	Manufacturing test	10		ppm

PRELIMINARY

Notice: The information in this document is subject to change without notice.

DC Electrical Specifications (VDD = 2.5V ± 5%, T_A = -40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input Voltage, Low	LVCMOS			0.7	V
V_{IH}	Input Voltage, High	LVCMOS	1.7		VDD+0.3	V
V_{OL}	Output Voltage, Low[1]	I_{OL}= 15mA			0.6	V
V_{OH}	Output Voltage, High[1]	I_{OH}= –15mA	1.8			V
I_{IL}	Input Current, Low[2]	V_{IL}= VSS			-100	µA
I_{IH}	Input Current, High[2]	V_{IL}= VDD			100	µA
I_{DDA}	PLL Supply Current	AVDD only		5	10	mA
I_{DDQ}	Quiescent Supply Current	All VDD pins except AVDD			8	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100MHz		135		mA
C_{IN}	Input Pin Capacitance			4		pF
Z_{OUT}	Output Impedance		14	18	22	Ω

Note: 1. Driving one 50Ωparallel-terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50 Ωseries-terminated transmission lines
2. Inputs have pull-up or pull-down resistors that affect the input current.

DC Electrical Specifications (VDD= 3.3V ± 5%, T_A= -40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input Voltage, Low	LVCMOS			0.8	V
V_{IH}	Input Voltage, High	LVCMOS	2.0		VDD + 0.3	V
V_{OL}	Output Voltage, Low[1]	I_{OL}= 24 mA			0.55	V
		I_{OL}= 12 mA			0.30	
V_{OH}	Output Voltage, High[1]	I_{OH}=-24 mA	2.4			V
I_{IL}	Input Current, Low[2]	V_{IL}= VSS			-100	µA
I_{IH}	Input Current, High[2]	V_{IL}= VDD			100	µA
I_{DDA}	PLL Supply Current	AVDD only		5	10	mA
I_{DDQ}	Quiescent Supply Current	All VDD pins except AVDD			8	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100MHz		225		mA
C_{IN}	Input Pin Capacitance			4		pF
Z_{OUT}	Output Impedance		12	15	18	Ω

Note: 1. Driving one 50Ω parallel-terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50Ω series-terminated transmission lines
2. Inputs have pull-up or pull-down resistors that affect the input current.

PRELIMINARY

Notice: The information in this document is subject to change without notice.

AC Electrical Specifications (VDD = 2.5V ± 5%, T_A = -40°C to +85°C)[1]

Parameter	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency		200		400	MHz
f_{in}	Input Frequency	÷8 Feedback	25		50	MHz
		÷12 Feedback	16.6		33.3	
		÷16 Feedback	12.5		25	
		÷24 Feedback	8.3		16.6	
		÷32 Feedback	6.3		12.5	
		÷48 Feedback	4.2		8.3	
		Bypass mode (PLL_EN = 0)	0		200	
f_{refDC}	Input Duty Cycle		25		75	%
t_r, t_f	TCLK Input Rise/FallTime	0.7V to 1.7V			1.0	nS
f_{MAX}	Maximum Output Frequency	÷4 Output	50		100	MHz
		÷8 Output	25		50	
		÷12 Output	16.6		33.3	
		÷16 Output	12.5		25	
		÷24 Output	8.3		16.6	
DC	Output Duty Cycle		45		55	%
t_r, t_f	Output Rise/Fall times	0.7V to 1.8V	0.1		0.75	nS
t(φ)	Propagation Delay (static phase offset)	TCLK to FB_IN, does not include jitter	-100		100	pS
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank			150	pS
$t_{sk(B)}$	Bank-to-Bank Skew	Banks at same frequency			150	pS
		Banks at different frequency			200	
$t_{PLZ, HZ}$	Output Disable Time				10	nS
$t_{PZL, ZH}$	Output Enable Time				10	nS
BW	PLL Closed Loop Bandwidth (–3 dB)			0.5 -1.0		MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency			100	pS
		Multiple frequencies			250	
$t_{JIT(PER)}$	Period Jitter				100	pS
$t_{JIT(φ)}$	I/O Phase Jitter				125	pS
t_{LOCK}	Maximum PLL Lock Time				1	mS

Note: 1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

PRELIMINARY

Notice: The information in this document is subject to change without notice.

AC Electrical Specifications (VDD = 3.3V ± 5%, T_A = -40°C to +85°C)[1]

Parameter	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO Frequency		200		500	MHz
f_{in}	Input Frequency	÷8 Feedback	25		62.5	MHz
		÷12 Feedback	16.6		41.6	
		÷16 Feedback	12.5		31.25	
		÷24 Feedback	8.3		20.8	
		÷32 Feedback	6.25		15.625	
		÷48 Feedback	4.2		10.4	
		Bypass mode (PLL_EN = 0)	0		200	
f_{refDC}	Input Duty Cycle		25		75	%
t_r, t_f	TCLK Input Rise/FallTime	0.8V to 2.0V			1.0	nS
f_{MAX}	Maximum Output Frequency	÷4 Output	50		125	MHz
		÷8 Output	25		62.5	
		÷12 Output	16.6		41.6	
		÷16 Output	12.5		31.25	
		÷24 Output	8.3		20.8	
DC	Output Duty Cycle		45		55	%
tr, tf	Output Rise/Fall times	0.8V to 2.4V	0.1		1.0	nS
$t_{(\varphi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN, same VDD, does not include jitter	-100		100	pS
$t_{sk(O)}$	Output-to-Output Skew	Skew within Bank			150	pS
$t_{sk(B)}$	Bank-to-Bank Skew	Banks at same voltage, same frequency			150	pS
		Banks at same voltage, different frequency			225	
		Banks at different voltage			250	
$t_{PLZ, HZ}$	Output Disable Time				10	nS
$t_{PZL, ZH}$	Output Enable Time				10	nS
BW	PLL Closed Loop Bandwidth (–3dB)			0.5 - 1.0		MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency			150	pS
		Multiple frequencies			300	
$t_{JIT(PER)}$	Period Jitter				100	pS
$t_{JIT(\varphi)}$	I/O Phase Jitter	I/O at same VDD			150	pS
t_{LOCK}	Maximum PLL Lock Time				1	mS

Note: 1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Outputs are at same supply voltage unless otherwise stated. Parameters are guaranteed by characterization and are not 100% tested.

PRELIMINARY

Notice: The information in this document is subject to change without notice.

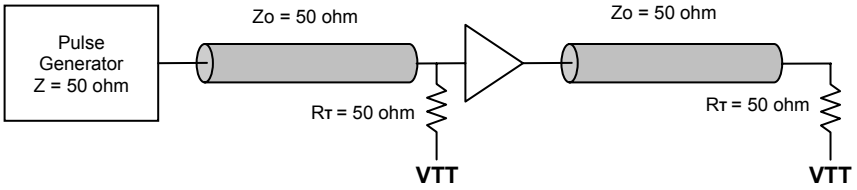


Figure 1. LVCMOS_CLK AC Test Reference for VDD = 3.3V/2.5V

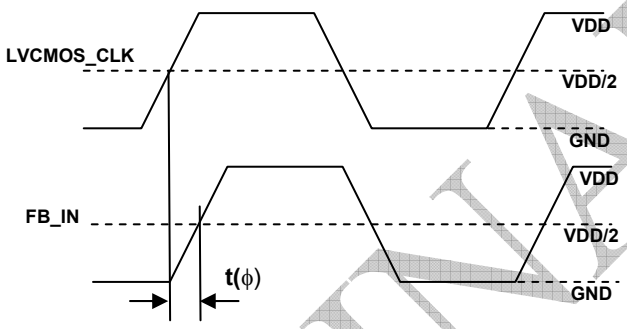


Figure 2. LVCMOS Propagation Delay $t_{(\phi)}$, Static Phase Offset

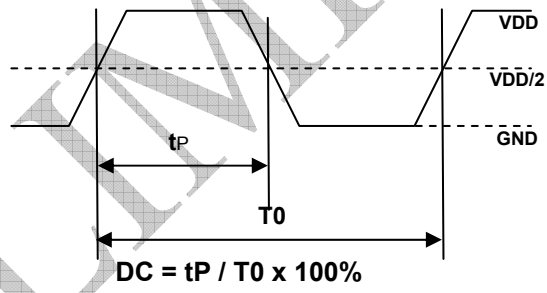


Figure 3. Output Duty Cycle (DC)

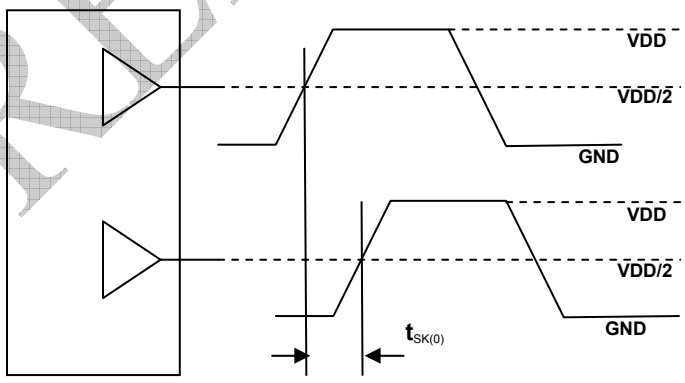


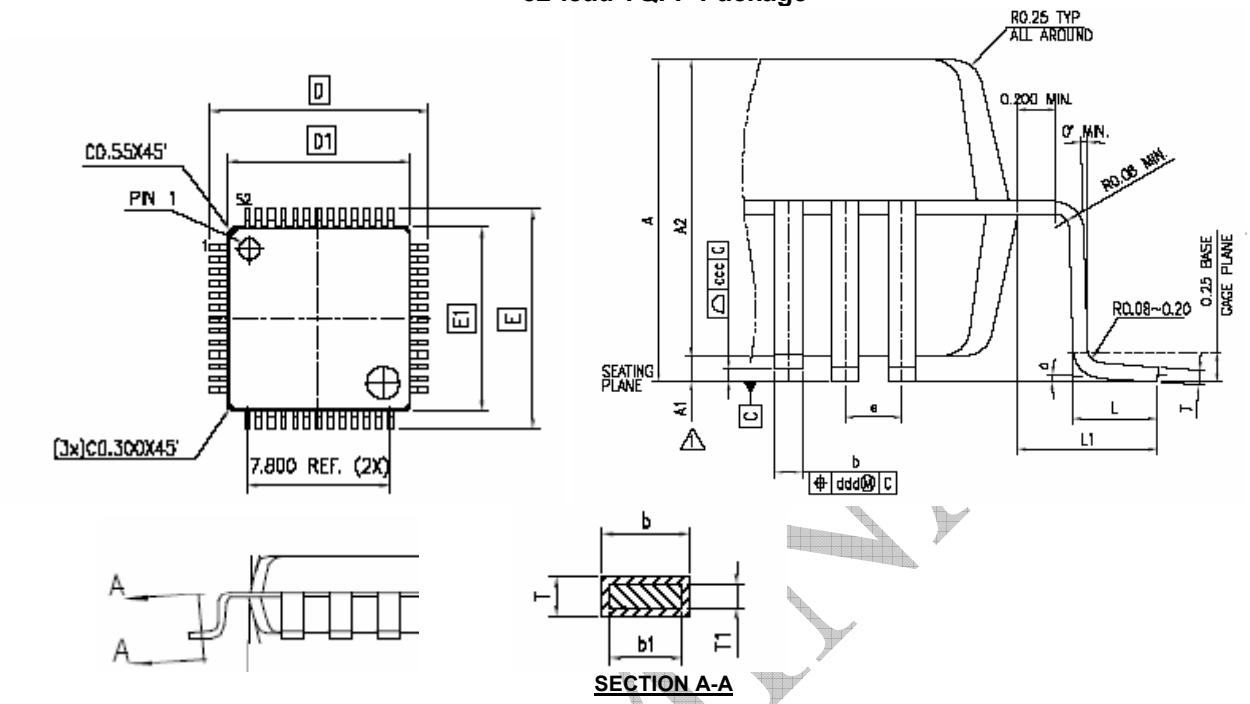
Figure 4. Output-to-Output Skew, $t_{sk(O)}$

PRELIMINARY

Notice: The information in this document is subject to change without notice.

Package Information

52-lead TQFP Package



SECTION A-A

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0472	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.4646	0.4803	11.8	12.2
D1	0.3898	0.3976	9.9	10.1
E	0.4646	0.4803	11.8	12.2
E1	0.3898	0.3976	9.9	10.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0102	0.0150	0.26	0.38
b1	0.0106	0.0130	0.27	0.33
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.0256 BASE		0.65 BASE	

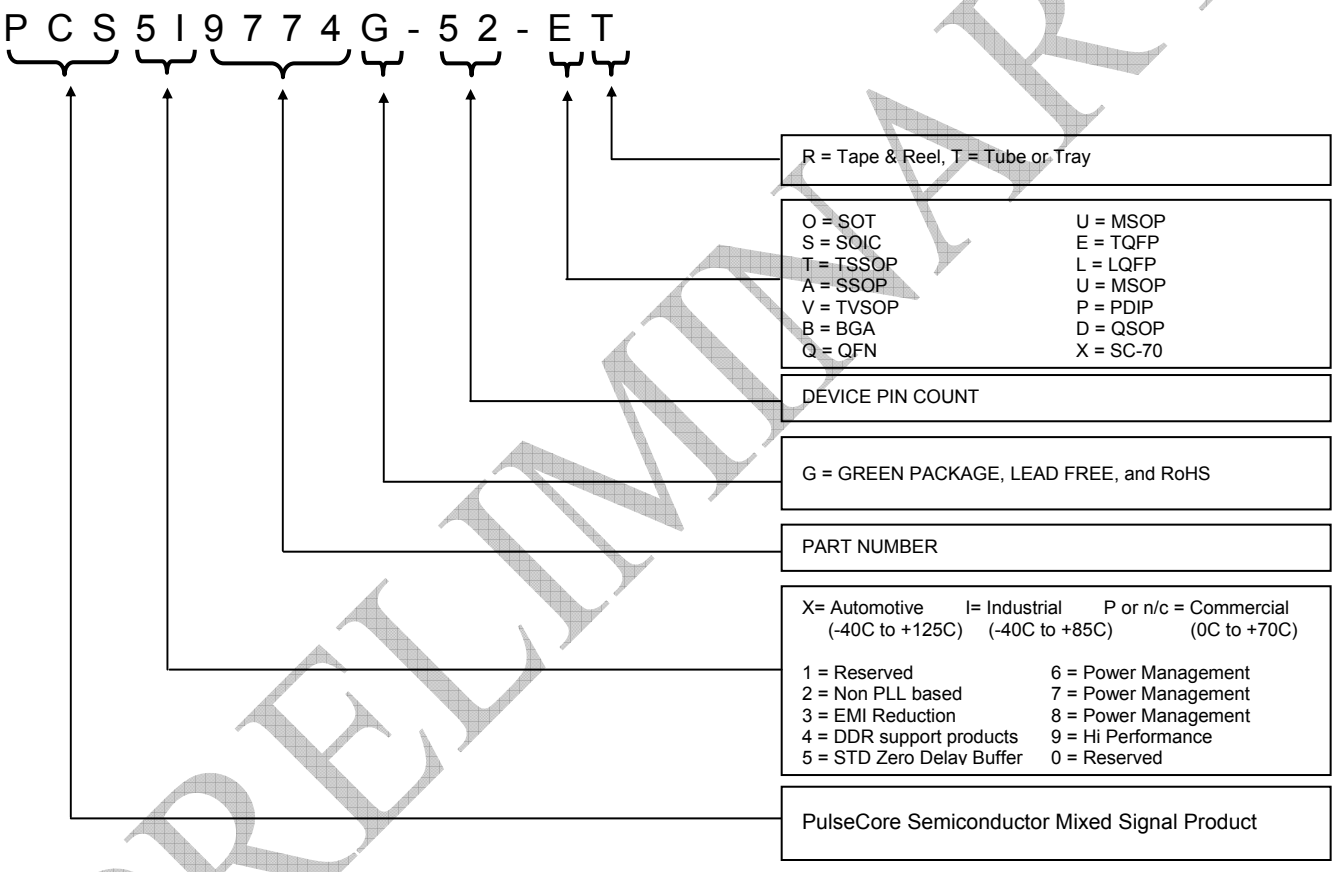
PRELIMINARY

Notice: The information in this document is subject to change without notice.

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS5P9774G-52-ET	PCS5P9774G	52-pin TQFP, Tray, Green	Commercial
PCS5P9774G-52-ER	PCS5P9774G	52-pin TQFP – Tape and Reel, Green	Commercial
PCS5I9774G-52-ET	PCS5I9774G	52-pin TQFP, Tray, Green	Industrial
PCS5I9774G-52-ER	PCS5I9774G	52-pin TQFP – Tape and Reel, Green	Industrial

Device Ordering Information



PRELIMINARY

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

Notice: The information in this document is subject to change without notice.

PRELIMINARY

PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

Copyright © PulseCore Semiconductor
All Rights Reserved
Preliminary Information
Part Number: PCS5I9774
Document Version: 0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

© Copyright 2006 PulseCore Semiconductor Corporation. All rights reserved. Our logo and name are trademarks or registered trademarks of PulseCore Semiconductor. All other brand and product names may be the trademarks of their respective companies. PulseCore reserves the right to make changes to this document and its products at any time without notice. PulseCore assumes no responsibility for any errors that may appear in this document. The data contained herein represents PulseCore's best data and/or estimates at the time of issuance. PulseCore reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. PulseCore does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of PulseCore products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in PulseCore's Terms and Conditions of Sale (which are available from PulseCore). All sales of PulseCore products are made exclusively according to PulseCore's Terms and Conditions of Sale. The purchase of products from PulseCore does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of PulseCore or third parties. PulseCore does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of PulseCore products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify PulseCore against all claims arising from such use.