Ordering number : EN7777A

SANYO Semiconductors
DATA SHEET

LA6572 — Monolithic Linear IC 5-CH Driver for Mini Disc and Compact Disk Applications (BTL : 5CH)

Overview

The LA6572 power amplifier 5-channel (BTL) built-in.

Features

- Power amplifier 5-channel (BTL) built-in.
- I_O max 1A.
- Level shift circuit built-in.
- Three channels (2-1-1) of MUTE circuit (output ON/OFF) incorporated. Only CH5 normally ON.
  (Operative independently for each of MUTE1: CH1, 2, MUTE2: CH3, MUTE3: CH4. Inoperative for 3.3REG).
- 3.3V power supply (3.3VREG) incorporated (PNP transistor connected externally).
- With 3.3V power supply (3.3VREG) ON/OFF function (EN-REG)
  (Operative for 3.3VREG only (inoperative for BTL AMP).
  (3.3VREG: OFF with EN-REG: L, 3.3VREG: ON with EN-REG : H).
- Operative for the fixed internal VREF (1.65V: TYP) for 5CH only.
- Overheat protection circuit (thermal shutdown) built-in.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	Each output for channel 1 to 5.	1	A
Maximum input voltage	VINB max		13	V
MUTE pin voltage	VMUTE		13	V
Allowable operation	Pd max	Independent IC	0.8	W
		Mounted on a specified board *	2	
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 114.3mm×76.1mm×1.6mm, glass epoxy

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Allowable Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply Voltage	V_{CC}		4.5 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8V$, VREF = 1.65V, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All Blocks						
No-load current drain ON	I_{CC}-ON	All outputs ON *1		30	50	mA
No-load current drain OFF	I_{CC}-OFF	All outputs OFF *1		10	20	mA
VREF input voltage range	VREF-IN		0.5		V_{CC}-1.5	V
VREF-OUT output voltage	VREF-OUT		1.6	1.65	1.7	V
VREF-OUT output current	I-VREF-OUT		2	5		mA
VREF changeover voltage H	VREF-SW-H	External VREF selected (VREF-SW: H)	3.5			V
VREF changeover voltage L	VREF-SW-L	Internal VREF selected (VREF-SW: L)			1.5	V
Thermal shutdown temperature	TSD	Design guarantee value *	150	175	200	°C
BTL AMP (CH1 to CH5)						
Output offset voltage	VOFF	Voltage difference between outputs for BTL AMP, each channel. *2	-50		50	mV
Input voltage range	V_{IN}	Input voltage range for input for OP-AMP.	0		V_{CC}-1.5	V
Output voltage	V_O	Each voltage between V_O^+ and V_O^- when R_L = 8Ω. *2	5.7	6.5		V
Closed-circuit voltage gain	VG	Input and output gain. Input OP-AMP: BUFFER	3.6	4	4.4	deg
Slew rate	SR	AMP Independent Multiply 2 between outputs.		0.5		V/μs
MUTE ON voltage	VMUTE-ON	Each MUTE *3	2			V
MUTE OFF voltage	VMUTE-OFF	Each MUTE *3			0.5	V
Input Amp Block						
Input voltage range	V_{IN}-OP		0		V_{CC}-1.5	V
Output offset voltage	VOFF-OP		-10		10	mV
Output current (SINK)	SINK-OP		2			mA
Output current (SOURCE)	SOURCE-OP	*4	300	500		μA
Power Supply Block (PNP Transistor: 2SB632K-Use)						
3.3V power supply output	V_{OUT}	I_O = 200mA	3.18	3.3	3.42	V
REG-IN SINK current	REG-IN-SINK	Base current to external PNP	5	10		mA
Line regulation	ΔVOLN	6V ≤ V_{CC} ≤ 12V, I_O = 200mA		20	150	mV
Load regulation	ΔVOLD	5mA ≤ I_O ≤ 200mA		50	200	mV
3.3V power supply ON voltage	REG-ON	EN voltage at which 3.3V power is turned ON. *5	2			V
3.3V power supply OFF voltage	REG-OFF	EN voltage at which 3.3V power is turned OFF. *5			0.5	V

*. This is design target value and is not measured.

*1. Current dissipation that is a sum of $V_{CC}1$ and $V_{CC}2$ at no load.

*2. Input AMP is a BUFFER AMP. $V_{IN}5+$ of CH5 is connected to VREF-OUT (CH5) (internal VREF).

*3. Voltage difference between both ends of load (8Ω). Output saturated.

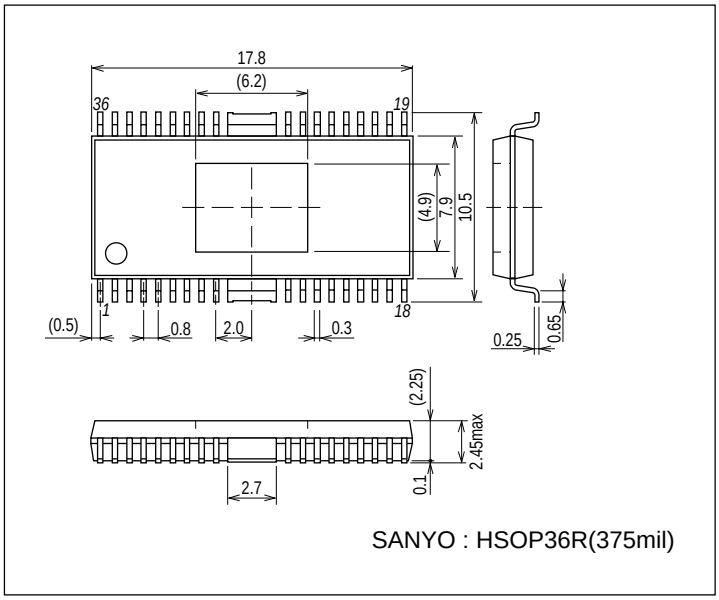
*4. The source of input OP-AMP is a constant current. As the 11kΩ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.

*5. Output ON with MUTE : “H”, output OFF with MUTE : “L” (HI impedance)

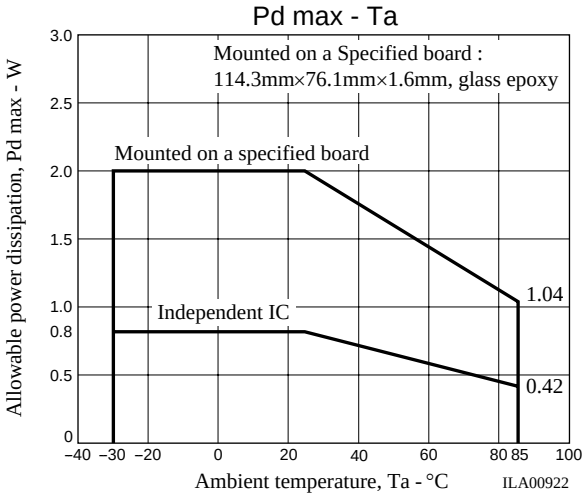
Package Dimensions

unit : mm (typ)

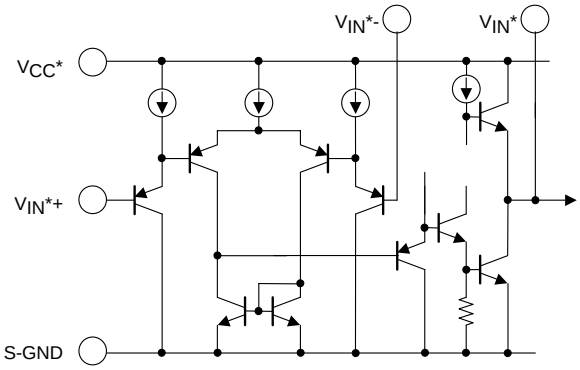
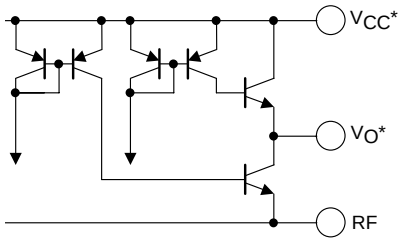
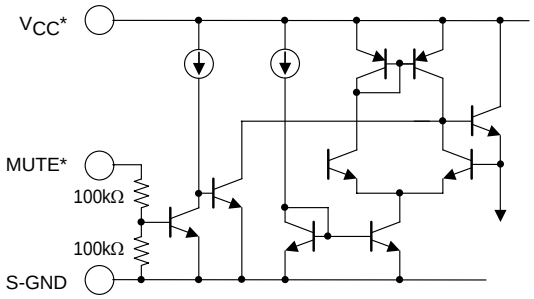
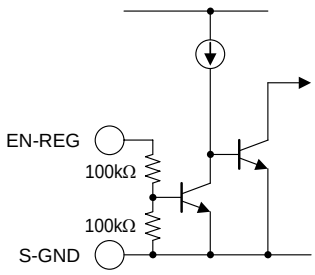
3251



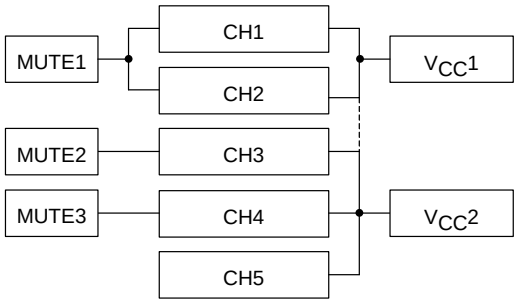
SANYO : HSOP36R(375mil)



Pin Description

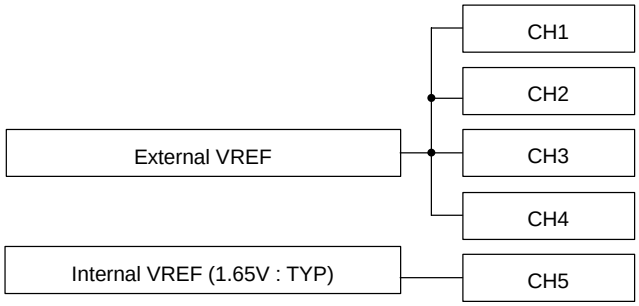
Pin Name	Pin Name	Pin No.	Equivalent Circuit Diagram	Description
Input	$V_{IN}1+$ $V_{IN}1-$ $V_{IN}1$ $V_{IN}2+$ $V_{IN}2-$ $V_{IN}2$ $V_{IN}3+$ $V_{IN}3-$ $V_{IN}3$ $V_{IN}4-$ $V_{IN}4+$ $V_{IN}4$ $V_{IN}5+$ $V_{IN}5-$ $V_{IN}5$	17 16 15 20 19 18 23 22 21 29 30 31 32 33 34		Each input pin
Output	V_O1+ V_O1- V_O2+ V_O2- V_O3+ V_O3- V_O4+ V_O4- V_O5+ V_O5-	12 13 10 11 8 9 6 7 5 4		Each output
MUTE	MUTE1 MUTE2 MUTE3	1 2 36		Turns ON/OFF the output for MUTE1 : CH1, 2, MUTE2 : CH3 and MUTE3 : CH4. Each MUTE operates independently. MUTE : H output ON MUTE : L output OFF The output has a HI impedance when OFF
EN-VREG	EN-VREG	24		3.3VREG ON/OFF pin. EN-REG ”H” : ON EN-REG ”L” : OFF

Relation of MUTE and Power (V_{CC}*)



* Connect $V_{CC}1$ and $V_{CC}2$ externally (to reduce the effects of voltage drop in the internal metal wiring).
* MUTE operates independently for each CH.

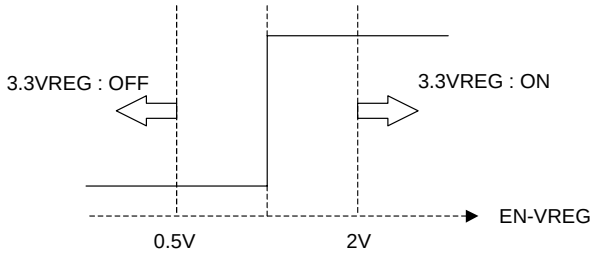
Relation of Each Channel and VREF



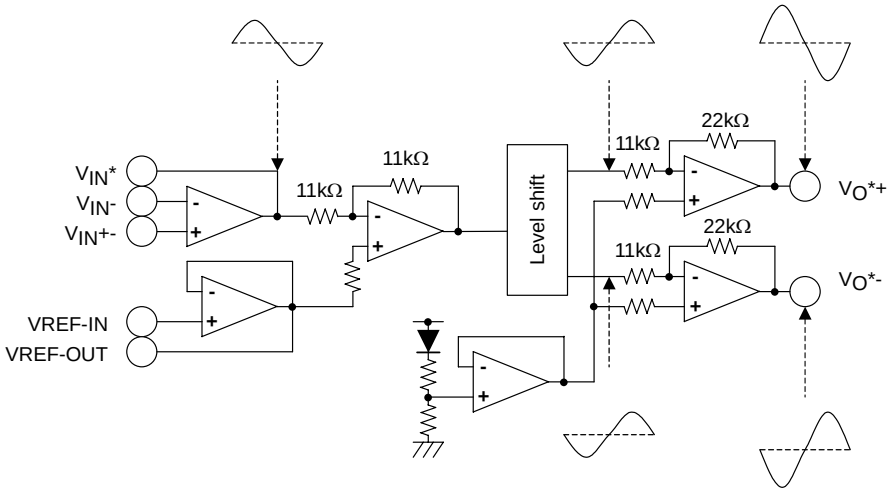
* CH1 through CH4 operate for external VREF.
  CH5 operates for internal VREF (1.65V (TYP) : fixed).

EN-REG (3.3 VREG) Operation

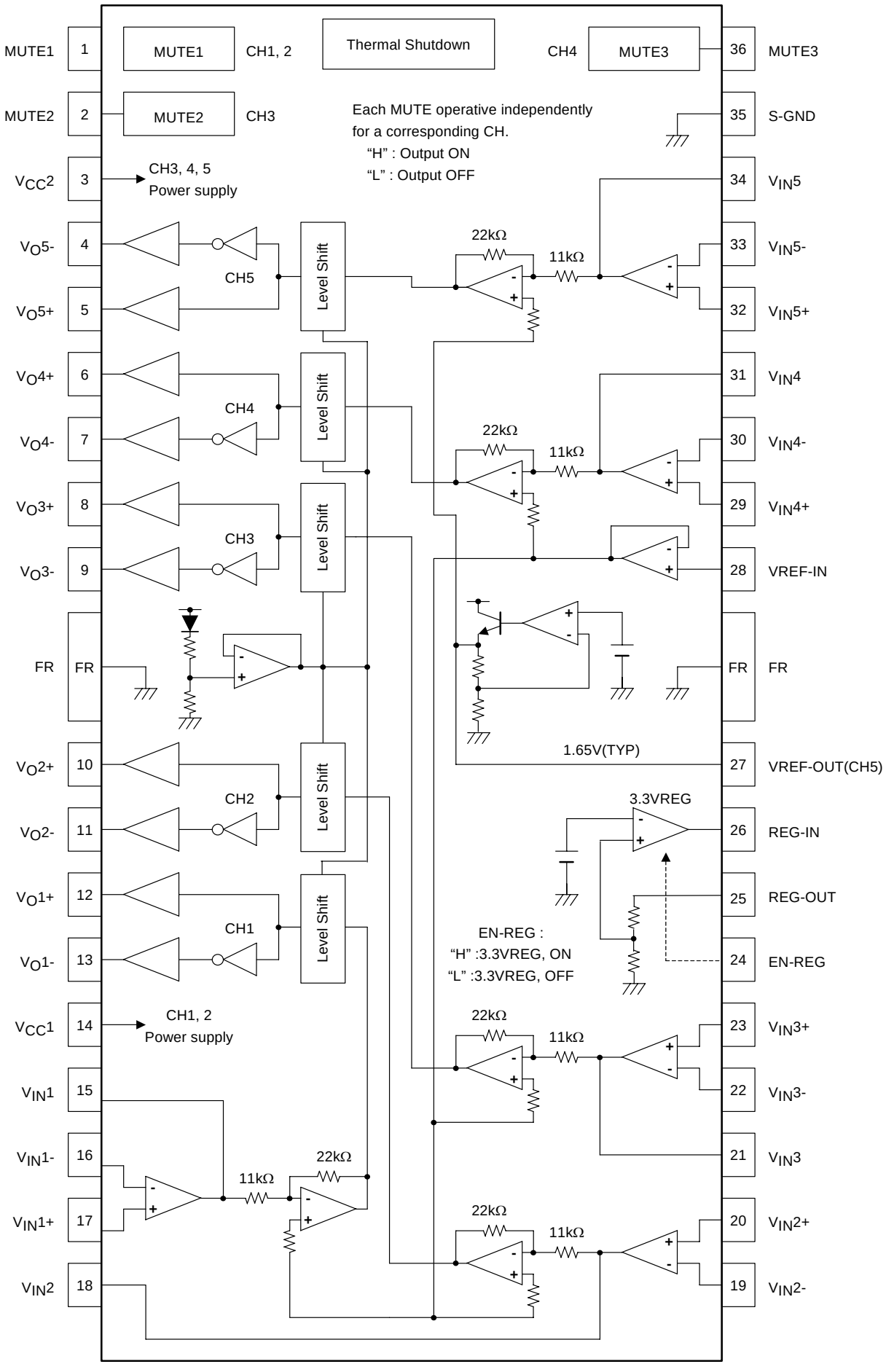
EN-REG voltage	3.3V power supply state
H	ON
L	OFF



Outline of Input and Output



Block Diagram

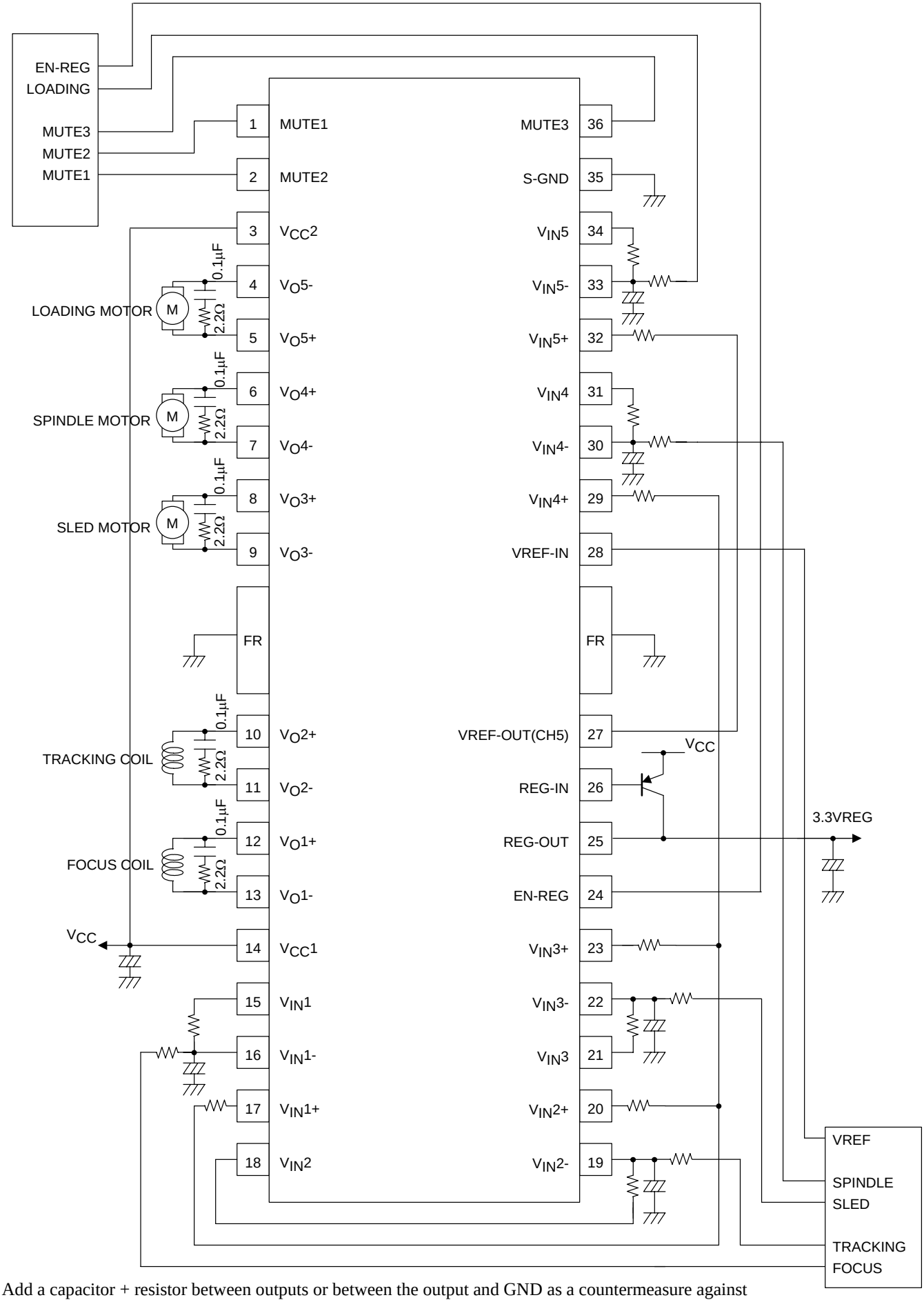


Pin Description

Pin No.	Pin Name	Description
1	MUTE1	CH1 and 2 output ON/OFF
2	MUTE2	CH3 output ON/OFF
3	$V_{CC}2$	Power supply for CH3, 4, and 5. Short-circuited with $V_{CC}1$.
4	V_O5-	Output pin (-) for channel 5
5	V_O5+	Output pin (+) for channel 5
6	V_O4+	Output pin (+) for channel 4
7	V_O4-	Output pin (-) for channel 4
8	V_O3+	Output pin (+) for channel 3
9	V_O3-	Output pin (-) for channel 3
10	V_O2+	Output pin (+) for channel 2
11	V_O2-	Output pin (-) for channel 2
12	V_O1+	Output pin (+) for channel 1
13	V_O1-	Output pin (-) for channel 1
14	$V_{CC}1$	Power supply for CH1, 2. Short-circuited with $V_{CC}2$.
15	$V_{IN}1$	Input pin for channel 1, input AMP output
16	$V_{IN}1-$	Input pin (-) for channel 1
17	$V_{IN}1+$	Input pin (+) for channel 1
18	$V_{IN}2$	Input pin for channel 2, input AMP output
19	$V_{IN}2-$	Input pin (-) for channel 2
20	$V_{IN}2+$	Input pin (+) for channel 2
21	$V_{IN}3$	Input pin for channel 3, input AMP output
22	$V_{IN}3-$	Input pin (-) for channel 3
23	$V_{IN}3+$	Input pin (+) for channel 1
24	EN-REG	3.3V ON/OFF pin that operates with 3.3VREG. EN: H→3.3VREG:ON, EN: L→3.3VREG:OFF
25	REG-OUT	Collector of PNP transistor connected to output 3.3VREG.
26	REG-IN	PNP transistor base connected
27	VREF-OUT(CH5)	VREF-AMP (CH5 output (TYP: 1.65V))
28	VREF-IN	Reference voltage applied pin
29	$V_{IN}4+$	Input pin (+) for channel 4
30	$V_{IN}4-$	Input pin (-) for channel 4
31	$V_{IN}4$	Input pin for channel 4, input AMP output
32	$V_{IN}5+$	Input pin (+) for channel 5
33	$V_{IN}5-$	Input pin (-) for channel 5
34	$V_{IN}5$	Input pin for channel 5, input AMP output
35	S-GND	Signal system GND
36	MUTE3	CH4 output ON/OFF

* Center frame (FR) becomes GND for the power system (P-GND). Set this to the minimum potential together with S-GND.

Sample Application Circuit



Add a capacitor + resistor between outputs or between the output and GND as a countermeasure against oscillation of the output.