19-4558; Rev 0; 4/09

3.3V Dual-Output LVPECL Clock Oscillator

DS4625

General Description

The DS4625 is a dual-output, low-jitter clock oscillator capable of producing frequency output pair combinations ranging from 100MHz to 625MHz. The device combines an AT-cut crystal, an oscillator, and a low-noise phase-locked loop (PLL) in a 5.0mm x 3.2mm surface-mount LCCC package. Standard frequency options are listed in the *Ordering Information/Selector Guide* table. For custom frequency options, contact the factory at: **Custom.Oscillators@maxim-ic.com**.

The DS4625 provides dual, low-voltage, positive emitter-coupled logic (LVPECL) clock output drivers. The output drivers can be enabled and disabled through the OE pin, which is an active-high CMOS input that has an internal pullup resistor. When high, both output pairs are enabled.

The device operates from a single +3.3V ±10% supply. The operating temperature range is -40°C to +70°C.

Applications

XGMII Clock Oscillator

InfiniBand™

SAS/SATA

PCIe®

1GbE/10GbE

Features

- **Standard Clock Output Frequencies: 100MHz, 125MHz, 150MHz, 156.25MHz, and 200MHz**
- **Phase Jitter < 0.7ps RMS (typical) from 12kHz to 20MHz**
- **LVPECL Output**
- **+3.3V ±10% Operating Voltage**
- **-40°C to +70°C Temperature Range**
- **Excellent Power-Supply Noise Rejection**
- **5.0mm x 3.2mm Ceramic LCCC Package**
- **Output Enable/Disable**

Ordering Information/Selector Guide

PART	TEMP RANGE	FREQUENCY (OP1:ON1) (MHz) (f_C)*	FREQUENCY (OP2:ON2) (MHz) (f_C)*	PIN-PACKAGE	TOP MARK
DS4625P+100/150	-40°C to +70°C	100.000	150.000	10 LCCC	6AC
DS4625P+125/125	-40°C to +70°C	125.000	125.000	10 LCCC	6BB
DS4625P+125/156	-40°C to +70°C	125.000	156.250	10 LCCC	6BD
DS4625P+150/150	-40°C to +70°C	150.000	150.000	10 LCCC	6CC
DS4625P+150/200	-40°C to +70°C	150.000	200.000	10 LCCC	6CE

+Denotes a lead(Pb)-free/RoHS-compliant package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Standard frequency options. Contact the factory at **Custom.Oscillators@maxim-ic.com for custom frequencies.*

Pin Configuration and Typical Application Circuit appear at end of data sheet.

InfiniBand is a trademark and service mark of the InfiniBand Trade Association.

PCIe is a registered trademark of PCI-SIG Corp.

3.3V Dual-Output LVPECL Clock Oscillator

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to ground unless otherwise noted.)
Voltage Range on Any Pin Relative to Ground.....-0.3V to +4.0V
Operating Temperature Range .....-40°C to +70°C
Junction Temperature.....+150°C

θ_{JA} .....+90°C/W (Note 1)
Storage Temperature Range .....-55°C to +85°C
Soldering Temperature (3 passes max of reflow).....Refer to the IPC/JEDEC J-STD-020 Specification.

Note 1: Package thermal resistances were obtained using a two-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		2.97	3.3	3.63	V
Input-Voltage High (OE)	V_{IH}		0.7 x V_{CC}		V_{CC}	V
Input-Voltage Low (OE)	V_{IL}		0		0.3 x V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +70°C, typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current	I_{CC_PU}	LVPECL, output unloaded		65	90	mA
	I_{CC_PL}	LVPECL, output loaded		120	140	mA
	I_{CC_OEZ}	$V_{OE} = V_{IL}$		80	115	mA
Output Frequency	f_{OUT1} / f_{OUT2}	$V_{OE} = V_{IH}$		f_C		MHz
Startup Time	t_{START}	(Note 4)		1.0		ms
Frequency Stability	$\Delta f_{TOTAL}/f_C$	Temperature, aging, load, supply, and initial tolerance (Note 5)	-50		+50	ppm
Frequency Stability Over Temperature with Initial Tolerance	$\Delta f_{TEMP}/f_C$	V_{CC} = +3.3V	-35		+35	ppm
Initial Tolerance	$\Delta f_{INITIAL}/f_C$	V_{CC} = +3.3V, T_A = +25°C		±20		ppm
Frequency Change Due to ΔV_{CC}	Δf_{VCC}	V_{CC} = +3.3V ±10%, T_A = +25°C	-3		+3	ppm/V
Frequency Change Due to Load Variation	$\Delta f_{LOAD}/f_C$	±10% variation in termination resistance		±1		ppm
Aging (15 Years)	$\Delta f_{AGING}/f_C$		-7		+7	ppm
OE Pullup Resistance	R_{PU}	T_A = +25°C	70	100	130	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +70°C, typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.085		V_{CC} - 0.88	V
Output Low Voltage	V_{OL}	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	V_{CC} - 1.825		V_{CC} - 1.62	V
Differential Output Voltage	$\lvert V_{OD} \rvert$	Output connected to 50Ω at PECL_BIAS at V_{CC} - 2.0V	0.595	0.710		V
Output Rise Time	t_R	20% to 80%		200		ps
Output Fall Time	t_F	80% to 20%		200		ps
Duty Cycle	D_{CYCLE}		45		55	%
Propagation Delay from OE Going Low to Output High Impedance	t_{PAZ}	(See Figure 2)			100	ns
Propagation Delay from OE Going High to Output Active	t_{PZA}	(See Figure 2)			100	ns
Jitter	J_{RMS}	Integrated phase RMS, 12kHz to 20MHz, V_{CC} = +3.3V, T_A = +25°C		0.7		ps
Accumulated Deterministic Jitter Due to Reference Spurs		125.00MHz output, V_{CC} = +3.3V, T_A = +25°C		0.1		ps
Accumulated Deterministic Jitter Due to Power-Supply Noise (P-P) (Note 6)		10kHz		12.9		ps
		100kHz		26.3		ps
		200kHz		20.1		ps
		1MHz		6.4		ps

Note 2: Limits at -40°C are guaranteed by design and are not production tested.
Note 3: AC parameters are guaranteed by design and not production tested.
Note 4: Startup time is from V_{CC} = V_{CCMIN} until PLL locks to the crystal oscillator output.
Note 5: Frequency stability is calculated as: $\Delta f_{TOTAL} = \Delta f_{TEMP} + \Delta f_{VCC} \times (3.3 \times 10\%) + \Delta f_{LOAD} + \Delta f_{AGING}$.
Note 6: Supply-induced jitter is the deterministic jitter as measured on a LeCroy SDA11000 measured with a 50mV_{P-P} sine wave forced on V_{CC}.

SINGLE-SIDEBAND PHASE NOISE

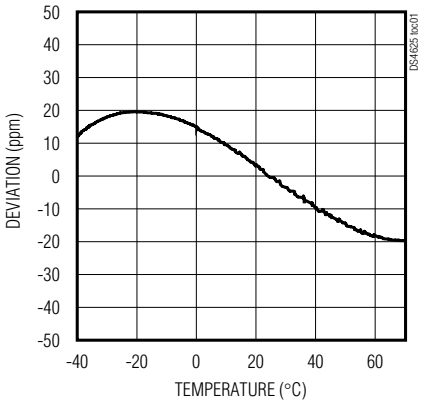
SSB PHASE NOISE (dBc/Hz) (TYPICAL, +25°C, +3.3V)						UNITS
OFFSET	f_C = 100MHz	f_C = 125MHz	f_C = 150MHz	f_C = 156.25MHz	f_C = 200MHz	
100Hz	-71	-85	-84	-79	-85	dBc/Hz
1kHz	-116	-117	-116	-115	-113	
10kHz	-119	-118	-116	-117	-113	
100kHz	-126	-125	-122	-123	-120	
1MHz	-143	-142	-141	-140	-139	
10MHz	-151	-149	-149	-148	-149	
20MHz	-151	-150	-149	-149	-150	

3.3V Dual-Output LVPECL Clock Oscillator

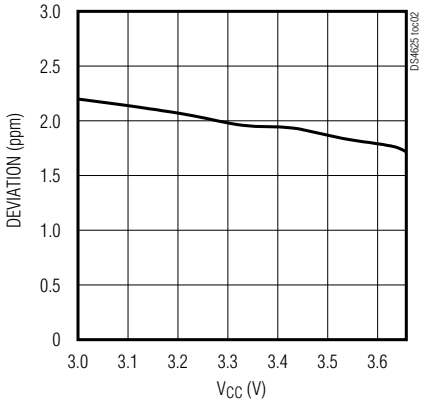
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

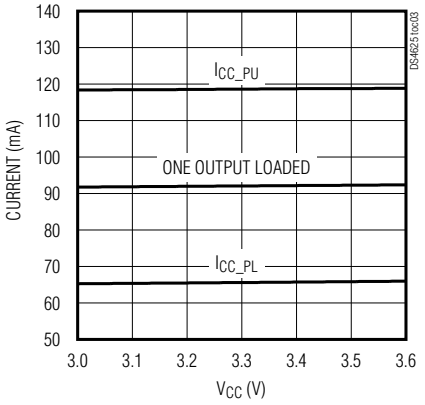
f_C DEVIATION vs. TEMPERATURE



f_C DEVIATION vs. V_{CC}



I_{CC} vs. V_{CC}



Pin Description

PIN	NAME	FUNCTION
1	OE	Active-High Output Enable. Has an internal pullup resistor (R_{PU}).
2, 3	GND	Ground
4	OP1	Positive Output 1 for LVPECL
5	ON1	Negative Output 1 for LVPECL
6	V_{CC}	Supply Voltage Input
A1, A2	N.C.	No Internal Connection. Must be connected to ground.
A3	OP2	Positive Output 2 for LVPECL
A4	ON2	Negative Output 2 for LVPECL
—	EP	Exposed Pad. The exposed pad must be used for thermal relief. This pad must be connected to ground.

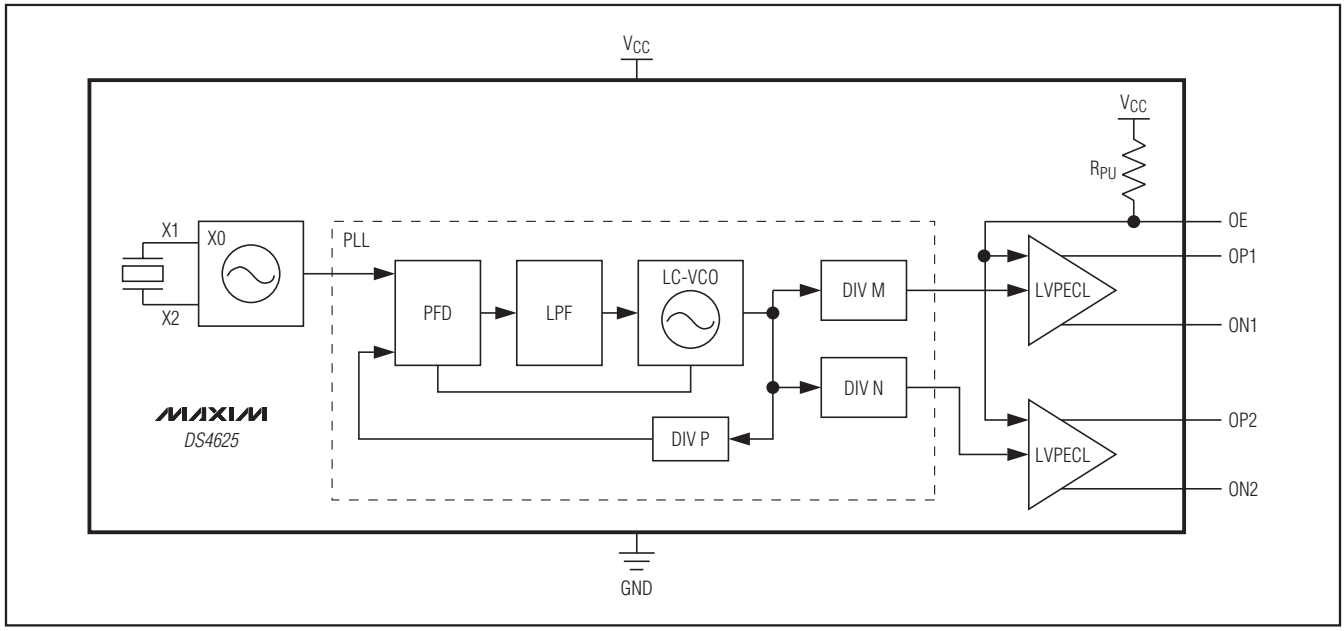


Figure 1. Block Diagram

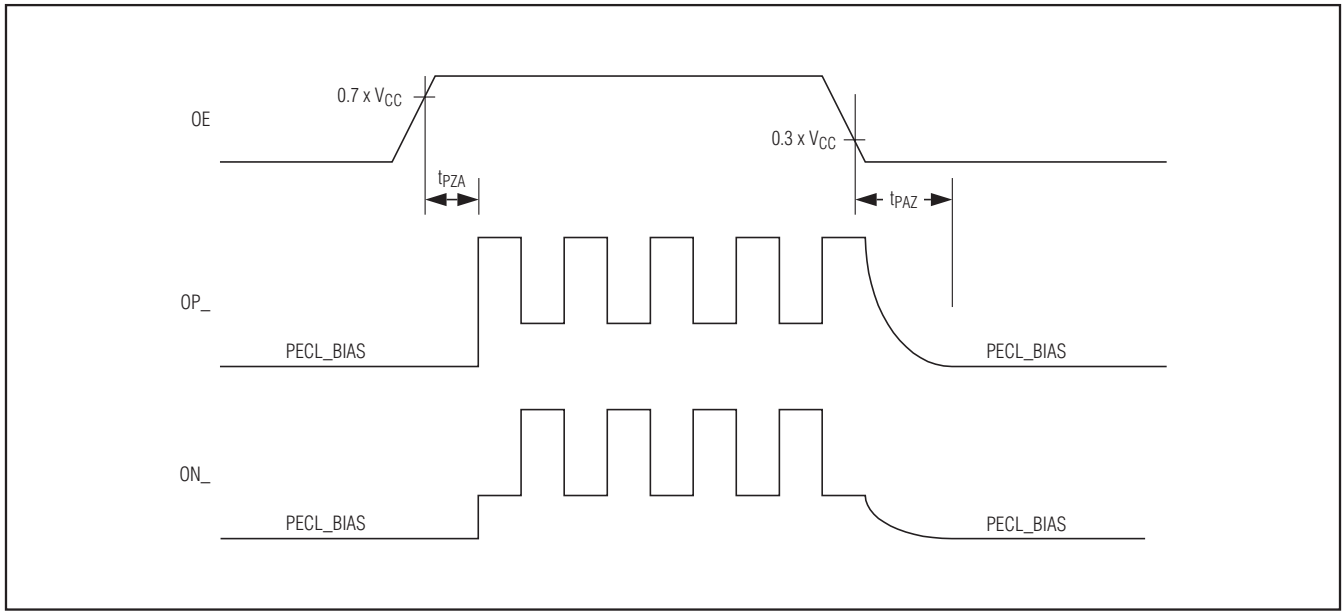
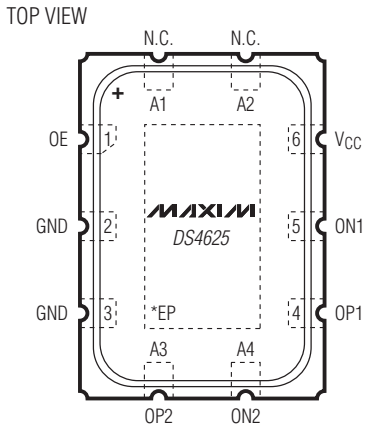


Figure 2. LVPECL Output Timing Diagram When OE is Enabled and Disabled

3.3V Dual-Output LVPECL Clock Oscillator

Pin Configuration



LCCC
(5.00mm × 3.20mm × 1.49mm)

*EXPOSED PAD

Detailed Description

The DS4625 is a dual-output, low-jitter clock oscillator that produces frequency output pair combinations as shown in the *Ordering Information/Selector Guide* table. The phase relationship between the outputs is not guaranteed. The device combines an AT-cut, fundamental-mode crystal, an oscillator, and a low-noise PLL in a 5.0mm x 3.2mm surface-mount LCCC package.

The DS4625 provides dual LVPECL clock output drivers. The output drivers can be enabled and disabled through the OE pin. The OE pin is an active-high CMOS input that has an internal pullup resistor. When OE is high, both output pairs are enabled.

Chip Information

PROCESS: Bipolar SiGe

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 LCCC	L1053+H2	**21-0389**

Typical Application Circuit