Data Sheet | May 29, 2009 | FN6633.0

Precision Single and Dual Low Noise Operational Amplifiers

The ISL28127 and ISL28227 are very high precision amplifiers featuring very low noise, low offset voltage, low input bias current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28127 single is available in an 8 Ld SOIC package. The ISL28227 dual amplifier will be offered in 8 Ld SOIC package. All devices are offered in standard pin configurations and operate over the extended temperature range to -40°C to +125°C.

Ordering Information

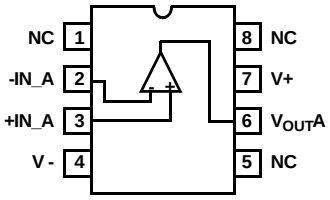
PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28127FBZ*	28127 FBZ	8 Ld SOIC	MDP0027
Coming Soon ISL28227FBZ*	28227 FBZ	8 Ld SOIC	MDP0027

*Add “-T13” suffix for tape and reel.Please refer to TB347 for details on reel specifications.

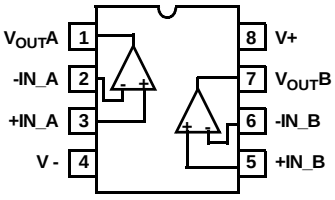
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL28127 (8 LD SOIC) TOP VIEW



ISL28227 (8 LD SOIC) TOP VIEW



Features

- Very Low Voltage Noise 2.5nV/Hz
- Low Input Offset . . . . . 70µV, Max.
- Superb Offset Drift . . . . . .0.5µV/°C, Max.
- Input Bias Current . . . . . .10nA, Max.
- Wide Supply Range . . . . . .4.5V to 40V
- Gain-bandwidth Product. . . . . .10MHz Unity Gain Stable
- Low Current Consumption 2.2mA
- Outstanding ESD performance
  - Human Body Model 4.0kV
  - Machine Model 500V
  - Charged Device Model 1.5kV
- Operating Temperature Range . . . . . .-40°C to +125°C
- No Phase Reversal
- Pb-Free (RoHS Compliant)

Applications

- Precision Instruments
- Medical Instrumentation
- Spectral Analysis Equipment
- Geophysical Analysis Equipment
- Telecom Equipment
- Active Filter Blocks
- Microphone Pre-amplifier
- Thermocouples and RTD Reference Buffers
- Data Acquisition
- Power Supply Control

Absolute Voltage Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 0.5V
Min/Max Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
Max/Min Input current for input voltage >V+ or <V- . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time) . . . . . Indefinite
ESD Tolerance
Human Body Model 4.0kV
Machine Model 500V
Charged Device Model 1.5kV

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
8 Ld SOIC Package 120
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
V_{OS}	Offset Voltage			10	70	µV
					120	µV
V_{OS}/T	Offset Voltage Drift			**0.1**	**0.5**	µV/°C
I_{OS}	Input Offset Current			1	10	nA
					12	nA
I_B	Input Bias Current			1	10	nA
					12	nA
V_{CM}	Input Voltage Range	Guaranteed by CMRR	-13		13	V
			-12		**12**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	115	120		dB
		V_{CM} = -12V to +12V	**115**			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	115	125		dB
		V_S = ±3V to ± 20V	**115**			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V R_L = 10kΩ to ground	1000	1500		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.65		V
			13.2			V
		R_L = 2kΩ to ground	13.4	13.5		V
			13.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.65	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.5	-13.4	V
					-13.1	V
I_S	Supply Current/Amplifier			2.2	2.8	mA
					3.7	mA

Electrical Specifications V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
I_{SC}	Short-Circuit	R_L = 0Ω to ground		±45		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	±2.25		±20	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			10		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		85		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		3		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		2.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		2.5		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		2.5		nV/√Hz
in	Current Noise Density	f = 10kHz		0.4		pA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 2kΩ		0.00022		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ, V_O = 4V_{P-P}		±3.6		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		36		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		38		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = -1 V_{OUT} = 10V_{P-P}, R_g = R_f =10k, R_L = 2kΩ to V_{CM}		3.4		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_L = 2kΩ to V_{CM}		3.8		µs
t_{OL}	Output Overload Recovery Time	A_V = 100, V_{IN} = 0.2V R_L = 2kΩ to V_{CM}		1.7		µs

Electrical Specifications V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
V_{OS}	Offset Voltage			10	70	µV
					120	µV
V_{OS}/T	Offset Voltage Drift			**0.1**	**0.5**	µV/°C
I_{OS}	Input Offset Current			1	10	nA
					12	nA
I_B	Input Bias Current			1	10	nA
					12	nA
V_{CM}	Common Mode Input Voltage Range	Guaranteed by CMRR	-3		3	V
			-2		**2**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	115	120		dB
		V_{CM} = -2V to +2V	**115**			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	115	125		dB
		V_S = ±3V to ±5V	**115**			dB

Electrical Specifications V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
A_{VOL}	Open-Loop Gain	V_O = -3V to +3V R_L = 10kΩ to ground	1000	1500		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.65		V
			3.2			V
		R_L = 2kΩ to ground	3.4	3.5		
			3.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.65	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.5	-3.4	
					-3.1	V
I_S	Supply Current/Amplifier			2.2	2.8	mA
					3.7	mA
I_{SC}	Short-Circuit			± 45		mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			10		MHz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, Vo = 2.5V_{RMS}, R_L = 2kΩ		0.0034		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ		±3.6		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		36		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = -1, V_{OUT} = 100mV_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		38		ns
t_s	Settling Time to 0.1%	A_V = -1, V_{OUT} = 4V_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		1.6		µs
	Settling Time to 0.01%	A_V = -1, V_{OUT} = 4V_{P-P}, R_f = R_g = 2kΩ, R_L = 2kΩ to V_{CM}		4.2		µs

NOTE:

2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

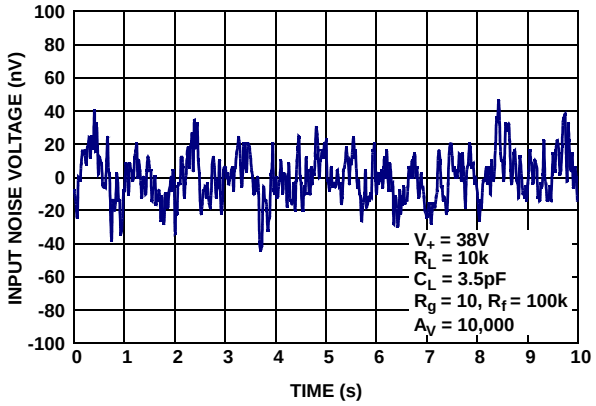


FIGURE 1. INPUT NOISE VOLTAGE 0.1Hz to 10Hz

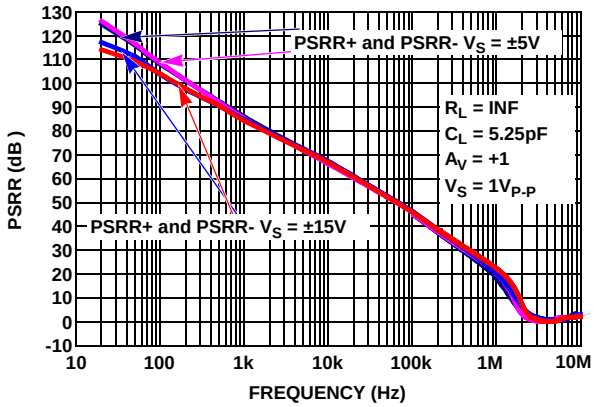


FIGURE 2. PSRR vs FREQUENCY, V_S = ±5V, ±15V

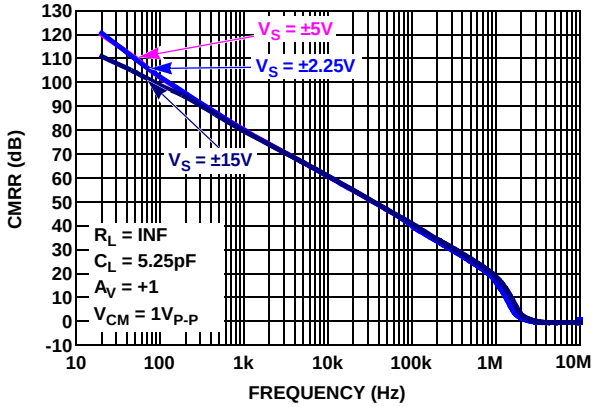


FIGURE 3. CMRR vs FREQUENCY, V_S = ±2.25, ±5V, ±15V

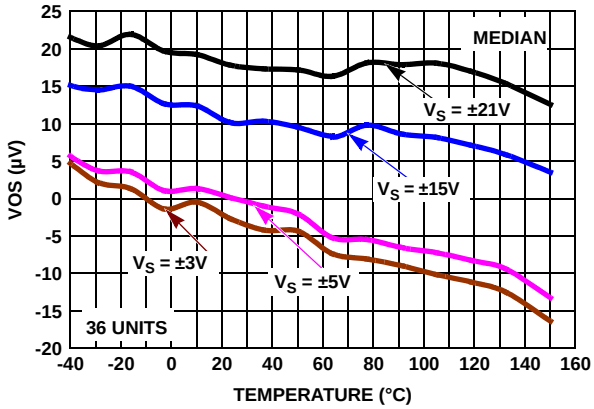


FIGURE 4. V_{OS} vs TEMPERATURE vs V_{SUPPLY}

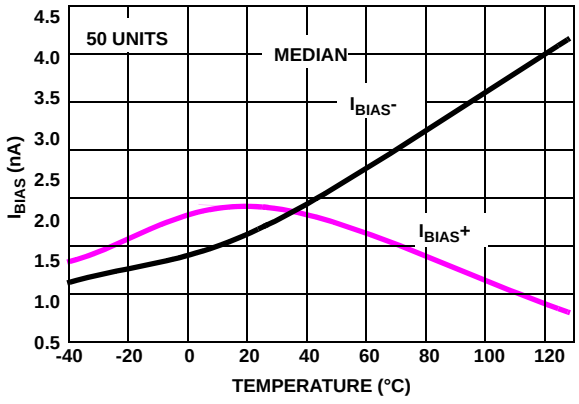


FIGURE 5. I_{IB} vs TEMPERATURE, V_S = ±15V

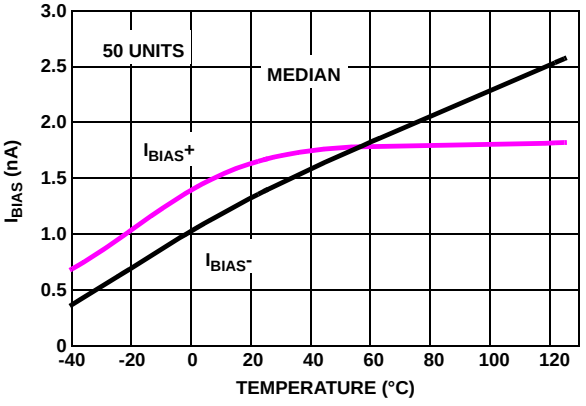


FIGURE 6. I_{IB} vs TEMPERATURE, V_S = ±5V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

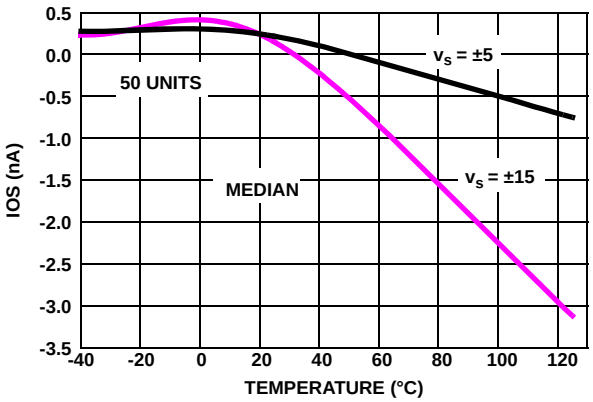


FIGURE 7. I_{OS} vs TEMPERATURE vs SUPPLY

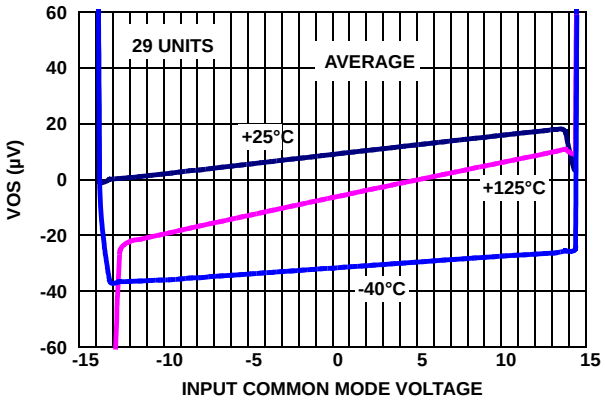


FIGURE 8. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, V_S = ±15V

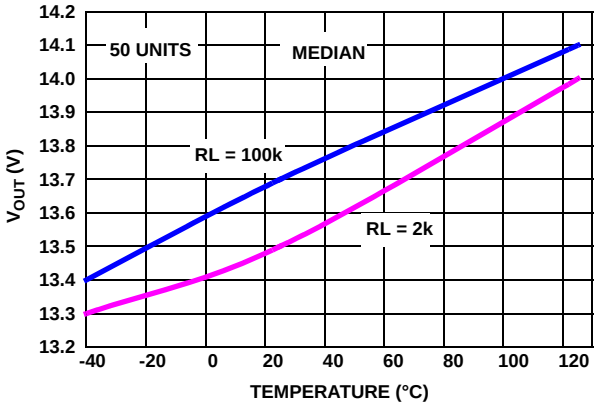


FIGURE 9. V_{OH} vs TEMPERATURE, V_S = ±15V

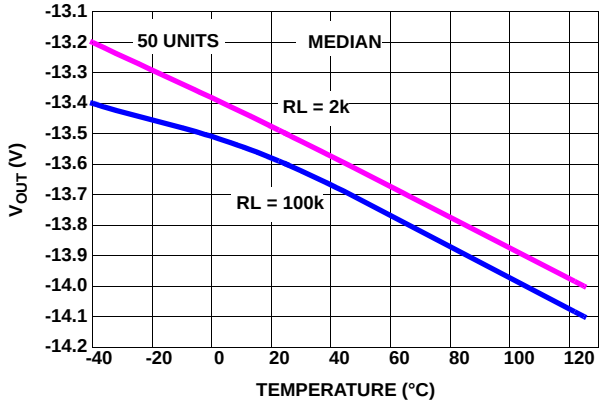


FIGURE 10. V_{OL} vs TEMPERATURE, V_S = ±15V

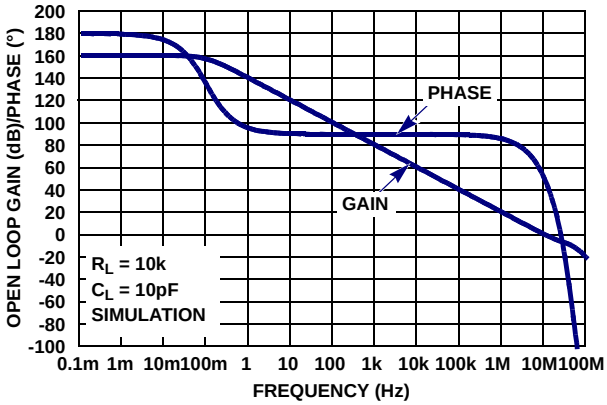


FIGURE 11. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 10pF

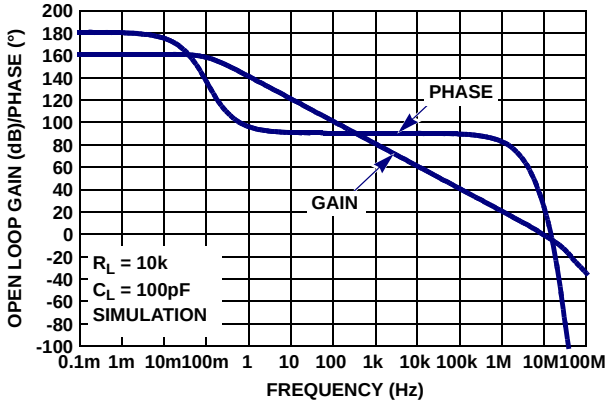


FIGURE 12. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 100pF

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

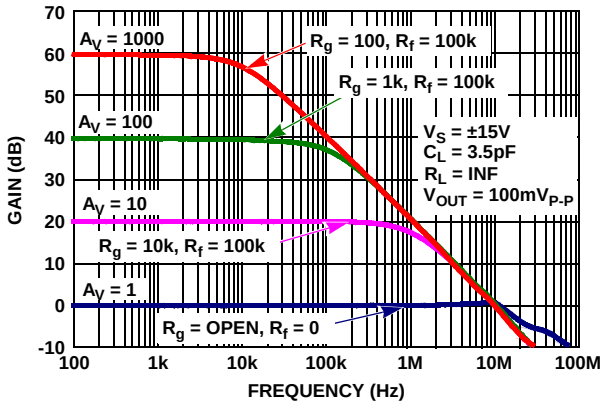


FIGURE 13. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

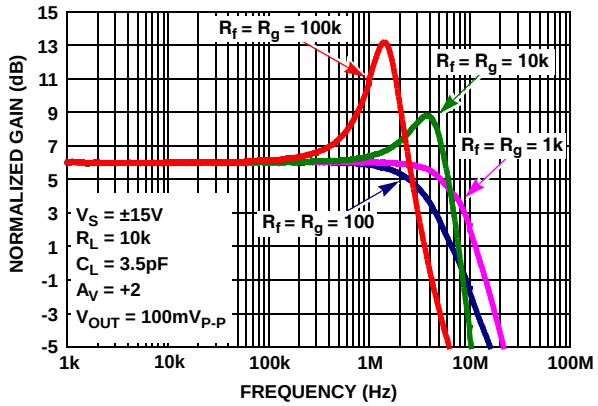


FIGURE 14. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

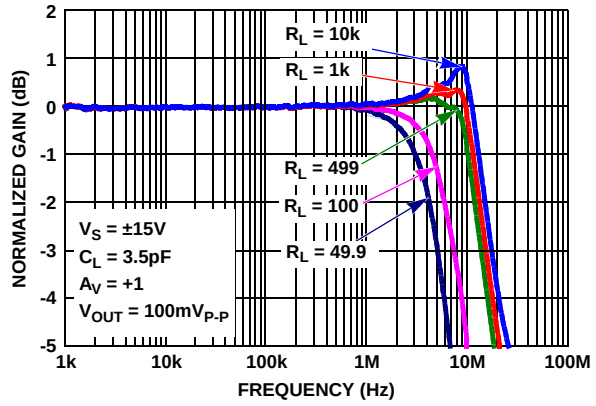


FIGURE 15. GAIN vs FREQUENCY vs R_L

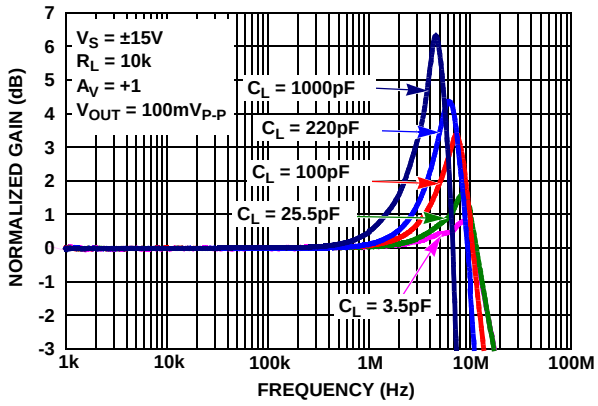


FIGURE 16. GAIN vs FREQUENCY vs C_L

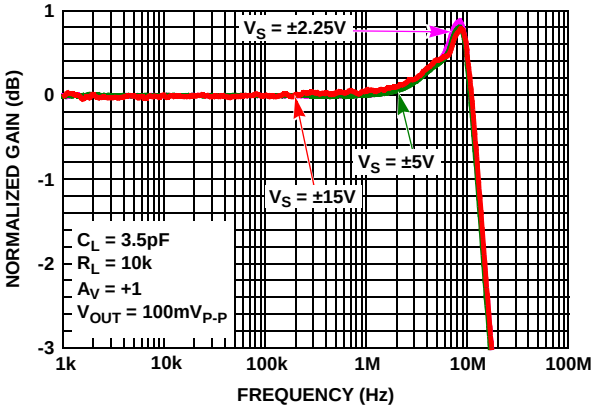


FIGURE 17. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

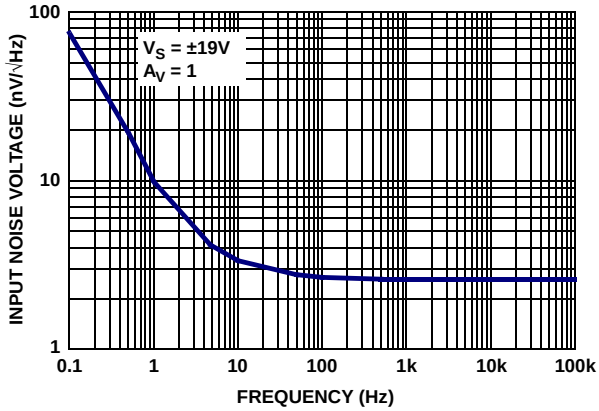


FIGURE 18. INPUT NOISE VOLTAGE SPECTRAL DENSITY

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

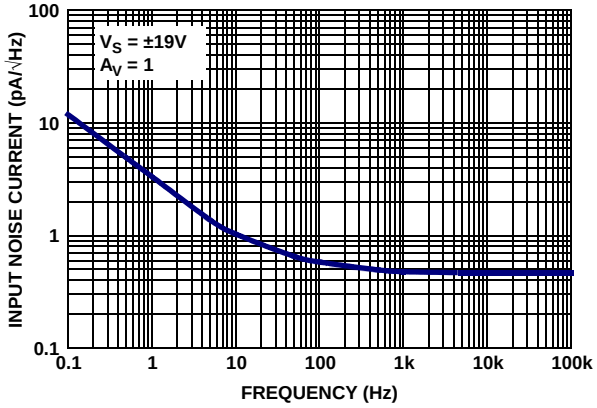


FIGURE 19. INPUT NOISE CURRENT SPECTRAL DENSITY

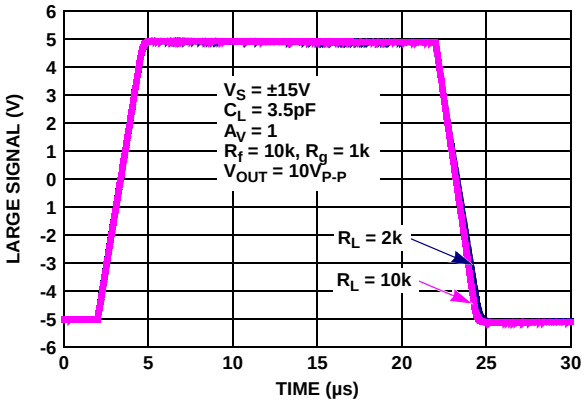


FIGURE 20. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

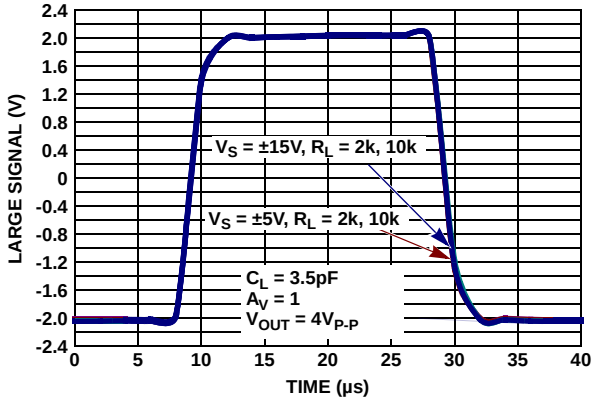


FIGURE 21. LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±5V, ±15V

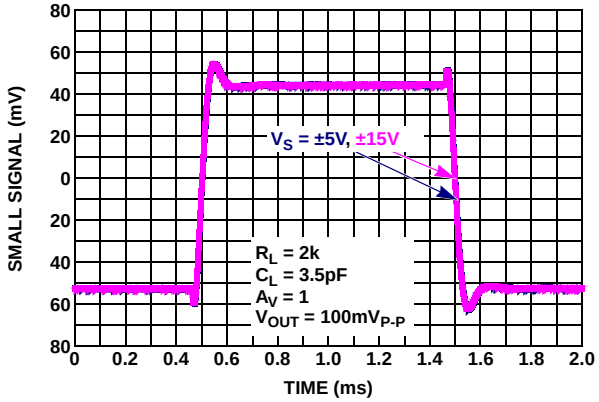


FIGURE 22. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

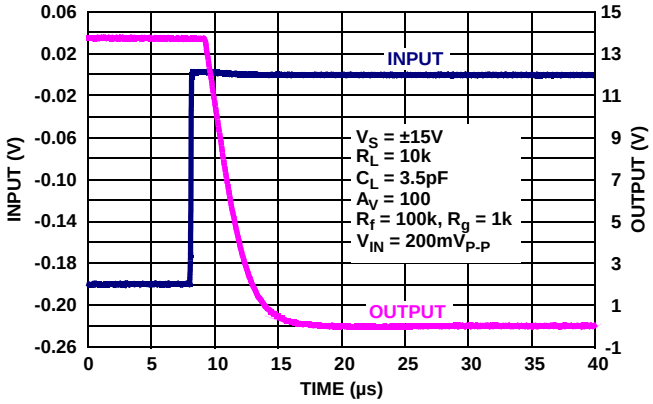


FIGURE 23. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

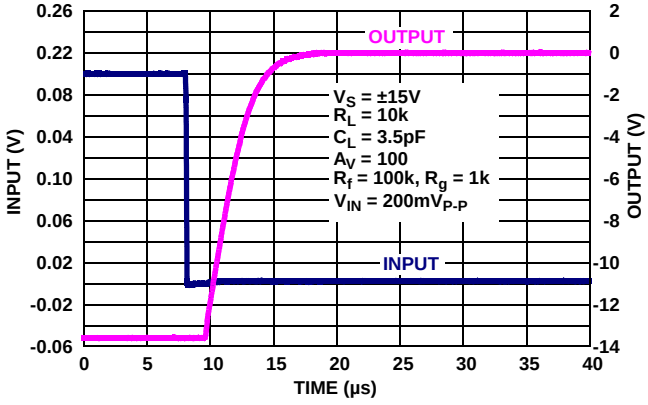


FIGURE 24. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

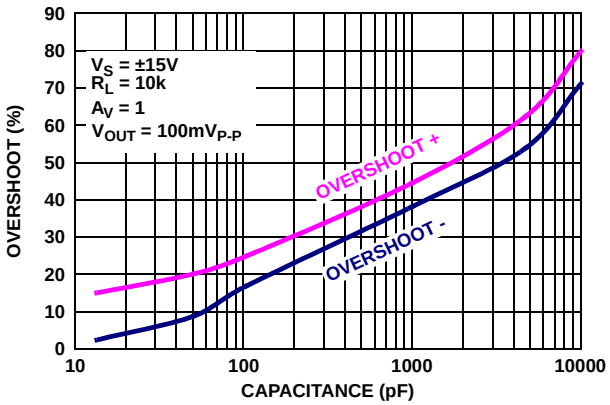
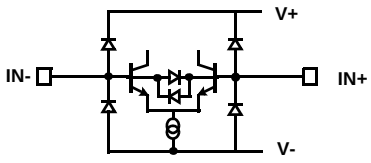


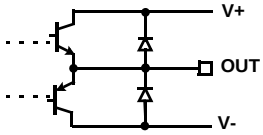
FIGURE 25. % OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V

Pin Descriptions

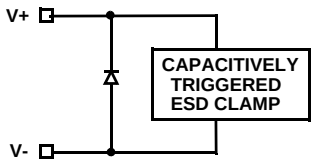
ISL28127 (8 LD SOIC)	ISL28227 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	4	V-	Circuit 3	Negative power supply
	5	+IN_B	Circuit 1	Amplifier B non-inverting input
	6	-IN_B	Circuit 1	Amplifier B inverting input
	7	$V_{OUT}B$	Circuit 2	Amplifier B output
7	8	V+	Circuit 3	Positive power supply
6	1	$V_{OUT}A$	Circuit 2	Amplifier A output
2	2	-IN_A	Circuit 1	Amplifier A inverting input
1, 5, 8		NC	-	No internal connection



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Applications Information

Functional Description

The ISL28127 and ISL28227 are single and dual, low noise 10MHz BW precision op amps. Both devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (1nA typical), low input offset voltage (10µV typ), low input noise voltage (3nV/√Hz), and low 1/f noise corner frequency (3Hz). These amplifiers also feature high open loop gain (1400V/mV) for excellent CMRR (120dB) and THD+N performance (0.0002% @ 3.5V_{RMS}, 1kHz into 2kΩ). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). Parameter variation with operating voltage is shown in the “Typical Performance Curves” beginning on page 5. The input common mode voltage sensitivity to temperature is shown in Figure 19 (±15V). Figure 20 shows VOS as a function of supply voltage and temperature with the common mode voltage at 0V for split supply operation.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, and an additional anti-parallel diode pair across the inputs (Figures 26 and 27).

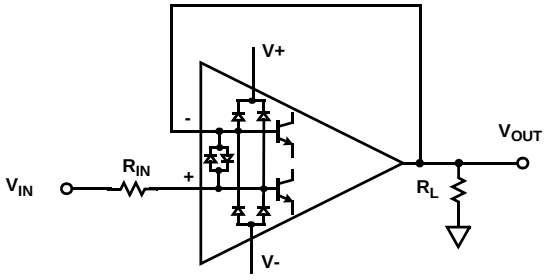


FIGURE 26. INPUT ESD DIODE CURRENT LIMITING - UNITY GAIN

For unity gain applications (Figure 26) where the output is connected directly to the non-inverting input a current limiting resistor (R_{IN}) will be needed under the following conditions to protect the anti-parallel differential input protection diodes.

- The amplifier input is supplied from a low impedance source.
- The input voltage rate-of-rise (dV/dt) exceeds the maximum slew rate of the amplifier (±3.6V/µs).

If the output lags far enough behind the input, the anti-parallel input diodes can conduct. For example, if an input pulse ramps from 0V to +10V in 1µs, then the output of the ISL28x27 will reach only +3.6V (slew rate = 3.6V/µs) while the input is at 10V, The input differential voltage of 6.4V will force input ESD diodes to conduct, dumping the input current directly into the output stage and the load. The resulting current flow can cause permanent damage to the ESD diodes. The ESD diodes are rated to 20mA, and in the previous example, setting R_{IN} to 1k resistor (Figure 26) would limit the current to < 6.4mA, and provide additional protection up to ±20V at the input.

In applications where one or both amplifier input terminals are at risk of exposure to high voltage, current limiting resistors may be needed at each input terminal (see Figure 27 R_{IN}+, R_{IN}-) to limit current through the power supply ESD diodes to 20mA.

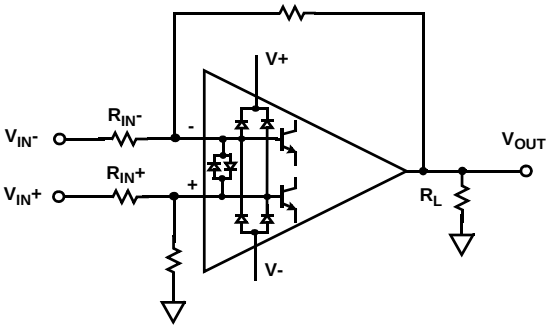


FIGURE 27. INPUT ESD DIODE CURRENT LIMITING - DIFFERENTIAL INPUT

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand an short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28127 and ISL28227 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

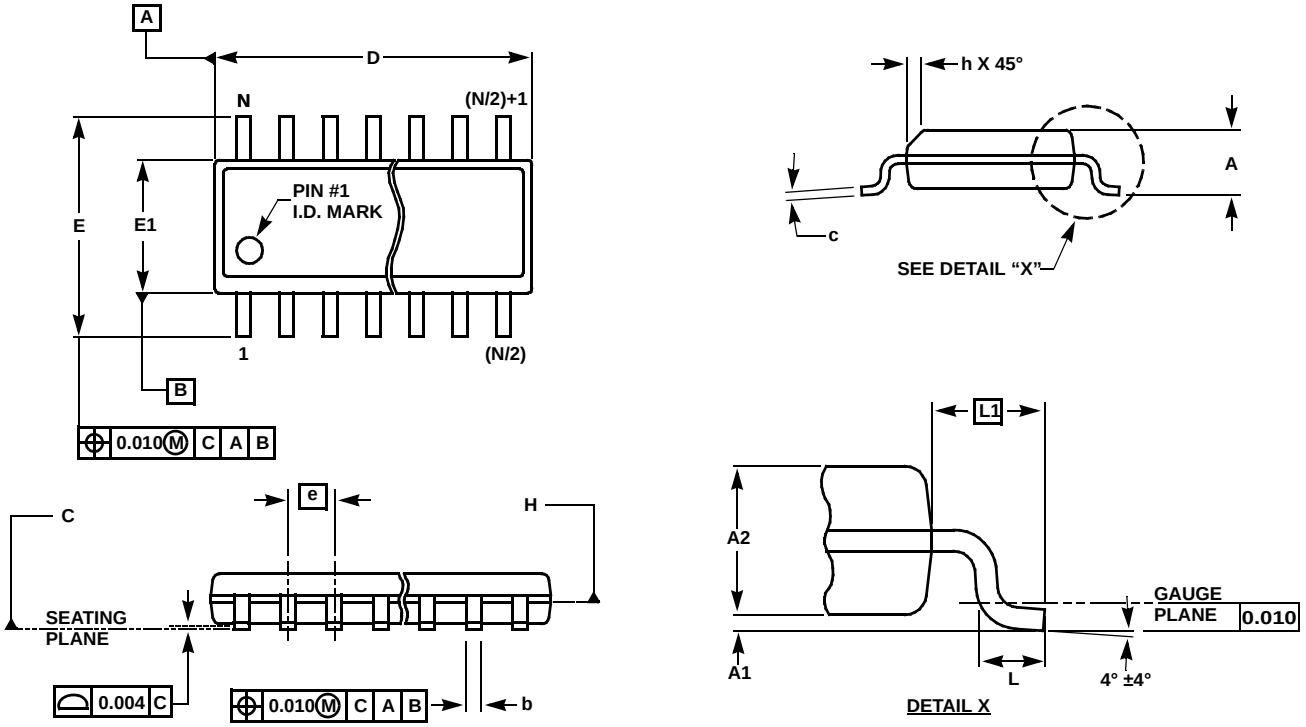
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

R_L = Load resistance

Revision History

DATE	REVISION	CHANGE
5/28/09	FN6633.0	Techdocs Issued File Number FN6633. Initial release of Datasheet with file number FN6633 making this a Rev 0.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994