

NST847BPDP6T5G

Dual Complementary General Purpose Transistor

The NST847BPDP6T5G device is a spin-off of our popular SOT-23/SOT-323/SOT-563 three-leaded device. It is designed for general purpose amplifier applications and is housed in the SOT-963 six-leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low-power surface mount applications where board space is at a premium.

Features

- h_{FE} , 200–450
- Low $V_{CE(sat)}$, ≤ 0.3 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- This is a Pb-Free Device

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	45	Vdc
Collector – Base Voltage	V_{CBO}	50	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	100	mAdc
Electrostatic Discharge	HBM MM	ESD Class 2 B	

THERMAL CHARACTERISTICS

Characteristic (Single Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 1)	P_D	240 1.9	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	520	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 2)	P_D	280 2.2	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	446	$^\circ\text{C}/\text{W}$
Characteristic (Dual Heated) (Note 3)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 1)	P_D	350 2.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	357	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 2)	P_D	420 3.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	297	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

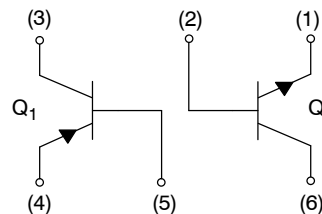
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-4 @ 100 mm², 1 oz. copper traces, still air.
2. FR-4 @ 500 mm², 1 oz. copper traces, still air.
3. Dual heated values assume total power is sum of two equally powered channels



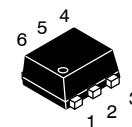
ON Semiconductor[®]

<http://onsemi.com>



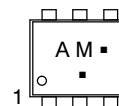
NST847BPDP6T5G*

*Q1 PNP
Q2 NPN



**SOT-963
CASE 527AD
PLASTIC**

MARKING DIAGRAM



A = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NST847BPDP6T5G	SOT-963 (Pb-Free)	8000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NST847BPDP6T5G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I _C = 1.0 mA, I _B = 0) (I _C = -1.0 mA, I _B = 0)	(NPN) (PNP)	V _{(BR)CEO}	45 -45	- -	V
Collector–Base Breakdown Voltage (I _C = 10 μA, I _E = 0) (I _C = -10 μA, I _E = 0)	(NPN) (PNP)	V _{(BR)CBO}	50 -50	- -	V
Collector–Emitter Breakdown Voltage (I _C = 10 μA) (I _C = -10 μA)	(NPN) (PNP)	V _{(BR)CES}	50 -50	- -	V
Emitter–Base Breakdown Voltage (I _E = 1.0 μA, I _C = 0) (I _E = -1.0 μA, I _C = 0)	(NPN) (PNP)	V _{(BR)EBO}	6.0 -5.0	- -	V
Collector Cutoff Current (V _{CB} = 30 V) (V _{CB} = 30 V, T _A = 150°C) (V _{CB} = -30 V) (V _{CB} = -30 V, T _A = 150°C)	(NPN) (NPN) (PNP) (PNP)	I _{CBO}	- - - -	- - - -	nA μA nA μA

ON CHARACTERISTICS (Note 4)

DC Current Gain (I _C = 2.0 mA, V _{CE} = 5.0 V) (I _C = -2.0 mA, V _{CE} = -5.0 V)	(NPN) (PNP)	h _{FE}	200 220	290 290	450 475	-
Collector–Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.5 mA) (I _C = 100 mA, I _B = 5.0 mA) (I _C = -10 mA, I _B = -0.5 mA) (I _C = -100 mA, I _B = -5.0 mA)	(NPN) (PNP)	V _{CE(sat)}	- -	- -	0.25 0.60 -0.30 -0.70	V
Base–Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.5 mA) (I _C = 100 mA, I _B = 5.0 mA) (I _C = -10 mA, I _B = -0.5 mA) (I _C = -100 mA, I _B = -5.0 mA)	(NPN) (PNP)	V _{BE(sat)}	- -	0.70 0.90 -0.70 -0.90	- -	V
Base–Emitter On Voltage (I _C = 2.0 mA, V _{CE} = 5.0 V) (I _C = 10 mA, V _{CE} = 5.0 V) (I _C = -2.0 mA, V _{CE} = -5.0 V) (I _C = -10 mA, V _{CE} = -5.0 V)	(NPN) (PNP)	V _{BE(on)}	0.58 - -0.60 -	0.66 - -	0.70 0.77 -0.75 -0.82	V

SMALL-SIGNAL CHARACTERISTICS

Current–Gain – Bandwidth Product (I _C = 10 mA, V _{CE} = 5.0 V, f = 100 MHz) (I _C = -10 mA, V _{CE} = -5.0 V, f = 100 MHz)	(NPN) (PNP)	f _T	100 100	- -	- -	MHz
Output Capacitance (V _{CB} = 10 V, f = 1.0 MHz) (V _{CB} = -10 V, f = 1.0 MHz)	(NPN) (PNP)	C _{ob}	- -	- -	4.5 4.5	pF
Noise Figure (I _C = 0.2 mA, V _{CE} = 5.0 V, R _S = 2 kΩ, f = 1 kHz, BW = 200 Hz) (I _C = -0.2 mA, V _{CE} = -5.0 V, R _S = 2 kΩ, f = 1 kHz, BW = 200 Hz)	(NPN) (PNP)	NF	- -	- -	10 10	dB

4. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

NST847BPDP6T5G

NPN TRANSISTOR

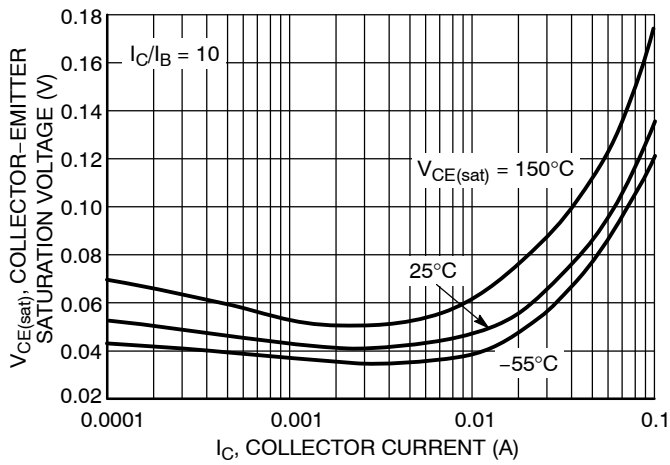


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

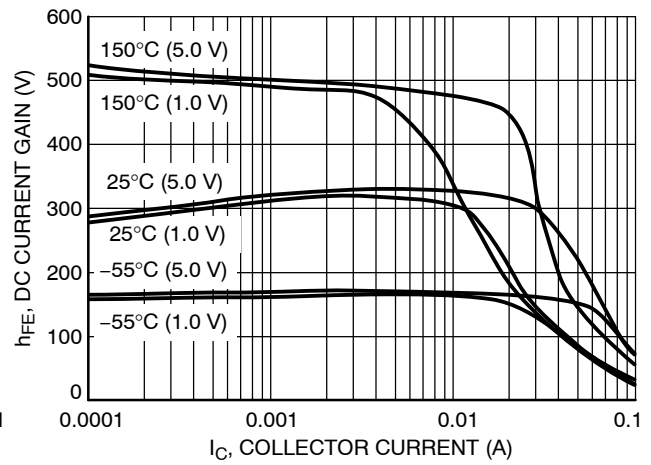


Figure 2. DC Current Gain vs. Collector Current

NST847BPDP6T5G

NPN TRANSISTOR

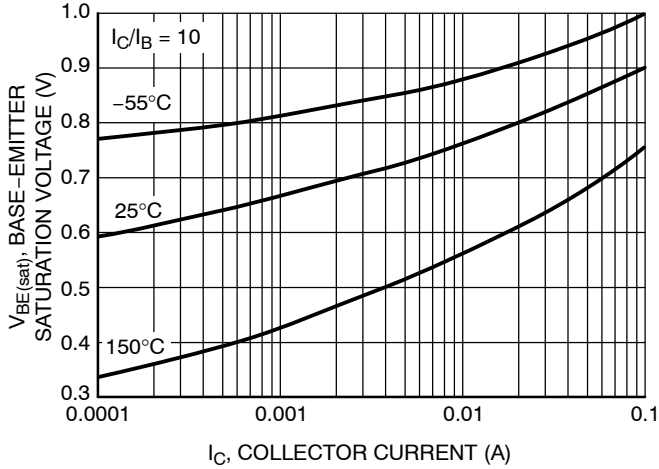


Figure 3. Base Emitter Saturation Voltage vs. Collector Current

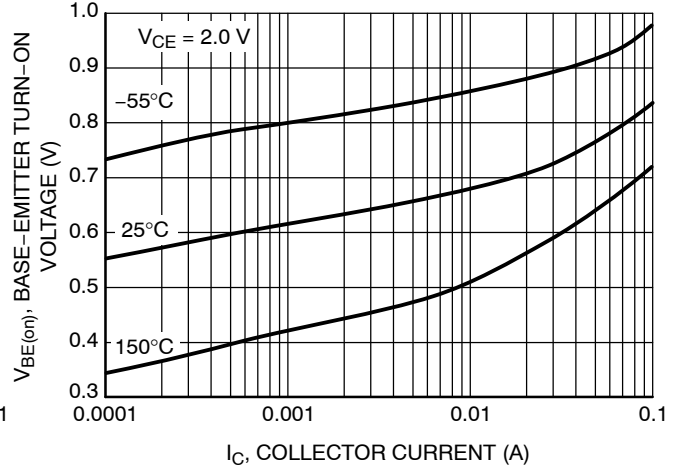


Figure 4. Base Emitter Turn-On Voltage vs. Collector Current

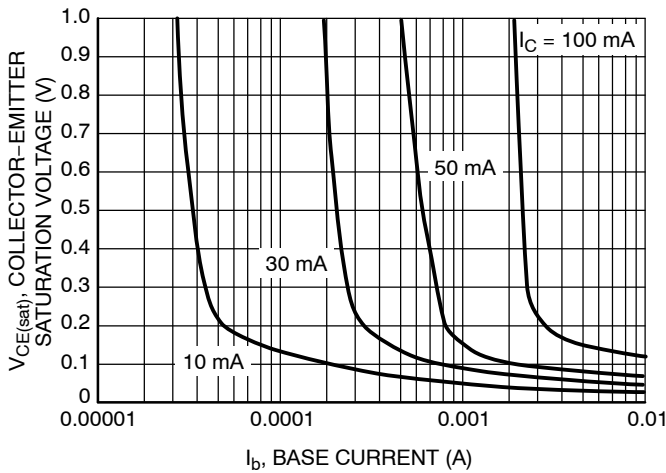


Figure 5. Saturation Region

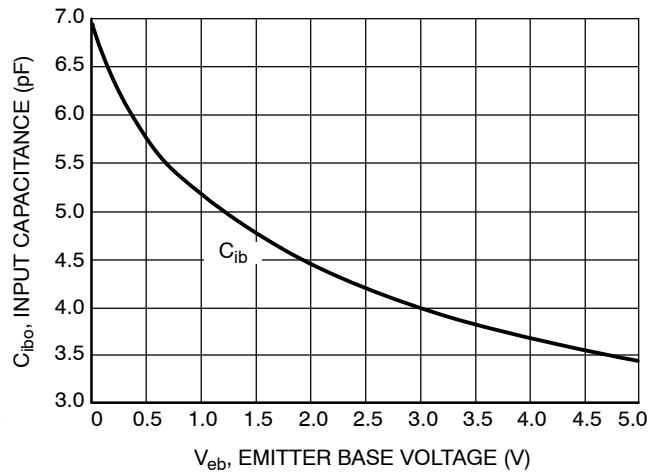


Figure 6. Input Capacitance

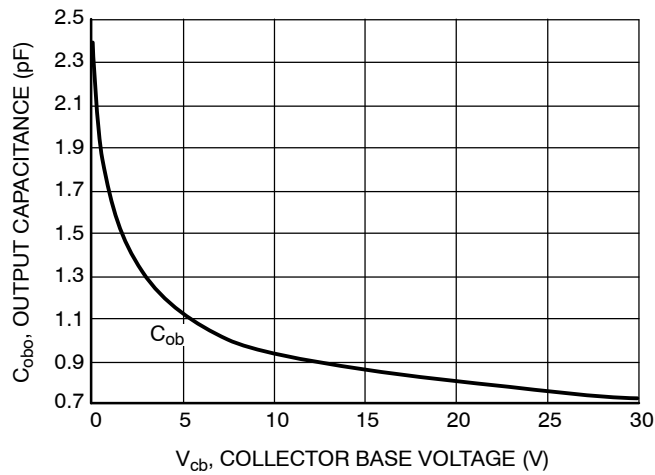


Figure 7. Output Capacitance

NST847BPDP6T5G

PNP TRANSISTOR

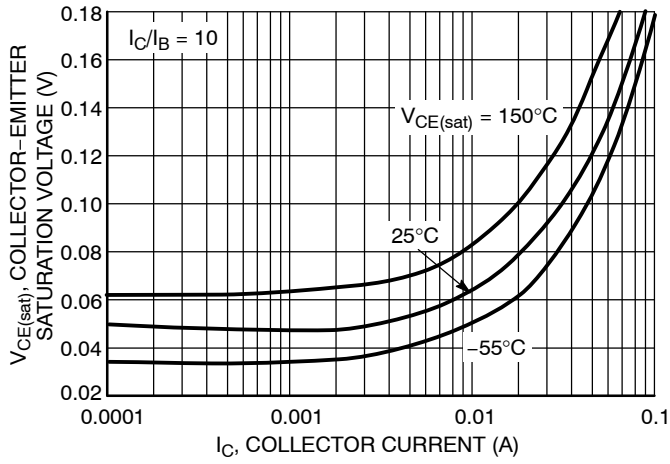


Figure 8. Collector Emitter Saturation Voltage vs. Collector Current

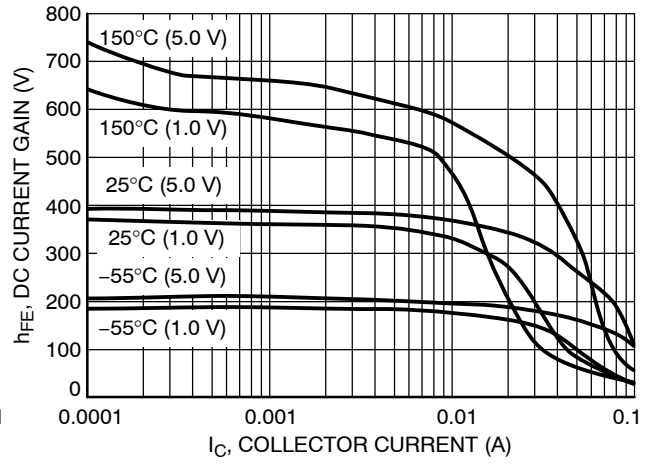


Figure 9. DC Current Gain vs. Collector Current

NST847BPDP6T5G

PNP TRANSISTOR

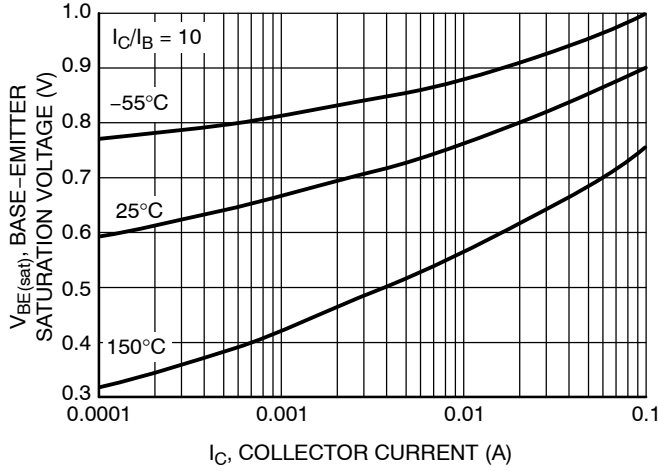


Figure 10. Base Emitter Saturation Voltage vs. Collector Current

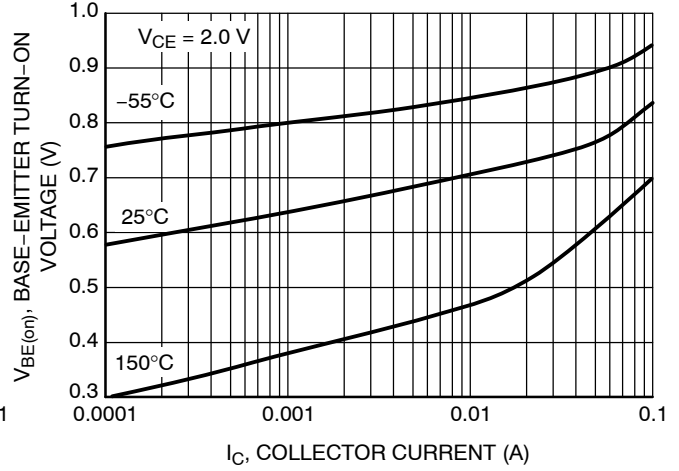


Figure 11. Base Emitter Turn-On Voltage vs. Collector Current

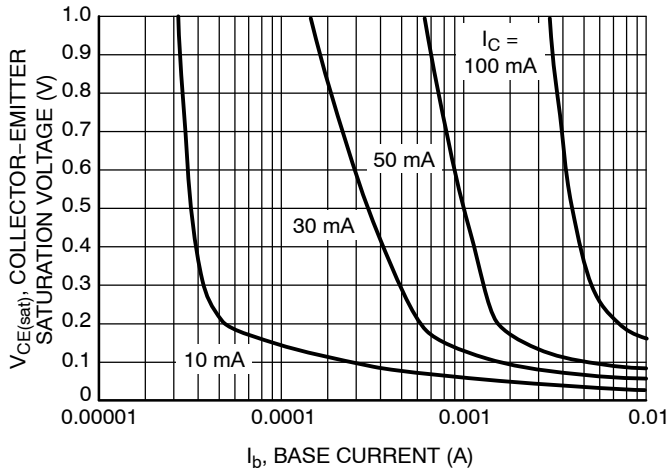


Figure 12. Saturation Region

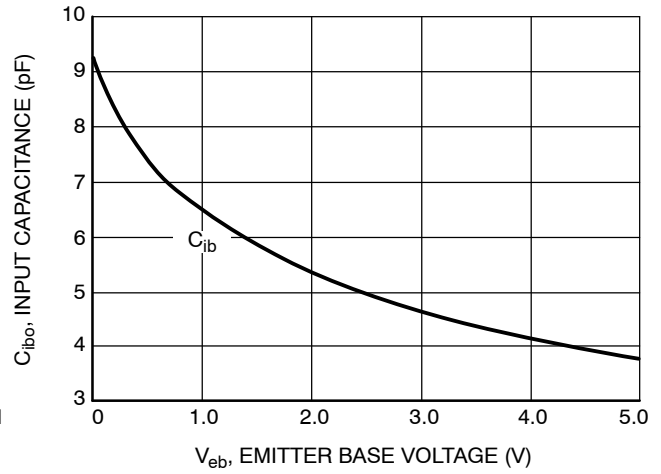


Figure 13. Input Capacitance

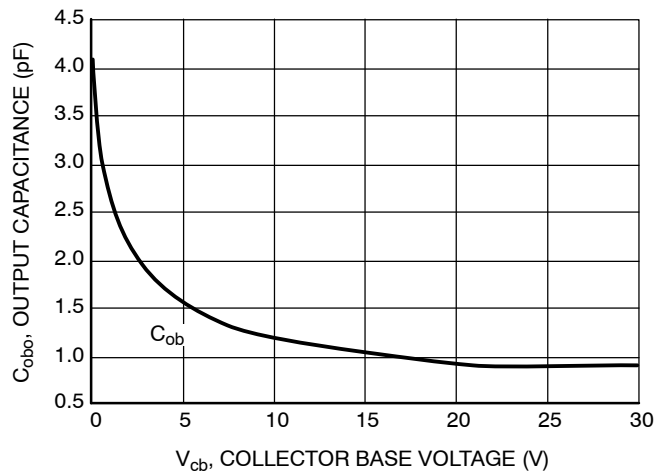
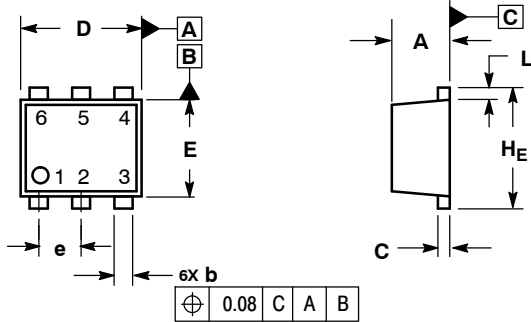


Figure 14. Output Capacitance

NST847BPDP6T5G

PACKAGE DIMENSIONS

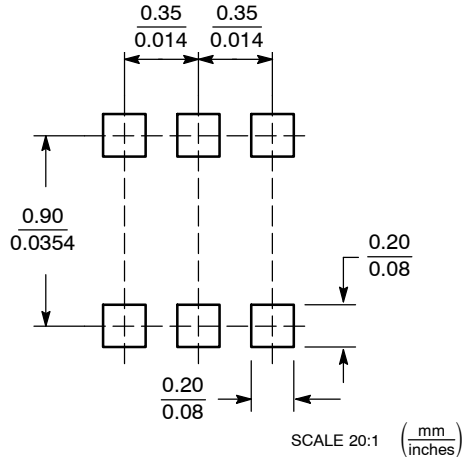
SOT-963
CASE 527AD-01
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40			
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.07	0.12	0.17	0.003	0.005	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
HE	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative