



# RF Power Field Effect Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

RF Power transistor designed for applications operating at frequencies between 1030 and 1090 MHz, 1% to 20% duty cycle. This device is suitable for use in pulsed applications.

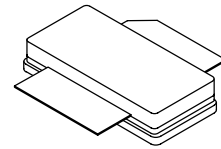
- Typical Pulsed Performance:  $V_{DD} = 50$  Volts,  $I_{DQ} = 250$  mA,  
 $P_{out} = 250$  Watts Peak,  $f = 1090$  MHz, Pulse Width = 100  $\mu$ sec,  
 Duty Cycle = 10%  
     Power Gain — 21 dB  
     Drain Efficiency — 60%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 1090 MHz, 250 Watts Peak Power

### Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 50  $V_{DD}$  Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRF6V10250HSR3**

**1090 MHz, 250 W, 50 V  
 PULSED  
 LATERAL N-CHANNEL  
 RF POWER MOSFET**



**CASE 465A-06, STYLE 1  
 NI-780S**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +100	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Storage Temperature Range	$T_{stg}$	- 65 to +150	$^{\circ}$ C
Case Operating Temperature	$T_C$	150	$^{\circ}$ C
Operating Junction Temperature	$T_J$	200	$^{\circ}$ C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 79 $^{\circ}$ C, 250 W Pulsed, 100 $\mu$ sec Pulse Width, 10% Duty Cycle	$R_{\theta JC}$	0.10	$^{\circ}$ C/W

1. MTTF calculator available at <http://www.freescale.com/rtf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rtf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	500	nAdc
Drain-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 100\text{ mA}$ )	$V_{(BR)DSS}$	100	—	—	Vdc
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 50\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	50	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 90\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	2	mA

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 528\text{ }\mu\text{Adc}$ )	$V_{GS(th)}$	1	1.8	3	Vdc
Gate Quiescent Voltage ( $V_{DD} = 50\text{ Vdc}$ , $I_D = 250\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	2	2.4	3	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.32\text{ Adc}$ )	$V_{DS(on)}$	—	0.25	—	Vdc

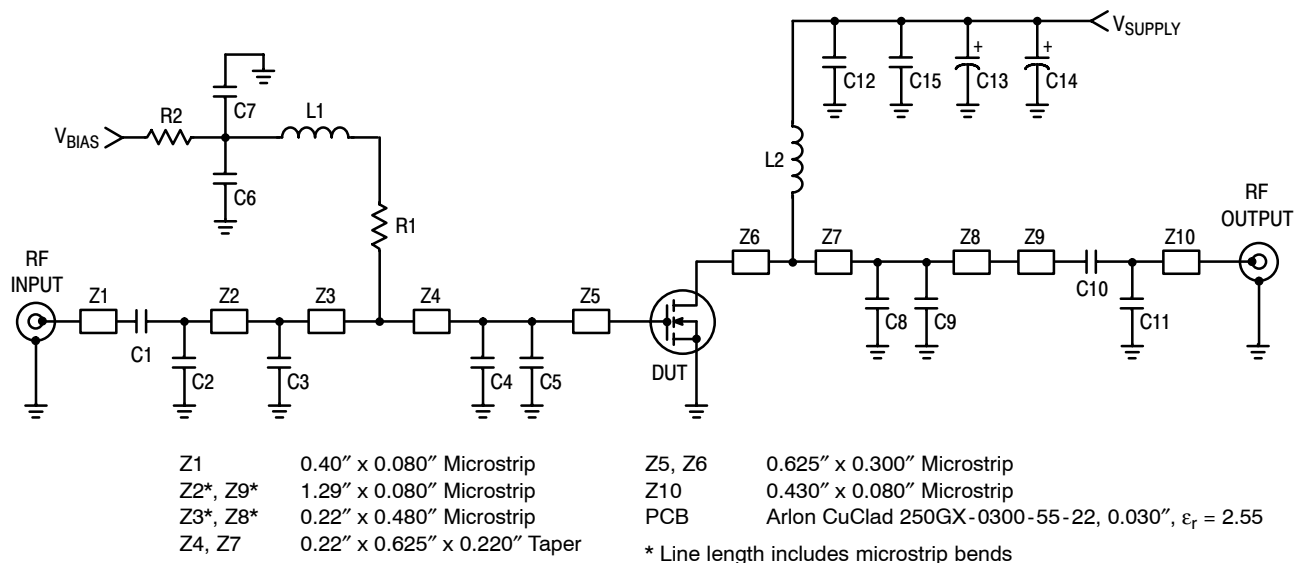
**Dynamic Characteristics** <sup>(1)</sup>

Reverse Transfer Capacitance ( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	0.8	—	pF
Output Capacitance ( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	340	—	pF
Input Capacitance ( $V_{DS} = 50\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	$C_{iss}$	—	280	—	pF

**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 50\text{ Vdc}$ ,  $I_{DQ} = 250\text{ mA}$ ,  $P_{out} = 250\text{ W Peak}$  (25 W Avg.),  $f = 1090\text{ MHz}$ , Pulsed, 100  $\mu\text{sec}$  Pulse Width, 10% Duty Cycle

Power Gain	$G_{ps}$	19	21	23	dB
Drain Efficiency	$\eta_D$	55	60	—	%
Input Return Loss	IRL	—	-12	-9	dB

1. Part internally matched both on input and output.



**Figure 1. MRF6V1025HSR3 Test Circuit Schematic**

**Table 5. MRF6V1025HSR3 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1	240 pF Chip Capacitor	ATC100B241JT500XT	ATC
C2, C9, C11	1.8 pF Chip Capacitors	ATC100B1R8CT500XT	ATC
C3	3.3 pF Chip Capacitor	ATC100B3R3CT500XT	ATC
C4, C5	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C6, C10, C12	39 pF Chip Capacitors	ATC100B390JT500XT	ATC
C7, C15	2.2 $\mu$ F, 50 V Chip Capacitors	C1825C225J5RAC	Kemet
C8	4.7 pF Chip Capacitor	ATC100B4R7CT500XT	ATC
C13, C14	470 $\mu$ F, 63 V Electrolytic Capacitors	EKME633ELL471MK25S	Multicomp
L1	5 nH, 2 Turn Inductor	A02TKLC	Coilcraft
L2	7 nH, Hand Wound	2T, 18awg	Freescale
R1	10 $\Omega$ , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
R2	20 $\Omega$ , 1 W Chip Resistor	CRCW251220R0FKEA	Vishay

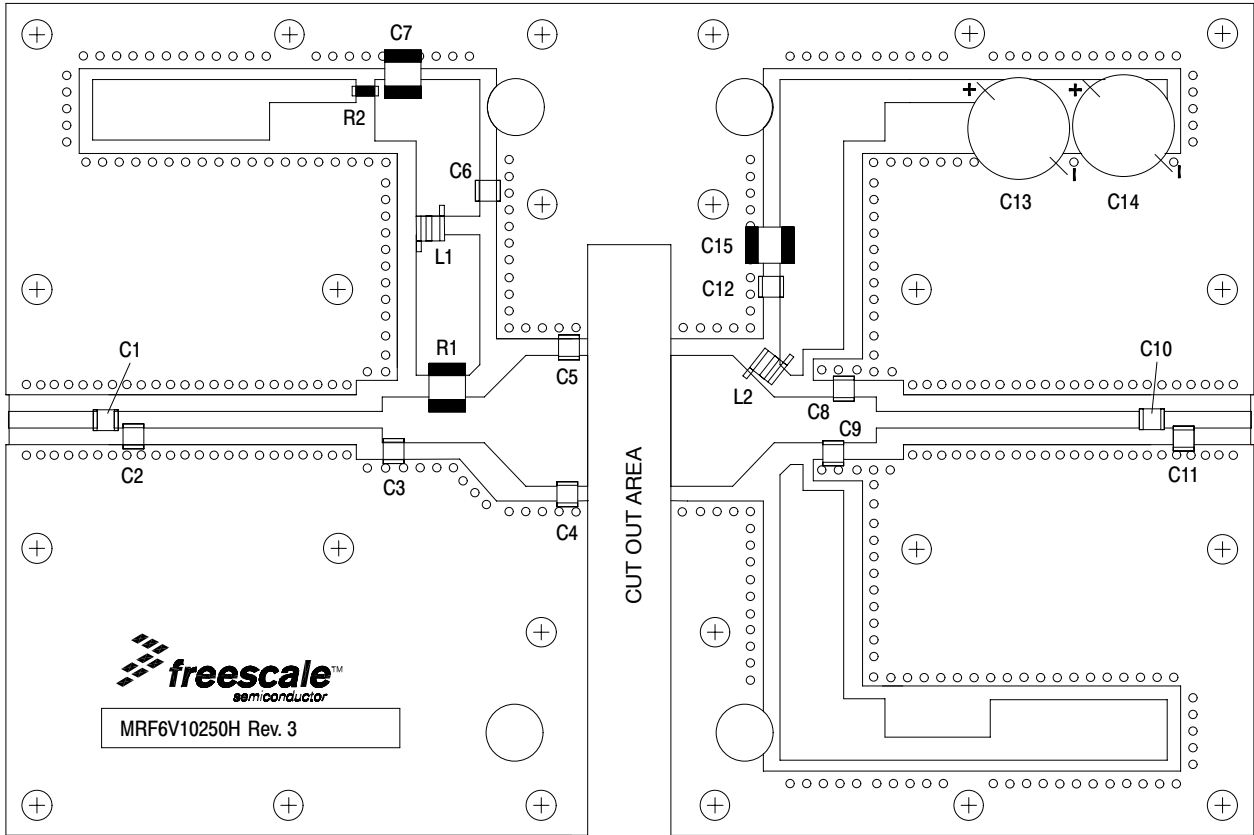
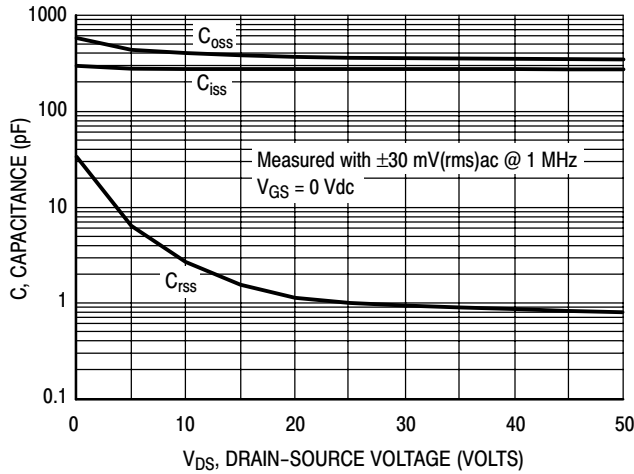
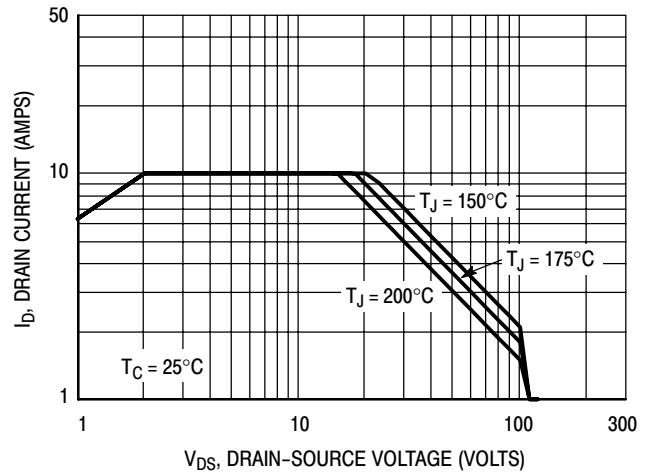


Figure 2. MRF6V10250HSR3 Test Circuit Component Layout

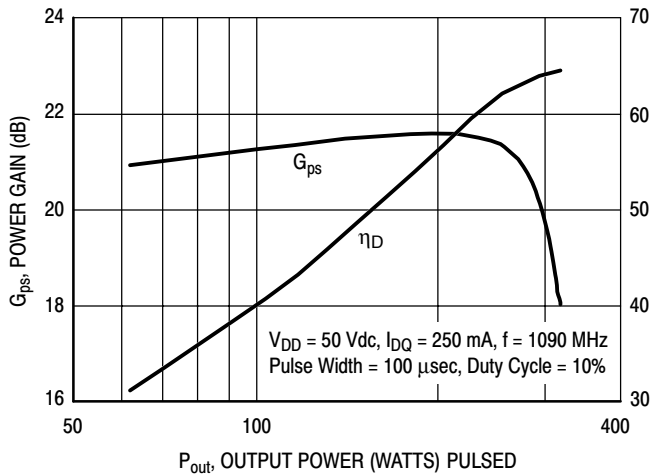
## TYPICAL CHARACTERISTICS



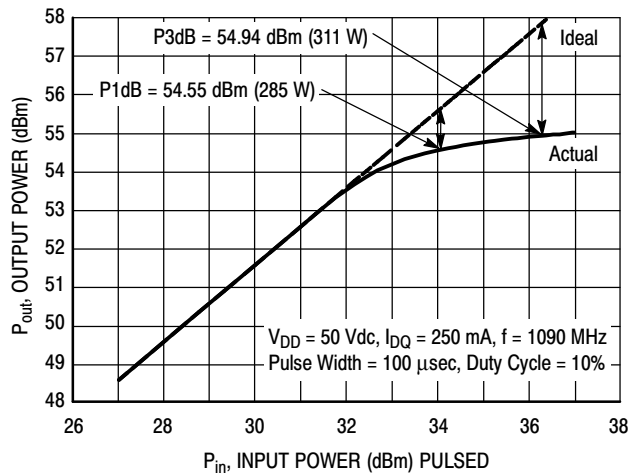
**Figure 3. Capacitance versus Drain-Source Voltage**



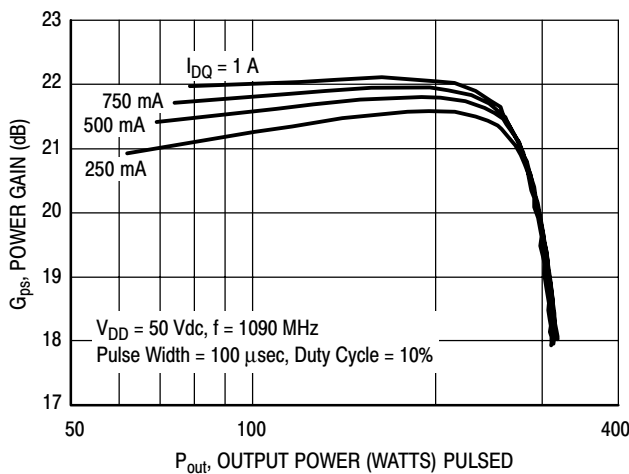
**Figure 4. DC Safe Operating Area**



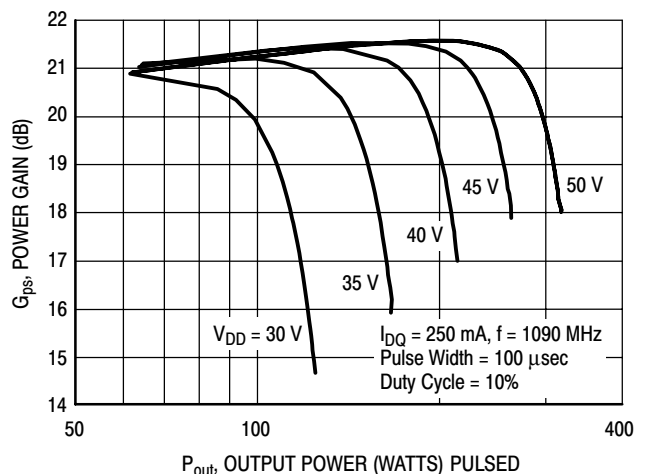
**Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power**



**Figure 6. Pulsed Output Power versus Input Power**

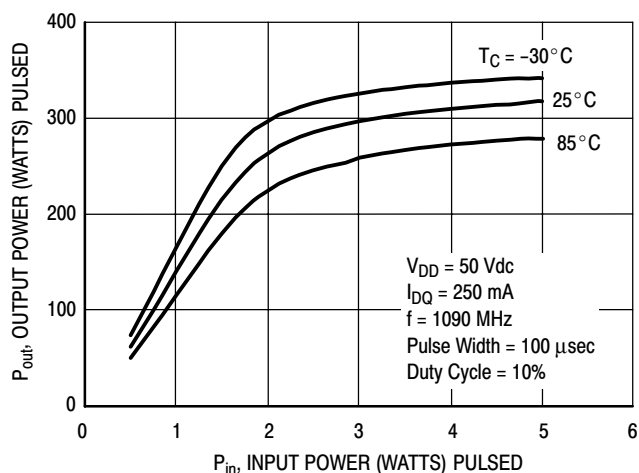


**Figure 7. Pulsed Power Gain versus Output Power**

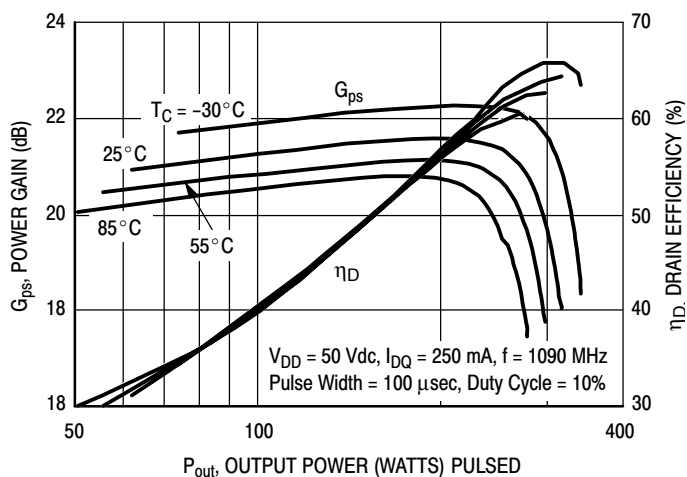


**Figure 8. Pulsed Power Gain versus Output Power**

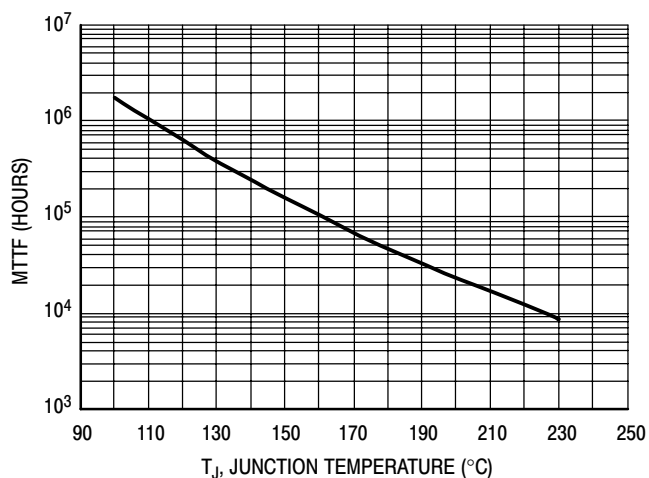
## TYPICAL CHARACTERISTICS



**Figure 9. Pulsed Power Output versus Power Input**



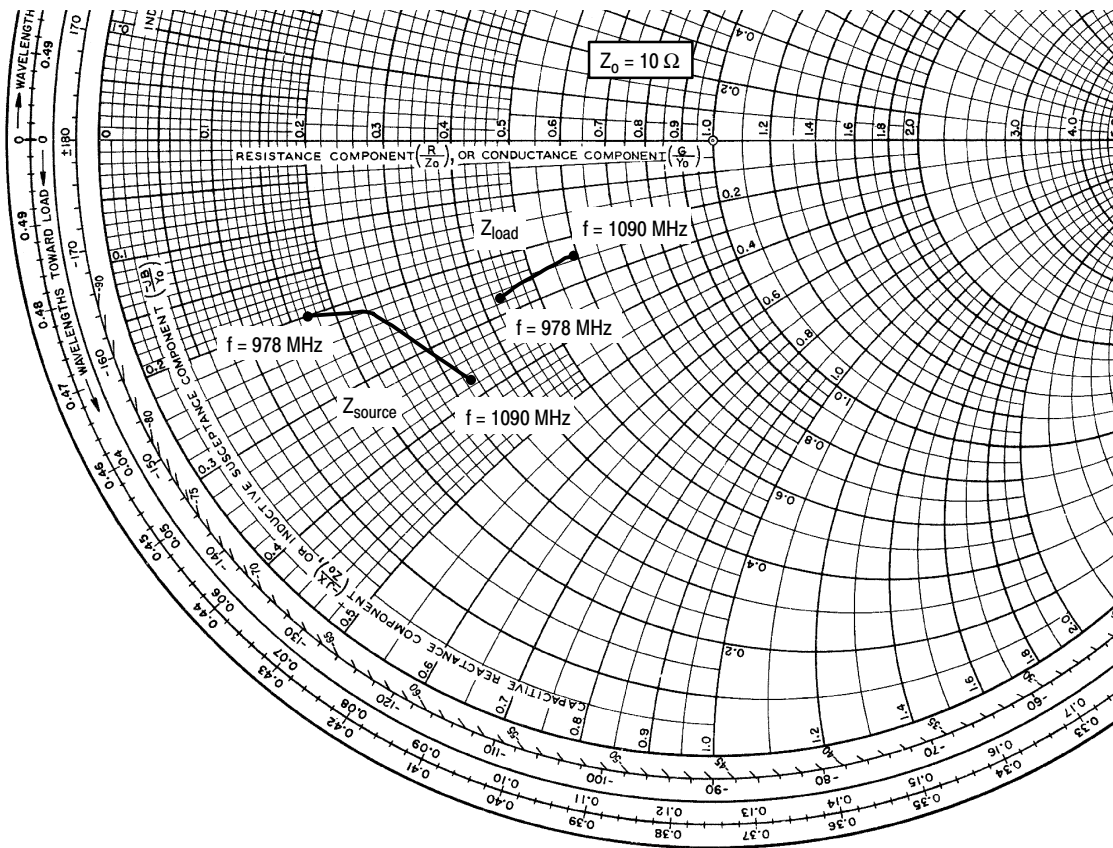
**Figure 10. Pulsed Power Gain and Drain Efficiency versus Output Power**



This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 50$  Vdc,  $P_{out} = 250$  W Peak, Pulse Width = 100  $\mu$ sec, Duty Cycle = 10%, and  $\eta_D = 60\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 11. MTTF versus Junction Temperature**



$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ} = 250 \text{ mA}$ ,  $P_{out} = 250 \text{ W Peak}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
978	$1.67 - j2.04$	$4.3 - j2.72$
1030	$2.39 - j2.23$	$5.66 - j2.42$
1090	$3.26 - j3.72$	$5.85 - j2.39$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

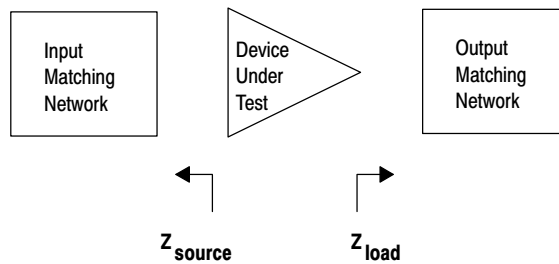
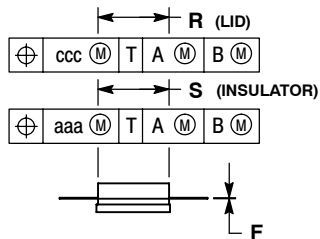
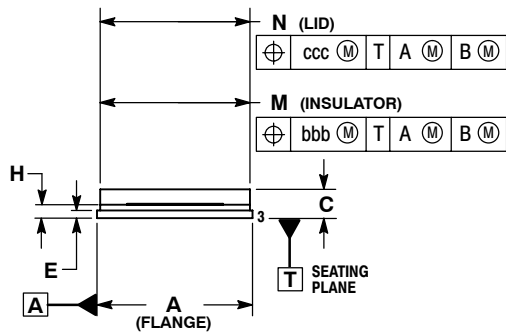
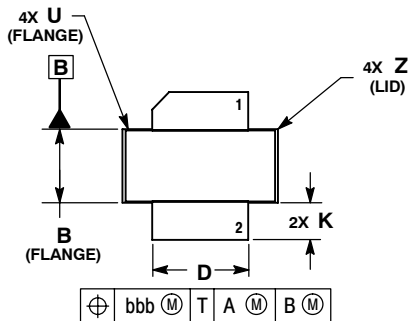


Figure 12. Series Equivalent Source and Load Impedance

# PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DELETED
  4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
1. DRAIN
  2. GATE
  5. SOURCE

CASE 465A-06  
 ISSUE H  
 NI-780S



## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2008	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

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