



# TDA19978B

Quad HDMI 1.3a receiver interface with equalizer (HDTV up to 1080p, up to UXGA for PC formats)

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Product data sheet

## HDMI

### 1. General description

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The TDA19978B is a four input HDMI 1.3a compliant receiver with embedded EDID memory. The built-in auto-adaptive equalizer improves signal quality and allows the use of cable lengths up to 25 m which are laboratory tested with a 0.5 mm (24 AWG) cable at 2.05 gigasamples per second. In addition, the TDA19978B is delivered with software drivers to ease configuration and use.

The TDA19978B supports:

- TV resolutions:
  - 480i (1440 × 480i at 60 Hz), 576i (1440 × 576i at 50 Hz) to HDTV (up to 1920 × 1080p at 50/60 Hz)
  - WUXGA (1920 × 1200p at 60 Hz) reduced blanking format
- PC resolutions:
  - VGA (640 × 480p at 60 Hz) to UXGA (1600 × 1200p at 60 Hz)
- Deep Color mode in 10-bit and 12-bit (up to 205 MHz TMDS clock)
- Gamut boundary description
- IEC 60958/IEC 61937, OBA (One Bit Audio), DST (Direct Stream Transfer) and HBR (High Bit Rate) stream

The TDA19978B includes:

- An enhanced PC and TV format recognition system
- Generation of a  $128/256/512 \times f_s$  system clock allowing the use of simple audio DACs without an integrated PLL (such as the UDA1334BTS)
- An embedded oscillator (an external crystal can also be used)
- Improved audio clock generation using an external reference clock
- OBA (as used in SACD), DST and HBR stream support

The TDA19978B converts HDMI streams without HDCP into RGB or YCbCr digital signals. The YCbCr digital output signal can be 4:4:4 or 4:2:2 semi-planar format based on the ITU-R BT.601 standard or 4:2:2 based on the ITU-R BT.656 format. The device can adjust the output timing of the video port by altering the values of  $t_{su(Q)}$  and  $t_{h(Q)}$ . In addition, all settings are controllable using the I<sup>2</sup>C-bus.



## 2. Features and benefits

- Complies with the HDMI 1.3a, DVI 1.0 and CEA-861-D
- Four (quad) independent HDMI inputs, up to the HDMI frequency of 205 MHz
- Embedded auto-adaptive equalizer on all HDMI links
- EDID memory: 253 shared bytes and three bytes dedicated to each HDMI input
- Supports color depth processing (8-bit, 10-bit or 12-bit per color)
- Color gamut metadata packet with interrupt on each update, readable via the I<sup>2</sup>C-bus
- Up to four S/PDIF or I<sup>2</sup>S-bus outputs (eight channels) at a sampling rate up to 192 kHz with IEC 60958/IEC 61937 stream
- HBR audio stream up to 768 kHz with four demultiplexed S/PDIF or I<sup>2</sup>S-bus outputs
- HBR streams (e.g. DTS-HD master audio and Dolby TrueHD up to eight channels due to HBR packet for stream with a frame rate up to 768 kHz) support
- DSD and DST audio stream up to six DSD channels output for SACD with DST audio packet support
- Channel status decoder supports multi-channel reception
- Improved audio clock generation using an external reference clock
- System/master clock output ( $128/256/512 \times f_s$ ) enables the use of the UDA1334BTS
- The HDMI interface supports:
  - ◆ All HDTV formats up to  $1920 \times 1080p$  at 50/60 Hz and WUXGA ( $1920 \times 1200p$  at 60 Hz) with support for reduced blanking
  - ◆ PC formats up to UXGA ( $1600 \times 1200p$  at 60 Hz)
- Embedded oscillator (an external crystal can be used)
- Frame and field detection for interlaced video signal
- Sync timing measurements for format recognition
- Improved system for measurements of blanking and video active area allowing an accurate recognition of PC and TV formats
- Repeater capability
- Programmable color space input signal conversion from RGB-to-YCbCr or YCbCr-to-RGB
- Output formats: RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2 semi-planar based on the ITU-R BT.601 standard and YCbCr 4:2:2 ITU-R BT.656
- 8-bit, 10-bit or 12-bit output formats selectable using the I<sup>2</sup>C-bus (8-bit and 10-bit only in 4:4:4 format)
- I<sup>2</sup>C-bus adjustable timing of video port ( $t_{su(Q)}$  and  $t_{h(Q)}$ )
- Downsampling-by-two with selectable filters on Cb and Cr channels in 4:2:2 mode
- Internal video and audio pattern generator
- Controllable using the I<sup>2</sup>C-bus; 5 V tolerant and bit rate up to 400 kbit/s
- DDC-bus inputs 5 V tolerant and bit rate up to 400 kbit/s
- LV-TTL outputs
- Power-down mode
- CMOS process
- 1.8 V and 3.3 V power supplies
- Lead-free (Pb) HLQFP144 package

### 3. Applications

- HDTV
- YCbCr or RGB high-speed video digitizer
- Projector, plasma and LCD TV
- Rear projection TV
- High-end TV
- Home theater amplifier
- DVD recorder
- AVR and HDMI splitter

### 4. Quick reference data

Table 1. Quick reference data

| Symbol                                                 | Parameter                     | Conditions                                     | Min   | Typ  | Max   | Unit |
|--------------------------------------------------------|-------------------------------|------------------------------------------------|-------|------|-------|------|
| <b>Digital inputs: pins RXxC+, RXxC-[1]</b>            |                               |                                                |       |      |       |      |
| f <sub>clk(max)</sub>                                  | maximum clock frequency       |                                                | 205   | -    | -     | MHz  |
| <b>Clock timing output: pins VCLK, ACLK and SYSCLK</b> |                               |                                                |       |      |       |      |
| f <sub>clk(max)</sub>                                  | maximum clock frequency       | pin VCLK                                       | 165   | -    | -     | MHz  |
|                                                        |                               | pin ACLK                                       | 25    | -    | -     | MHz  |
|                                                        |                               | pin SYSCLK                                     | 50    | -    | -     | MHz  |
| <b>Supplies</b>                                        |                               |                                                |       |      |       |      |
| V <sub>DDH(3V3)</sub>                                  | HDMI supply voltage (3.3 V)   |                                                | 3.135 | 3.3  | 3.465 | V    |
| V <sub>DDH(1V8)</sub>                                  | HDMI supply voltage (1.8 V)   |                                                | 1.71  | 1.8  | 1.89  | V    |
| V <sub>DDI(3V3)</sub>                                  | input supply voltage (3.3 V)  |                                                | 3.135 | 3.3  | 3.465 | V    |
| V <sub>DDC(1V8)</sub>                                  | core supply voltage (1.8 V)   |                                                | 1.71  | 1.8  | 1.89  | V    |
| V <sub>DDO(3V3)</sub>                                  | output supply voltage (3.3 V) |                                                | 3.135 | 3.3  | 3.465 | V    |
| P                                                      | power dissipation             | Active mode [2]                                |       |      |       |      |
|                                                        |                               | 720p at 60 Hz                                  | -     | 0.75 | -     | W    |
|                                                        |                               | 1080p at 60 Hz                                 | -     | 1.13 | -     | W    |
|                                                        |                               | 1080p at 60 Hz; Deep Color mode                | -     | 1.63 | -     | W    |
| P <sub>cons</sub>                                      | power consumption             | Power-down mode                                |       |      |       |      |
|                                                        |                               | pin PD = HIGH                                  | -     | 1    | -     | mW   |
|                                                        |                               | I <sup>2</sup> C-bus; EDID                     | -     | 4    | -     | mW   |
|                                                        |                               | I <sup>2</sup> C-bus; EDID; activity detection | -     | 150  | -     | mW   |

[1] x = A, B, C or D.

[2] At 30 % activity on video port output.

### 5. Ordering information

Table 2. Ordering information

| Type number | Package  |                                                                                                           | Version  |
|-------------|----------|-----------------------------------------------------------------------------------------------------------|----------|
|             | Name     | Description                                                                                               |          |
| TDA19978BHV | HLQFP144 | plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad | SOT612-3 |

6. Block diagram

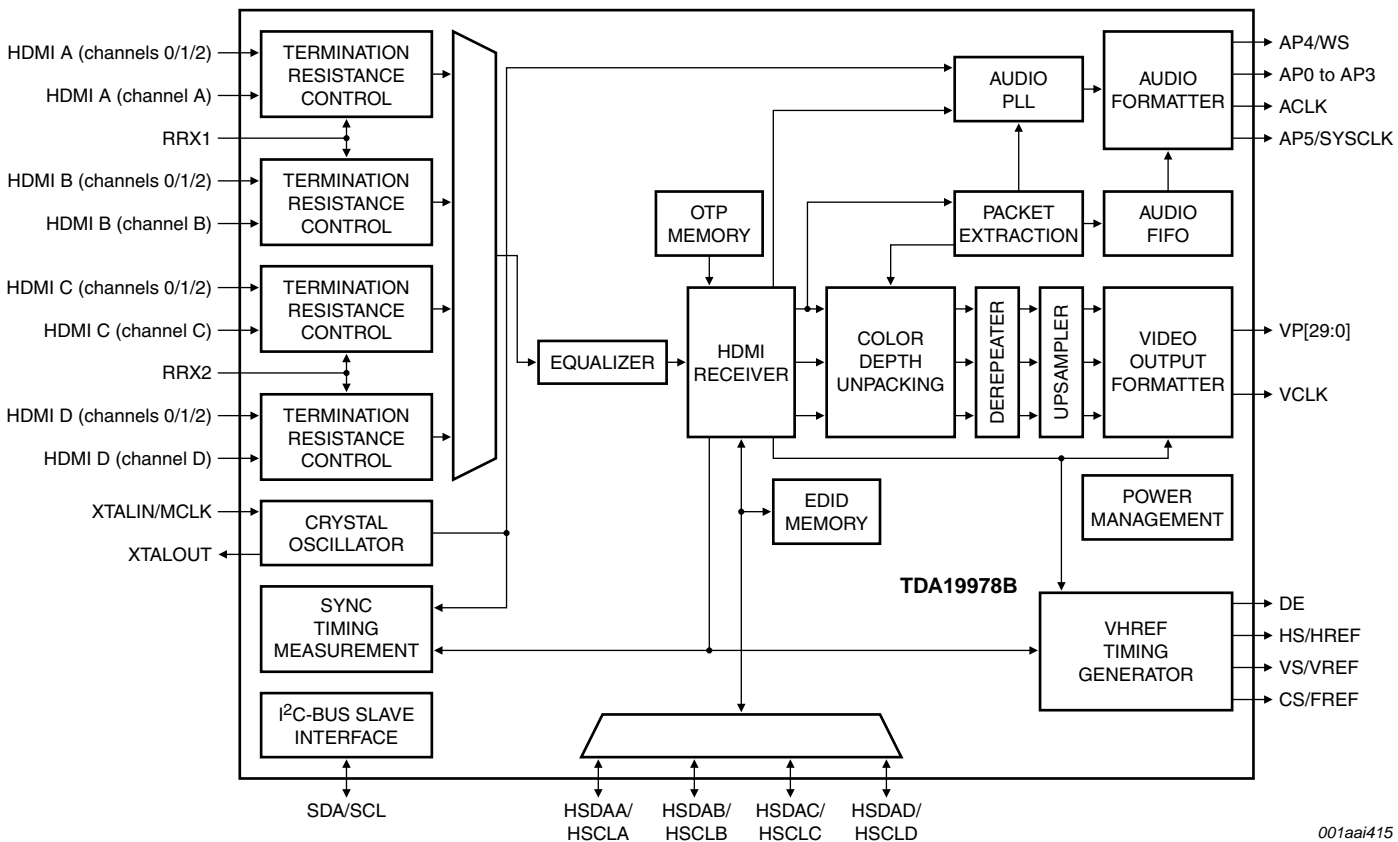


Fig 1. Block diagram of TDA19978B

## 7. Pinning information

### 7.1 Pinning

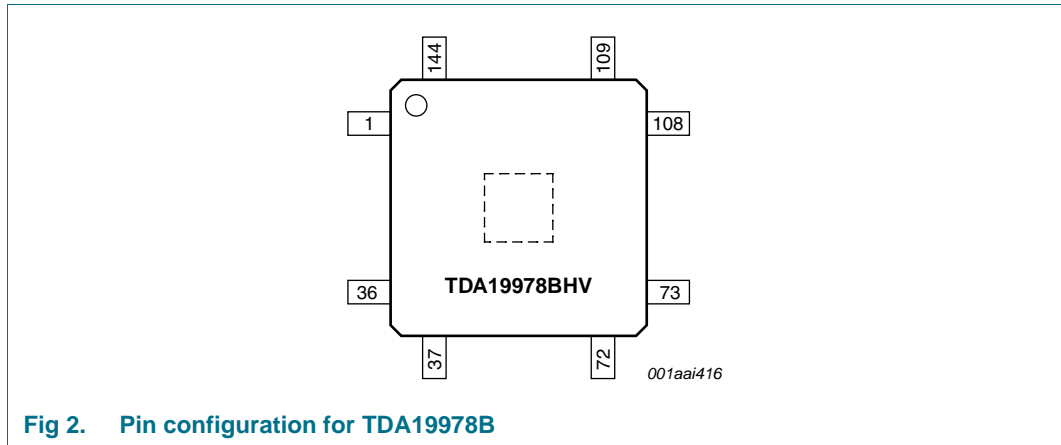


Fig 2. Pin configuration for TDA19978B

### 7.2 Pin description

Table 3. Pin description

| Symbol                | Pin | Type <sup>[1]</sup> | Description                            |
|-----------------------|-----|---------------------|----------------------------------------|
| V <sub>SSC</sub>      | 1   | G                   | ground for the digital core            |
| PD                    | 2   | I                   | power-down control input (active HIGH) |
| V <sub>DDH(3V3)</sub> | 3   | P                   | HDMI receiver supply voltage; 3.3 V    |
| RXDC+                 | 4   | I                   | HDMI input D positive clock channel    |
| RXDC-                 | 5   | I                   | HDMI input D negative clock channel    |
| V <sub>SSH</sub>      | 6   | G                   | HDMI receiver ground                   |
| RXCC-                 | 7   | I                   | HDMI input C negative clock channel    |
| RXCC+                 | 8   | I                   | HDMI input C positive clock channel    |
| V <sub>DDH(3V3)</sub> | 9   | P                   | HDMI receiver supply voltage; 3.3 V    |
| RXD0+                 | 10  | I                   | HDMI input D positive data channel 0   |
| RXD0-                 | 11  | I                   | HDMI input D negative data channel 0   |
| V <sub>SSH</sub>      | 12  | G                   | HDMI receiver ground                   |
| RXC0-                 | 13  | I                   | HDMI input C negative data channel 0   |
| RXC0+                 | 14  | I                   | HDMI input C positive data channel 0   |
| V <sub>DDH(1V8)</sub> | 15  | P                   | HDMI receiver supply voltage; 1.8 V    |
| RXD1+                 | 16  | I                   | HDMI input D positive data channel 1   |
| RXD1-                 | 17  | I                   | HDMI input D negative data channel 1   |
| V <sub>SSH</sub>      | 18  | G                   | HDMI receiver ground                   |
| RXC1-                 | 19  | I                   | HDMI input C negative data channel 1   |
| RXC1+                 | 20  | I                   | HDMI input C positive data channel 1   |
| V <sub>DDH(3V3)</sub> | 21  | P                   | HDMI receiver supply voltage; 3.3 V    |
| RXD2+                 | 22  | I                   | HDMI input D positive data channel 2   |
| RXD2-                 | 23  | I                   | HDMI input D negative data channel 2   |

**Table 3. Pin description ...continued**

| Symbol                | Pin | Type <sup>[1]</sup> | Description                                                       |
|-----------------------|-----|---------------------|-------------------------------------------------------------------|
| V <sub>SSH</sub>      | 24  | G                   | HDMI receiver ground                                              |
| RXC2-                 | 25  | I                   | HDMI input C negative data channel 2                              |
| RXC2+                 | 26  | I                   | HDMI input C positive data channel 2                              |
| V <sub>PP</sub>       | 27  | P                   | OTP memory programming voltage <sup>[2]</sup>                     |
| V <sub>DDC(1V8)</sub> | 28  | P                   | digital core supply voltage; 1.8 V                                |
| V <sub>DDO(3V3)</sub> | 29  | P                   | video port output supply voltage; 3.3 V                           |
| VCLK                  | 30  | O                   | video clock output                                                |
| V <sub>SSO</sub>      | 31  | G                   | video port output ground                                          |
| CS/FREF               | 32  | O                   | composite synchronization output<br>composite field output signal |
| VS/VREF               | 33  | O                   | vertical synchronization output<br>vertical reference output      |
| HS/HREF               | 34  | O                   | horizontal synchronization output<br>horizontal reference output  |
| DE                    | 35  | O                   | data enable output                                                |
| VP[0]                 | 36  | O                   | video port output bit 0                                           |
| V <sub>SSC</sub>      | 37  | G                   | digital core ground                                               |
| VP[1]                 | 38  | O                   | video port output bit 1                                           |
| VP[2]                 | 39  | O                   | video port output bit 2                                           |
| VP[3]                 | 40  | O                   | video port output bit 3                                           |
| V <sub>DDO(3V3)</sub> | 41  | P                   | video port output supply voltage; 3.3 V                           |
| V <sub>DDC(1V8)</sub> | 42  | P                   | digital core supply voltage; 1.8 V                                |
| V <sub>SSO</sub>      | 43  | G                   | video port output ground                                          |
| VP[4]                 | 44  | O                   | video port output bit 4                                           |
| VP[5]                 | 45  | O                   | video port output bit 5                                           |
| VP[6]                 | 46  | O                   | video port output bit 6                                           |
| VP[7]                 | 47  | O                   | video port output bit 7                                           |
| VP[8]                 | 48  | O                   | video port output bit 8                                           |
| VP[9]                 | 49  | O                   | video port output bit 9                                           |
| VP[10]                | 50  | O                   | video port output bit 10                                          |
| VP[11]                | 51  | O                   | video port output bit 11                                          |
| V <sub>DDO(3V3)</sub> | 52  | P                   | video port output supply voltage; 3.3 V                           |
| VP[12]                | 53  | O                   | video port output bit 12                                          |
| V <sub>SSO</sub>      | 54  | G                   | video port output ground                                          |
| VP[13]                | 55  | O                   | video port output bit 13                                          |
| VP[14]                | 56  | O                   | video port output bit 14                                          |
| VP[15]                | 57  | O                   | video port output bit 15                                          |
| VP[16]                | 58  | O                   | video port output bit 16                                          |
| VP[17]                | 59  | O                   | video port output bit 17                                          |
| VP[18]                | 60  | O                   | video port output bit 18                                          |
| VP[19]                | 61  | O                   | video port output bit 19                                          |

Table 3. Pin description ...continued

| Symbol                  | Pin | Type <sup>[1]</sup> | Description                                                                                                                                                                            |
|-------------------------|-----|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VP[20]                  | 62  | O                   | video port output bit 20                                                                                                                                                               |
| V <sub>DDO(3V3)</sub>   | 63  | P                   | video port output supply voltage; 3.3 V                                                                                                                                                |
| V <sub>DDC(1V8)</sub>   | 64  | P                   | digital core supply voltage; 1.8 V                                                                                                                                                     |
| V <sub>SSO</sub>        | 65  | G                   | video port output ground                                                                                                                                                               |
| VP[21]                  | 66  | O                   | video port output bit 21                                                                                                                                                               |
| VP[22]                  | 67  | O                   | video port output bit 22                                                                                                                                                               |
| VP[23]                  | 68  | O                   | video port output bit 23                                                                                                                                                               |
| VP[24]                  | 69  | O                   | video port output bit 24                                                                                                                                                               |
| VP[25]                  | 70  | O                   | video port output bit 25                                                                                                                                                               |
| VP[26]                  | 71  | O                   | video port output bit 26                                                                                                                                                               |
| VP[27]                  | 72  | O                   | video port output bit 27                                                                                                                                                               |
| V <sub>SSC</sub>        | 73  | G                   | digital core ground                                                                                                                                                                    |
| V <sub>DDO(3V3)</sub>   | 74  | P                   | video port output supply voltage; 3.3 V                                                                                                                                                |
| VP[28]                  | 75  | O                   | video port output bit 28                                                                                                                                                               |
| VP[29]                  | 76  | O                   | video port output bit 29                                                                                                                                                               |
| V <sub>SSO</sub>        | 77  | G                   | video port output ground                                                                                                                                                               |
| ACLK                    | 78  | O                   | audio clock output                                                                                                                                                                     |
| AP0                     | 79  | O                   | audio port 0 output                                                                                                                                                                    |
| AP1                     | 80  | O                   | audio port 1 output                                                                                                                                                                    |
| AP2                     | 81  | O                   | audio port 2 output                                                                                                                                                                    |
| AP3                     | 82  | O                   | audio port 3 output                                                                                                                                                                    |
| AP4/WS                  | 83  | O                   | audio port 4 output<br>word select output                                                                                                                                              |
| V <sub>DDO(3V3)</sub>   | 84  | P                   | video port output supply voltage; 3.3 V                                                                                                                                                |
| AP5/SYSCLK              | 85  | O                   | audio port 5 output<br>system clock audio output                                                                                                                                       |
| V <sub>SSO</sub>        | 86  | G                   | video port output ground                                                                                                                                                               |
| V <sub>DDH(3V3)</sub>   | 87  | P                   | HDMI audio PLL supply voltage; 3.3 V                                                                                                                                                   |
| V <sub>DDH(3V3)</sub>   | 88  | P                   | HDMI audio PLL supply voltage; 3.3 V                                                                                                                                                   |
| V <sub>SSH</sub>        | 89  | G                   | HDMI audio PLL ground                                                                                                                                                                  |
| V <sub>DDH(1V8)</sub>   | 90  | P                   | HDMI audio PLL supply voltage; 1.8 V                                                                                                                                                   |
| V <sub>SSH</sub>        | 91  | G                   | HDMI audio PLL ground                                                                                                                                                                  |
| V <sub>DDC(1V8)</sub>   | 92  | P                   | digital core supply voltage; 1.8 V                                                                                                                                                     |
| XTALOUT                 | 93  | O                   | crystal oscillator output                                                                                                                                                              |
| XTALIN/MCLK             | 94  | I                   | crystal oscillator input<br>test pattern clock input                                                                                                                                   |
| V <sub>DDI(3V3)</sub>   | 95  | P                   | digital inputs supply voltage; 3.3 V                                                                                                                                                   |
| $\overline{\text{VAI}}$ | 96  | O                   | video activity indication output (open-drain); warns the external microprocessor that a special event has occurred; must be connected to a pull-up resistor; 5 V tolerant (active LOW) |
| SDA                     | 97  | I/O                 | I <sup>2</sup> C-bus serial data input/output                                                                                                                                          |

Table 3. Pin description ...continued

| Symbol         | Pin | Type <sup>[1]</sup> | Description                                                       |
|----------------|-----|---------------------|-------------------------------------------------------------------|
| SCL            | 98  | I                   | I <sup>2</sup> C-bus serial clock input                           |
| HSDAA          | 99  | I/O                 | HDMI input/output A DDC-bus serial data                           |
| HSCLA          | 100 | I                   | HDMI input A DDC-bus serial clock                                 |
| HSDAB          | 101 | I/O                 | HDMI input/output B DDC-bus serial data                           |
| HSCLB          | 102 | I                   | HDMI input B DDC-bus serial clock                                 |
| TEST0          | 103 | I                   | reserved for test; connect to digital inputs ground ( $V_{SSC}$ ) |
| $V_{DDH(3V3)}$ | 104 | P                   | HDMI deep PLL supply voltage; 3.3 V                               |
| $V_{SSH}$      | 105 | G                   | HDMI deep PLL ground                                              |
| RRX1           | 106 | I                   | HDMI inputs A and B termination resistance control                |
| $V_{DDC(1V8)}$ | 107 | P                   | digital core supply voltage; 1.8 V                                |
| $V_{DDH(1V8)}$ | 108 | P                   | HDMI receiver supply voltage; 1.8 V                               |
| $V_{SSC}$      | 109 | G                   | digital core ground                                               |
| A0             | 110 | I                   | I <sup>2</sup> C-bus address control input                        |
| $V_{DDH(3V3)}$ | 111 | P                   | HDMI receiver supply voltage; 3.3 V                               |
| RXBC+          | 112 | I                   | HDMI input B positive clock channel                               |
| RXBC-          | 113 | I                   | HDMI input B negative clock channel                               |
| $V_{SSH}$      | 114 | G                   | HDMI receiver ground                                              |
| RXAC-          | 115 | I                   | HDMI input A negative clock channel                               |
| RXAC+          | 116 | I                   | HDMI input A positive clock channel                               |
| $V_{DDH(3V3)}$ | 117 | P                   | HDMI receiver supply voltage; 3.3 V                               |
| RXB0+          | 118 | I                   | HDMI input B positive data channel 0                              |
| RXB0-          | 119 | I                   | HDMI input B negative data channel 0                              |
| $V_{SSH}$      | 120 | G                   | HDMI receiver ground                                              |
| RXA0-          | 121 | I                   | HDMI input A negative data channel 0                              |
| RXA0+          | 122 | I                   | HDMI input A positive data channel 0                              |
| $V_{DDH(1V8)}$ | 123 | P                   | HDMI receiver supply voltage; 1.8 V                               |
| RXB1+          | 124 | I                   | HDMI input B positive data channel 1                              |
| RXB1-          | 125 | I                   | HDMI input B negative data channel 1                              |
| $V_{SSH}$      | 126 | G                   | HDMI receiver ground                                              |
| RXA1-          | 127 | I                   | HDMI input A negative data channel 1                              |
| RXA1+          | 128 | I                   | HDMI input A positive data channel 1                              |
| $V_{DDH(3V3)}$ | 129 | P                   | HDMI receiver supply voltage; 3.3 V                               |
| RXB2+          | 130 | I                   | HDMI input B positive data channel 2                              |
| RXB2-          | 131 | I                   | HDMI input B negative data channel 2                              |
| $V_{SSH}$      | 132 | G                   | HDMI receiver ground                                              |
| RXA2-          | 133 | I                   | HDMI input A negative data channel 2                              |
| RXA2+          | 134 | I                   | HDMI input A positive data channel 2                              |
| $V_{SSH}$      | 135 | G                   | HDMI receiver ground                                              |
| $V_{DDC(1V8)}$ | 136 | P                   | digital core supply voltage; 1.8 V                                |
| $V_{DDC(1V8)}$ | 137 | P                   | digital core supply voltage; 1.8 V                                |
| HSDAC          | 138 | I/O                 | HDMI input/output C DDC-bus serial data                           |



Table 3. Pin description ...continued

| Symbol                | Pin | Type <sup>[1]</sup> | Description                                                         |
|-----------------------|-----|---------------------|---------------------------------------------------------------------|
| HSCLC                 | 139 | I                   | HDMI input C DDC-bus serial clock                                   |
| HSDAD                 | 140 | I/O                 | HDMI input/output D DDC-bus serial data                             |
| HSCLD                 | 141 | I                   | HDMI input D DDC-bus serial clock                                   |
| V <sub>DDI(3V3)</sub> | 142 | P                   | digital inputs supply voltage; 3.3 V                                |
| RRX2                  | 143 | I                   | HDMI inputs C and D termination resistance control                  |
| V <sub>DDH(1V8)</sub> | 144 | P                   | HDMI receiver supply voltage; 1.8 V                                 |
| Exposed die pad       | -   | G                   | exposed die pad; connect to digital core ground (V <sub>SSC</sub> ) |

[1] P = power supply; G = ground; I = input; O = output and I/O = input/output.

[2] Connected to the ground of the HDMI receiver (V<sub>SSH</sub>) in normal operation.

## 8. Functional description

The TDA19978B converts digital data streams input by the HDMI sources into parallel digital data for use by media and video signal processing integrated circuits in devices for HDTV. Data streams can be decoded without HDCP protection.

Outputs from the TDA19978B can be RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2 semi-planar format based on the ITU-R BT.601 standard or YCbCr 4:2:2 based on the ITU-R BT.656 format. Inputs can be both progressive and interlaced formats. The TDA19978B comprises a color space conversion block, downsampling filters and an embedded timing code function. In addition, the repeater function enables other HDMI devices to be connected to form an extended "total application".

### 8.1 Software drivers

Software drivers are provided for easy configuration and use of the TDA19978B. These drivers can be integrated with a large range of processors, with or without an operating system. They control activity detection, input selection, video mode identification, color conversion, Power-down modes and InfoFrame notification.

### 8.2 HDMI inputs

Control of the four HDMI inputs can be automatic using activity detection or using the I<sup>2</sup>C-bus. The HDMI receiver inputs are defined by pins RXx0+, RXx0-, RXx1+, RXx1-, RXx2+, RXx2-, RXxC+, RXxC-, RRX1, RRX2, HSCLx and HSDAx (x equals A, B, C or D as applicable).

### 8.3 Termination resistance control

The HDMI receiver input contains a termination resistance control set by an external resistor connected between pins RRXx and V<sub>DDH(3V3)</sub> (x equals 1 for inputs A and B or 2 for inputs C and D). Typically, the characteristic impedance is 50 Ω and the default value of the external terminal control resistor is 12 kΩ ± 1 %.

## 8.4 Equalizer

The auto-adaptive equalizer automatically measures and selects the settings which provide the best signal quality for each cable. This improves signal quality and enables the use of cable lengths up to 25 m (laboratory tested, contact NXP semiconductors for detailed information). The equalizer is fully automatic and consequently does not need any external control.

## 8.5 Activity detection

The TDA19978B uses activity detection to automatically select the active HDMI input. An internal, fully programmable, frequency filter controls activity detection. It sees only the activity on the HDMI inputs with a frequency range between the minimal frequency (22.5 MHz) and the maximal frequency (205 MHz).

This activity detection can generate an interrupt enabling users to manage each HDMI input.

## 8.6 Color depth unpacking

In Deep Color mode, the TDA19978B receives several fragments of a pixel group at the HDMI link frequency. The color depth unpacking block translates the received pixel group into pixels at the pixel frequency. This operation is fully automatic and does not need any external control.

## 8.7 Derepeater

The HDMI source uses pixel repetition to increase the transmitted pixel clock frequency for transmitting video formats at native pixel rates below 25 Mpixel/s or to increase the number of audio sample packets in each line. The derepeater function discards repeated pixels and divides the clock to reproduce the native video format.

## 8.8 Upsample

The HDMI source can use YCbCr 4:2:2 pixel encoding which enables the number of bits allocated per component to be increased up to 12. The upsample function transforms this 12-bit YCbCr 4:2:2 data stream into a 12-bit YCbCr 4:4:4 data stream by repeating or linearly interpolating the chrominance pixels Cb and Cr.

Upsampling mode is selected using the I<sup>2</sup>C-bus.

## 8.9 Packet extraction

Information sent during the Data Island periods is extracted from the HDMI data stream. Audio clock regeneration, general control and InfoFrames can be read using the I<sup>2</sup>C-bus while audio samples are sent to the audio FIFO.

The TDA19978B can receive HDMI 1.3a packets, general control and color gamut metadata packets.

In audio applications, the TDA19978B manages HBR packets for high bit rate compressed audio streams (IEC 61937), OBA samples and DST packets for one bit audio and SACD with DSD and DST audio streams.

The TDA19978B includes a two-channel status decoder supporting multi-channel reception for audio sample packets. This enables the user to obtain channel status information from the IEC 60958/IEC 61937 stream such as:

- The audio stream type (non-linear as IEC 61937 or L-PCM as IEC 60958)
- Copyright protection
- Sampling frequency

Refer to *IEC 60958/IEC 61937* specifications for more details.

An update of each InfoFrame or the channel status content is indicated by a register bit and the HIGH-to-LOW transition on output pin VA1. This makes CPU polling unnecessary.

### 8.10 Audio PLL

The TDA19978B generates a  $128/256/512 \times f_s$  system clock enabling the use of simple audio DACs without an integrated PLL, such as the UDA1334BTS. The programming of the audio PLL can be either automatic, using the audio clock regeneration parameters found in the Data Islands or set manually using the I<sup>2</sup>C-bus.

All standard audio sampling frequencies 32 kHz, 44.1 kHz, 88.2 kHz, 176.4 kHz, 48 kHz, 96 kHz and 192 kHz are accepted by the device.

### 8.11 Audio formatter

Audio samples can be output in either S/PDIF, I<sup>2</sup>S-bus formats or DSD (SACD). In I<sup>2</sup>S-bus or S/PDIF modes, up to eight audio channels can be controlled using the audio port pins (AP0 to AP5). In DSD mode (SACD), up to six audio channels can be controlled using these pins. The audio port mapping depends on the channel allocation (see [Table 4](#), [Table 5](#) and [Table 6](#) for detailed information).

**Table 4. Audio port configuration (Layout 0)**

All audio ports are LV-TTL compatible.

| Audio port | Pin | Layout 0                         |                                        |                     |
|------------|-----|----------------------------------|----------------------------------------|---------------------|
|            |     | I <sup>2</sup> S-bus             | S/PDIF                                 | OBA                 |
| AP5        | 85  | SYSCLK <sup>[1]</sup>            | SYSCLK <sup>[1]</sup>                  |                     |
| AP4        | 83  | WS (word select)                 | WS <sup>[1]</sup>                      |                     |
| AP3        | 82  |                                  |                                        |                     |
| AP2        | 81  |                                  |                                        |                     |
| AP1        | 80  |                                  |                                        | DSD channel 1       |
| AP0        | 79  | SD                               | S/PDIF                                 | DSD channel 0       |
| ACLK       | 78  | SCK (I <sup>2</sup> S-bus clock) | master clock for S/PDIF <sup>[1]</sup> | DSD clock           |
|            |     | 64 × f <sub>s</sub>              | 64 × f <sub>s</sub>                    | 64 × f <sub>s</sub> |
|            |     | 32 × f <sub>s</sub>              |                                        |                     |

[1] Can be activated with the I<sup>2</sup>C-bus (optional).

**Table 5. Audio port configuration (Layout 1)**

All audio ports are LV-TTL compatible.

| Audio port | Pin | Layout 1                         |                                        |                     |
|------------|-----|----------------------------------|----------------------------------------|---------------------|
|            |     | I <sup>2</sup> S-bus             | S/PDIF                                 | OBA                 |
| AP5        | 85  | SYSCLK <sup>[1]</sup>            | SYSCLK <sup>[1]</sup>                  | DSD channel 5       |
| AP4        | 83  | WS (word select)                 | WS <sup>[1]</sup>                      | DSD channel 4       |
| AP3        | 82  | SD3                              | S/PDIF3                                | DSD channel 3       |
| AP2        | 81  | SD2                              | S/PDIF2                                | DSD channel 2       |
| AP1        | 80  | SD1                              | S/PDIF1                                | DSD channel 1       |
| AP0        | 79  | SD0                              | S/PDIF0                                | DSD channel 0       |
| ACLK       | 78  | SCK (I <sup>2</sup> S-bus clock) | master clock for S/PDIF <sup>[1]</sup> | DSD clock           |
|            |     | 64 × f <sub>s</sub>              | 64 × f <sub>s</sub>                    | 64 × f <sub>s</sub> |
|            |     | 32 × f <sub>s</sub>              |                                        |                     |

[1] Can be activated with the I<sup>2</sup>C-bus (optional).

**Table 6. Audio port configuration for HBR and DST packets**

All audio ports are LV-TTL compatible.

| Audio port | Pin | HBR demultiplexed                |                                        | DST                  |
|------------|-----|----------------------------------|----------------------------------------|----------------------|
|            |     | I <sup>2</sup> S-bus             | S/PDIF                                 |                      |
| AP5        | 85  | SYSCLK <sup>[1]</sup>            | SYSCLK <sup>[1]</sup>                  |                      |
| AP4        | 83  | WS (word select)                 | WS <sup>[1]</sup>                      | frame_start          |
| AP3        | 82  | SDx + 3                          | S/PDIFx + 3                            |                      |
| AP2        | 81  | SDx + 2                          | S/PDIFx + 2                            |                      |
| AP1        | 80  | SDx + 1                          | S/PDIFx + 1                            |                      |
| AP0        | 79  | SDx                              | S/PDIFx                                | DSD channel 0        |
| ACLK       | 78  | SCK (I <sup>2</sup> S-bus clock) | master clock for S/PDIF <sup>[1]</sup> | DSD clock            |
|            |     | 64 × f <sub>s</sub> (ACR)        | 64 × f <sub>s</sub>                    | 64 × f <sub>s</sub>  |
|            |     | 32 × f <sub>s</sub> (ACR)        |                                        | 128 × f <sub>s</sub> |

[1] Can be activated with the I<sup>2</sup>C-bus (optional).

### 8.12 Sync timing measurement

To assist input format recognition, the vertical/horizontal periods and the horizontal pulse width are measured based on the externally generated MCLK frequency (27 MHz crystal). This function has an accuracy of 1 LSB = 1 × MCLK period.

### 8.13 Format measurement timing

The TDA19978B includes an improved system for accurate recognition of PC and TV formats. This system measures the parameters of blanking and video active area.

This function can be useful for example when the TDA19978B receives PC format data in HDMI or DVI modes.

### 8.14 Color space conversion

The color space conversion enables an RGB signal from the HDMI input to be converted into a YCbCr signal or converting the YCbCr signal from the HDMI input into an RGB signal. The color space conversion formula is:

$$\begin{bmatrix} YG \\ VR \\ UB \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left( \begin{bmatrix} CY \\ RV \\ BU \end{bmatrix} + \begin{bmatrix} O11 \\ O12 \\ O13 \end{bmatrix} \right) + \begin{bmatrix} O01 \\ O02 \\ O03 \end{bmatrix} \quad (1)$$

Activation of the color space conversion function and programming of all coefficients and offsets is done via the I<sup>2</sup>C-bus.

### 8.15 4:2:2 downsampling filters

These filters downsample the Cb and Cr signals by a factor of 2. A delay has been added to the G/Y channel corresponding to the downsample filters pipeline delay to make sure the Y channel is in phase with the Cb and Cr channels.

Four different filters, from simple cut to ITU-R BT.601 compliant digital, can be selected using the I<sup>2</sup>C-bus.

### 8.16 Range control

The range control function truncates the range of data to remove super-white and super-black pixels at specified ceiling and floor values.

### 8.17 Dithering function

The error dispersal rounding (dithering) function can convert the color depth from 30-bit or 36-bit to reduced 30-bit or 24-bit color depth. When dithering is triggered, the TDA19978B applies round, truncate or noise-shaping algorithms.

When the error dispersal rounding function is not used, the data coming from the filter is directly sent to the 4:2:2 formatter. The error dispersal rounding function works only with the active video signal.

### 8.18 4:2:2 formatter

The 4:2:2 formatter contains the YCbCr 4:2:2 semi-planar and the YCbCr 4:2:2 ITU-R BT.656 formatting functions. The selection of these functions is made using the I<sup>2</sup>C-bus.

- In YCbCr 4:2:2 mode: the data frequency of the Y signal is equal to the pixel clock frequency. While the data frequency of the Cb and Cr signals is equal to half the pixel clock frequency
- In semi-planar mode: the output clock frequency should be the same as the pixel clock frequency
- In ITU-R BT.656 mode: the data frequency should be the same as the formatter clock frequency (e.g. pixel clock frequency × 2)

The Start Active Video (SAV) and End Active Video (EAV) timing reference codes can be included in the data stream based on the HREF, VREF and FREF positions from the VHREF timing generator.

Specific codes programmed using the I<sup>2</sup>C-bus can replace the data stream during the blanking period to mask gain and clamp calibration.

### 8.19 Video port selection

Each channel can be allocated to a specified video port using the I<sup>2</sup>C-bus (see [Section 13 "Output video port formats \(mapping examples\)" on page 20](#)) to optimize board layout at the interface with video processing ICs. For example:

- R, G or B in RGB 4:4:4 mode on pins VP[29:20]
- Y, Cb or Cr in YUV 4:4:4 mode on pins VP[19:10]
- Y or Cb-Cr in 4:2:2 semi-planar mode on pins VP[9:0]
- Cb-Y-Cr-Y in 4:2:2 ITU-R BT.656 mode on pins VP[9:0]

Each video port can be set to high-impedance using the I<sup>2</sup>C-bus.

### 8.20 Output buffers

The output buffers are LV-TTL compatible. The outputs can be switched between active and high-impedance by the I<sup>2</sup>C-bus.

The outputs HREF, VREF and FREF can be set to high-impedance (Z) or forced LOW (L), independently of the timing reference codes.

### 8.21 VHREF timing generator

The VHREF timing generator outputs all of the timing signals used by the device:

- VREF, HREF and FREF signals for SAV, EAV and active video area definition
- VS and HS to change width and position compared with the HDMI inputs

### 8.22 I<sup>2</sup>C-bus serial interface

The I<sup>2</sup>C-bus serial interface enables the internal registers of the device to be programmed. The slave address of the device is selected by pin A0.

### 8.23 Power management

The TDA19978B can use one of three Power-down modes:

- level 0: full Power-down mode
- level 1: internal EDID memory with I<sup>2</sup>C-bus serial interface active
- level 2: internal EDID memory with I<sup>2</sup>C-bus serial interface and activity detection enabled

The user can activate each mode with pin PD or using I<sup>2</sup>C-bus registers:

- level 0: PD pin is HIGH
- level 1: settings defined in the I<sup>2</sup>C-bus registers
- level 2: settings defined in the I<sup>2</sup>C-bus registers

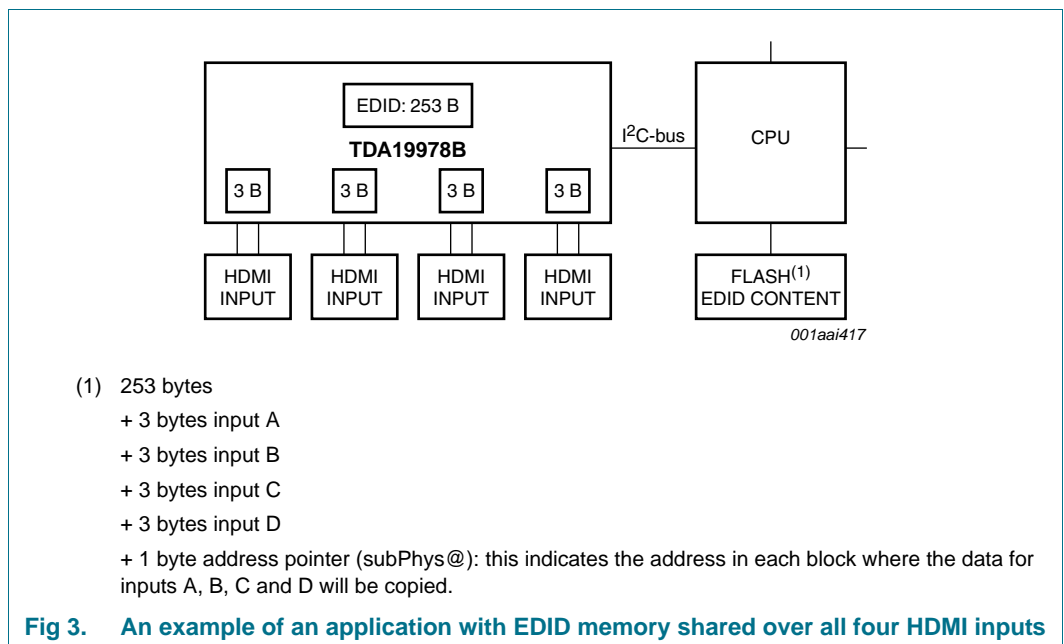
### 8.24 EDID memory management

The TDA19978B embedded EDID memory can be shared with all HDMI inputs. The embedded EDID memory shares 253 bytes with the four HDMI inputs. In addition, three bytes are dedicated to the physical address and checksum for each HDMI input (see [Figure 3](#)). This memory is accessible in parallel by all HDMI inputs. You can share the EDID memory over zero, one, two, three or four HDMI input(s) as shown in [Figure 4](#).

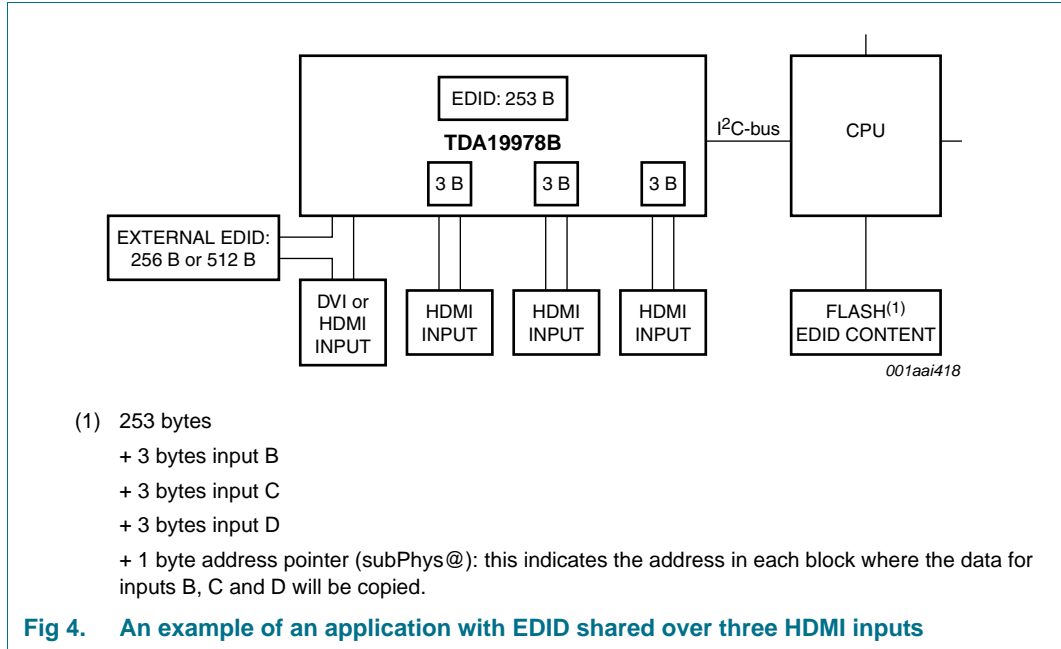
The content of embedded volatile EDID memory must be programmed using the I<sup>2</sup>C-bus for each power-on of TDA19978B. The embedded EDID memory remains accessible on each HDMI input when the TDA19978B uses a different low-power mode.

The “physical address” of each HDMI input can be easily changed with the TDA19978B without corrupting the integrity of each DDC-bus.

#### 8.24.1 EDID memory shared over all four HDMI inputs



8.24.2 EDID memory shared over three HDMI inputs



9. I<sup>2</sup>C-bus protocol

The TDA19978B is a slave I<sup>2</sup>C-bus device and the SCL pin is only an input pin. The timing and protocol for I<sup>2</sup>C-bus are standard.

Bit A0 of the I<sup>2</sup>C-bus device address is externally selected by the A0 pin. The main device I<sup>2</sup>C-bus address is given in [Table 7](#).

Table 7. I<sup>2</sup>C-bus slave address

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 1  | 0  | 0  | 1  | 1  | 0  | A0 | 0/1 |

10. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                | Parameter                        | Conditions | Min   | Max   | Unit |
|-----------------------|----------------------------------|------------|-------|-------|------|
| V <sub>DDx(3V3)</sub> | supply voltage on all 3.3 V pins |            | -0.5  | +4.6  | V    |
| V <sub>DDx(1V8)</sub> | supply voltage on all 1.8 V pins |            | -0.5  | +2.5  | V    |
| ΔV <sub>DD</sub>      | supply voltage difference        |            | -0.5  | +0.5  | V    |
| I <sub>O</sub>        | output current                   |            | -     | 35    | mA   |
| T <sub>stg</sub>      | storage temperature              |            | -55   | +150  | °C   |
| T <sub>amb</sub>      | ambient temperature              |            | 0     | 70    | °C   |
| T <sub>j</sub>        | junction temperature             |            | -     | 125   | °C   |
| V <sub>ESD</sub>      | electrostatic discharge voltage  | HBM        | -2000 | +2000 | V    |



## 11. Thermal characteristics

**Table 9. Thermal characteristics**

| Symbol        | Parameter                                   | Conditions  | Typ  | Unit |
|---------------|---------------------------------------------|-------------|------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 22.8 | K/W  |
| $R_{th(j-c)}$ | thermal resistance from junction to case    |             | 11.1 | K/W  |

## 12. Characteristics

**Table 10. Characteristics**

$T_{amb} = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ; typical values measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                   | Parameter                                            | Conditions                          | Min   | Typ  | Max   | Unit |    |
|--------------------------|------------------------------------------------------|-------------------------------------|-------|------|-------|------|----|
| <b>Supplies</b>          |                                                      |                                     |       |      |       |      |    |
| $V_{DDH(3V3)}$           | HDMI supply voltage (3.3 V)                          |                                     | 3.135 | 3.3  | 3.465 | V    |    |
| $V_{DDH(1V8)}$           | HDMI supply voltage (1.8 V)                          |                                     | 1.71  | 1.8  | 1.89  | V    |    |
| $V_{DDI(3V3)}$           | input supply voltage (3.3 V)                         |                                     | 3.135 | 3.3  | 3.465 | V    |    |
| $V_{DDC(1V8)}$           | core supply voltage (1.8 V)                          |                                     | 1.71  | 1.8  | 1.89  | V    |    |
| $V_{DDO(3V3)}$           | output supply voltage (3.3 V)                        |                                     | 3.135 | 3.3  | 3.465 | V    |    |
| $I_{DDH(3V3)}$           | HDMI supply current (3.3 V)                          | 720p at 60 Hz                       | [1]   | -    | 103   | -    | mA |
|                          |                                                      | 1080p at 60 Hz                      | [1]   | -    | 106   | -    | mA |
|                          |                                                      | 1080p at 60 Hz; Deep Color mode     | [1]   | -    | 110   | -    | mA |
| $I_{DDH(1V8)}$           | HDMI supply current (1.8 V)                          | 720p at 60 Hz                       | [1]   | -    | 48    | -    | mA |
|                          |                                                      | 1080p at 60 Hz                      | [1]   | -    | 68    | -    | mA |
|                          |                                                      | 1080p at 60 Hz; Deep Color mode     | [1]   | -    | 85    | -    | mA |
| $I_{DDI(3V3)}$           | input supply current (3.3 V)                         | 720p at 60 Hz                       | [1]   | -    | 1     | -    | mA |
|                          |                                                      | 1080p at 60 Hz                      | [1]   | -    | 1     | -    | mA |
|                          |                                                      | 1080p at 60 Hz; Deep Color mode     | [1]   | -    | 1     | -    | mA |
| $I_{DDO(3V3)}$           | output supply current (3.3 V)                        | 720p at 60 Hz                       | [1]   | -    | 49    | -    | mA |
|                          |                                                      | 1080p at 60 Hz                      | [1]   | -    | 78    | -    | mA |
|                          |                                                      | 1080p at 60 Hz; Deep Color mode     | [1]   | -    | 120   | -    | mA |
| $I_{DDC(1V8)}$           | core supply current (1.8 V)                          | 720p at 60 Hz                       | [1]   | -    | 148   | -    | mA |
|                          |                                                      | 1080p at 60 Hz                      | [1]   | -    | 283   | -    | mA |
|                          |                                                      | 1080p at 60 Hz; Deep Color mode     | [1]   | -    | 453   | -    | mA |
| $\Delta V_{DD(3V3-3V3)}$ | supply voltage difference between two 3.3 V supplies | start-up and established conditions | -100  | -    | +100  | mV   |    |
| $\Delta V_{DD(1V8-1V8)}$ | supply voltage difference between two 1.8 V supplies | start-up and established conditions | -100  | -    | +100  | mV   |    |
| P                        | power dissipation                                    | Active mode                         | [1]   |      |       |      |    |
|                          |                                                      | 720p at 60 Hz                       | -     | 0.75 | -     | W    |    |
|                          |                                                      | 1080p at 60 Hz                      | -     | 1.13 | -     | W    |    |
|                          |                                                      | 1080p at 60 Hz; Deep Color mode     | -     | 1.63 | -     | W    |    |

**Table 10. Characteristics ...continued**

$T_{amb} = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ; typical values measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol     | Parameter         | Conditions                                     | Min | Typ | Max | Unit |
|------------|-------------------|------------------------------------------------|-----|-----|-----|------|
| $P_{cons}$ | power consumption | Power-down mode                                |     |     |     |      |
|            |                   | pin PD = HIGH                                  | -   | 1   | -   | mW   |
|            |                   | I <sup>2</sup> C-bus; EDID                     | -   | 4   | -   | mW   |
|            |                   | I <sup>2</sup> C-bus; EDID; activity detection | -   | 150 | -   | mW   |

**Clock timing output: pins VCLK, ACLK and SYSCLK**

|                |                         |            |     |    |   |     |
|----------------|-------------------------|------------|-----|----|---|-----|
| $f_{clk(max)}$ | maximum clock frequency | pin VCLK   | 165 | -  | - | MHz |
|                |                         | pin ACLK   | 25  | -  | - | MHz |
|                |                         | pin SYSCLK | 50  | -  | - | MHz |
| $\delta_{clk}$ | clock duty cycle        | pin VCLK   | -   | 50 | - | %   |
|                |                         | pin ACLK   | -   | 50 | - | %   |
|                |                         | pin SYSCLK | -   | 50 | - | %   |

**Timing output: pins VP[29:0];  $f_s = 165\text{ MHz}$ ;  $C_L = 10\text{ pF}$ ; see [Figure 5](#)**

|               |                         |                                                   |      |                     |      |    |
|---------------|-------------------------|---------------------------------------------------|------|---------------------|------|----|
| $t_{su(Q)}$   | data output set-up time |                                                   | 0.40 | -                   | 1.50 | ns |
| $t_{h(Q)}$    | data output hold time   |                                                   | 0.80 | -                   | 2.00 | ns |
| $t_{d(pipe)}$ | pipeline delay time     | clock intervals from inputs to outputs; all modes | -    | $80 \times T_{clk}$ | -    |    |

**Timing output: pins AP[5:0] with respect to pin ACLK;  $f_{clk} = 12.288\text{ MHz}$ ;  $C_L = 10\text{ pF}$ ; see [Figure 6](#)**

|             |                         |  |    |   |   |    |
|-------------|-------------------------|--|----|---|---|----|
| $t_{su(Q)}$ | data output set-up time |  | 69 | - | - | ns |
| $t_{h(Q)}$  | data output hold time   |  | 2  | - | - | ns |

**LV-TTL digital outputs: pins VP[29:0], VCLK, AP[5:0], ACLK, DE, HS, VS, HREF, VREF, FREF;  $C_L = 10\text{ pF}$**

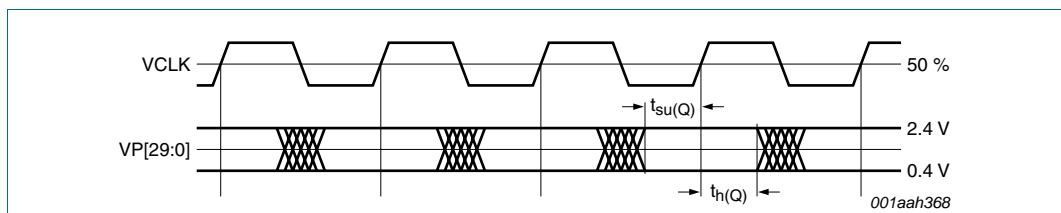
|           |                                  |                                          |                     |      |     |               |               |
|-----------|----------------------------------|------------------------------------------|---------------------|------|-----|---------------|---------------|
| $V_{OL}$  | LOW-level output voltage         | $I_{OL} = 2\text{ mA}$                   | -                   | -    | 0.4 | V             |               |
| $V_{OH}$  | HIGH-level output voltage        | $I_{OH} = -2\text{ mA}$                  | 2.4                 | -    | -   | V             |               |
| $I_{LOZ}$ | OFF-state output leakage current | high-impedance state; $V_O = 0\text{ V}$ | <a href="#">[2]</a> | -    | 0   | $\mu\text{A}$ |               |
|           |                                  | $V_O = V_{DDO(3V3)} \times \frac{1}{3}$  |                     | 10   | -   | 100           | $\mu\text{A}$ |
|           |                                  | $V_O = V_{DDO(3V3)} \times \frac{2}{3}$  |                     | -100 | -   | -10           | $\mu\text{A}$ |
|           |                                  | $V_O = V_{DDO(3V3)}$                     |                     | -    | 0   | -             | $\mu\text{A}$ |

**Table 10. Characteristics ...continued**

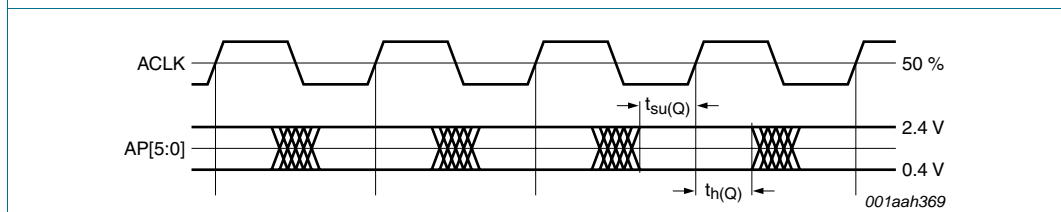
$T_{amb} = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ; typical values measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                                                                   | Parameter                         | Conditions                                                                         | Min   | Typ | Max   | Unit |
|--------------------------------------------------------------------------|-----------------------------------|------------------------------------------------------------------------------------|-------|-----|-------|------|
| <b>Digital inputs: pins RXxC+, RXxC- [3]</b>                             |                                   |                                                                                    |       |     |       |      |
| $V_{I(dif)}$                                                             | differential input voltage        | $R_{RRX1} = 12\text{ k}\Omega \pm 1\%$ ;<br>$R_{RRX2} = 12\text{ k}\Omega \pm 1\%$ | 150   | -   | 1200  | mV   |
| $V_{I(cm)}$                                                              | common-mode input voltage         |                                                                                    | 2.735 | -   | 3.475 | V    |
| $f_{clk(max)}$                                                           | maximum clock frequency           |                                                                                    | 205   | -   | -     | MHz  |
| <b>Digital inputs: pins RXx0+, RXx0-, RXx1+, RXx1-, RXx2+, RXx2- [3]</b> |                                   |                                                                                    |       |     |       |      |
| $V_{I(dif)}$                                                             | differential input voltage        | $R_{RRX1} = 12\text{ k}\Omega \pm 1\%$ ;<br>$R_{RRX2} = 12\text{ k}\Omega \pm 1\%$ | 150   | -   | 1200  | mV   |
| $V_{I(cm)}$                                                              | common-mode input voltage         |                                                                                    | 2.735 | -   | 3.475 | V    |
| <b>I<sup>2</sup>C-bus: pins SCL and SDA [4]</b>                          |                                   |                                                                                    |       |     |       |      |
| $f_{SCL}$                                                                | SCL clock frequency               |                                                                                    | -     | -   | 400   | kHz  |
| $C_b$                                                                    | capacitive load for each bus line |                                                                                    | -     | -   | 400   | pF   |
| $C_i$                                                                    | capacitance for each I/O pin      |                                                                                    | -     | -   | 10    | pF   |
| <b>DDC I<sup>2</sup>C-bus: pins HSCLx, HSDAx [3][5]</b>                  |                                   |                                                                                    |       |     |       |      |
| $f_{SCL}$                                                                | SCL clock frequency               | Standard-mode                                                                      | -     | -   | 100   | kHz  |
|                                                                          |                                   | Fast-mode                                                                          | -     | -   | 400   | kHz  |
| $C_i$                                                                    | capacitance for each I/O pin      |                                                                                    | -     | -   | 10    | pF   |

- [1] At 30 % activity on video port output.
- [2] In high-impedance state, the output buffer is set to repeater mode recopying the input logic state with a small current. The output current changes from most negative to the most positive value at the triggering level which is internally set to  $V_{DDO(3V3)} / 2$  (e.g. the value of a pull-up or pull-down resistor must be lower than  $18\text{ k}\Omega$  to have a stable output value of  $V_{DDO(3V3)}$  or  $0\text{ V}$ ).
- [3] x = A, B, C or D.
- [4] Fast-mode, 5 V tolerant.
- [5] 5 V tolerant.



**Fig 5. Output timing diagram pin VCLK and pins VP[29:0]**



**Fig 6. Output timing diagram pin ACLK and pins AP[5:0]**

### 13. Output video port formats (mapping examples)

The following tables show examples of possible output formats that are enabled by the video port swap function in the driver.

**Table 11. Output in 12-bit video port format (mapping example 1)**

| Signal | YCbCr 4:2:2 semi-planar <sup>[1]</sup> |                     | YCbCr 4:2:2 ITU-R BT.656 <sup>[1]</sup> |                     |        |                     |
|--------|----------------------------------------|---------------------|-----------------------------------------|---------------------|--------|---------------------|
| VP[29] | Y <sub>0</sub> [11]                    | Y <sub>1</sub> [11] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[28] | Y <sub>0</sub> [10]                    | Y <sub>1</sub> [10] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[27] | Y <sub>0</sub> [9]                     | Y <sub>1</sub> [9]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[26] | Y <sub>0</sub> [8]                     | Y <sub>1</sub> [8]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[25] | Y <sub>0</sub> [7]                     | Y <sub>1</sub> [7]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[24] | Y <sub>0</sub> [6]                     | Y <sub>1</sub> [6]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[23] | Y <sub>0</sub> [5]                     | Y <sub>1</sub> [5]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[22] | Y <sub>0</sub> [4]                     | Y <sub>1</sub> [4]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[21] | Y <sub>0</sub> [3]                     | Y <sub>1</sub> [3]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[20] | Y <sub>0</sub> [2]                     | Y <sub>1</sub> [2]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[19] | Y <sub>0</sub> [1]                     | Y <sub>1</sub> [1]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[18] | Y <sub>0</sub> [0]                     | Y <sub>1</sub> [0]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[17] | Cb[11]                                 | Cr[11]              | Cb[11]                                  | Y <sub>0</sub> [11] | Cr[11] | Y <sub>1</sub> [11] |
| VP[16] | Cb[10]                                 | Cr[10]              | Cb[10]                                  | Y <sub>0</sub> [10] | Cr[10] | Y <sub>1</sub> [10] |
| VP[15] | Cb[9]                                  | Cr[9]               | Cb[9]                                   | Y <sub>0</sub> [9]  | Cr[9]  | Y <sub>1</sub> [9]  |
| VP[14] | Cb[8]                                  | Cr[8]               | Cb[8]                                   | Y <sub>0</sub> [8]  | Cr[8]  | Y <sub>1</sub> [8]  |
| VP[13] | Cb[7]                                  | Cr[7]               | Cb[7]                                   | Y <sub>0</sub> [7]  | Cr[7]  | Y <sub>1</sub> [7]  |
| VP[12] | Cb[6]                                  | Cr[6]               | Cb[6]                                   | Y <sub>0</sub> [6]  | Cr[6]  | Y <sub>1</sub> [6]  |
| VP[11] | Cb[5]                                  | Cr[5]               | Cb[5]                                   | Y <sub>0</sub> [5]  | Cr[5]  | Y <sub>1</sub> [5]  |
| VP[10] | Cb[4]                                  | Cr[4]               | Cb[4]                                   | Y <sub>0</sub> [4]  | Cr[4]  | Y <sub>1</sub> [4]  |
| VP[9]  | Cb[3]                                  | Cr[3]               | Cb[3]                                   | Y <sub>0</sub> [3]  | Cr[3]  | Y <sub>1</sub> [3]  |
| VP[8]  | Cb[2]                                  | Cr[2]               | Cb[2]                                   | Y <sub>0</sub> [2]  | Cr[2]  | Y <sub>1</sub> [2]  |
| VP[7]  | Cb[1]                                  | Cr[1]               | Cb[1]                                   | Y <sub>0</sub> [1]  | Cr[1]  | Y <sub>1</sub> [1]  |
| VP[6]  | Cb[0]                                  | Cr[0]               | Cb[0]                                   | Y <sub>0</sub> [0]  | Cr[0]  | Y <sub>1</sub> [0]  |
| VP[5]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[4]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[3]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[2]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[1]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[0]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |

[1] Z = high-impedance; L = LOW-level; depending on the driver configuration.

Table 12. Output in 12-bit video port format (mapping example 2)

| Signal | YCbCr 4:2:2 semi-planar <sup>[1]</sup> |                     | YCbCr 4:2:2 ITU-R BT.656 <sup>[1]</sup> |                     |        |                     |
|--------|----------------------------------------|---------------------|-----------------------------------------|---------------------|--------|---------------------|
| VP[29] | Cb[11]                                 | Cr[11]              | Cb[11]                                  | Y <sub>0</sub> [11] | Cr[11] | Y <sub>1</sub> [11] |
| VP[28] | Cb[10]                                 | Cr[10]              | Cb[10]                                  | Y <sub>0</sub> [10] | Cr[10] | Y <sub>1</sub> [10] |
| VP[27] | Cb[9]                                  | Cr[9]               | Cb[9]                                   | Y <sub>0</sub> [9]  | Cr[9]  | Y <sub>1</sub> [9]  |
| VP[26] | Cb[8]                                  | Cr[8]               | Cb[8]                                   | Y <sub>0</sub> [8]  | Cr[8]  | Y <sub>1</sub> [8]  |
| VP[25] | Cb[7]                                  | Cr[7]               | Cb[7]                                   | Y <sub>0</sub> [7]  | Cr[7]  | Y <sub>1</sub> [7]  |
| VP[24] | Cb[6]                                  | Cr[6]               | Cb[6]                                   | Y <sub>0</sub> [6]  | Cr[6]  | Y <sub>1</sub> [6]  |
| VP[23] | Cb[5]                                  | Cr[5]               | Cb[5]                                   | Y <sub>0</sub> [5]  | Cr[5]  | Y <sub>1</sub> [5]  |
| VP[22] | Cb[4]                                  | Cr[4]               | Cb[4]                                   | Y <sub>0</sub> [4]  | Cr[4]  | Y <sub>1</sub> [4]  |
| VP[21] | Cb[3]                                  | Cr[3]               | Cb[3]                                   | Y <sub>0</sub> [3]  | Cr[3]  | Y <sub>1</sub> [3]  |
| VP[20] | Cb[2]                                  | Cr[2]               | Cb[2]                                   | Y <sub>0</sub> [2]  | Cr[2]  | Y <sub>1</sub> [2]  |
| VP[19] | Cb[1]                                  | Cr[1]               | Cb[1]                                   | Y <sub>0</sub> [1]  | Cr[1]  | Y <sub>1</sub> [1]  |
| VP[18] | Cb[0]                                  | Cr[0]               | Cb[0]                                   | Y <sub>0</sub> [0]  | Cr[0]  | Y <sub>1</sub> [0]  |
| VP[17] | Y <sub>0</sub> [11]                    | Y <sub>1</sub> [11] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[16] | Y <sub>0</sub> [10]                    | Y <sub>1</sub> [10] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[15] | Y <sub>0</sub> [9]                     | Y <sub>1</sub> [9]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[14] | Y <sub>0</sub> [8]                     | Y <sub>1</sub> [8]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[13] | Y <sub>0</sub> [7]                     | Y <sub>1</sub> [7]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[12] | Y <sub>0</sub> [6]                     | Y <sub>1</sub> [6]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[11] | Y <sub>0</sub> [5]                     | Y <sub>1</sub> [5]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[10] | Y <sub>0</sub> [4]                     | Y <sub>1</sub> [4]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[9]  | Y <sub>0</sub> [3]                     | Y <sub>1</sub> [3]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[8]  | Y <sub>0</sub> [2]                     | Y <sub>1</sub> [2]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[7]  | Y <sub>0</sub> [1]                     | Y <sub>1</sub> [1]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[6]  | Y <sub>0</sub> [0]                     | Y <sub>1</sub> [0]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[5]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[4]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[3]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[2]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[1]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[0]  | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |

[1] Z = high-impedance; L = LOW-level; depending on the driver configuration.

Table 13. Output in 10-bit video port format (mapping example 1)

| Signal | RGB   | YCbCr 4:4:4 | YCbCr 4:2:2 semi-planar <sup>[1]</sup> |                     | YCbCr 4:2:2 ITU-R BT.656 <sup>[1]</sup> |                     |        |                     |
|--------|-------|-------------|----------------------------------------|---------------------|-----------------------------------------|---------------------|--------|---------------------|
| VP[29] | G[11] | Y[11]       | Y <sub>0</sub> [11]                    | Y <sub>1</sub> [11] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[28] | G[10] | Y[10]       | Y <sub>0</sub> [10]                    | Y <sub>1</sub> [10] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[27] | G[9]  | Y[9]        | Y <sub>0</sub> [9]                     | Y <sub>1</sub> [9]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[26] | G[8]  | Y[8]        | Y <sub>0</sub> [8]                     | Y <sub>1</sub> [8]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[25] | G[7]  | Y[7]        | Y <sub>0</sub> [7]                     | Y <sub>1</sub> [7]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[24] | G[6]  | Y[6]        | Y <sub>0</sub> [6]                     | Y <sub>1</sub> [6]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[23] | G[5]  | Y[5]        | Y <sub>0</sub> [5]                     | Y <sub>1</sub> [5]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[22] | G[4]  | Y[4]        | Y <sub>0</sub> [4]                     | Y <sub>1</sub> [4]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[21] | G[3]  | Y[3]        | Y <sub>0</sub> [3]                     | Y <sub>1</sub> [3]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[20] | G[2]  | Y[2]        | Y <sub>0</sub> [2]                     | Y <sub>1</sub> [2]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[19] | R[11] | Cr[11]      | Cb[11]                                 | Cr[11]              | Cb[11]                                  | Y <sub>0</sub> [11] | Cr[11] | Y <sub>1</sub> [11] |
| VP[18] | R[10] | Cr[10]      | Cb[10]                                 | Cr[10]              | Cb[10]                                  | Y <sub>0</sub> [10] | Cr[10] | Y <sub>1</sub> [10] |
| VP[17] | R[9]  | Cr[9]       | Cb[9]                                  | Cr[9]               | Cb[9]                                   | Y <sub>0</sub> [9]  | Cr[9]  | Y <sub>1</sub> [9]  |
| VP[16] | R[8]  | Cr[8]       | Cb[8]                                  | Cr[8]               | Cb[8]                                   | Y <sub>0</sub> [8]  | Cr[8]  | Y <sub>1</sub> [8]  |
| VP[15] | R[7]  | Cr[7]       | Cb[7]                                  | Cr[7]               | Cb[7]                                   | Y <sub>0</sub> [7]  | Cr[7]  | Y <sub>1</sub> [7]  |
| VP[14] | R[6]  | Cr[6]       | Cb[6]                                  | Cr[6]               | Cb[6]                                   | Y <sub>0</sub> [6]  | Cr[6]  | Y <sub>1</sub> [6]  |
| VP[13] | R[5]  | Cr[5]       | Cb[5]                                  | Cr[5]               | Cb[5]                                   | Y <sub>0</sub> [5]  | Cr[5]  | Y <sub>1</sub> [5]  |
| VP[12] | R[4]  | Cr[4]       | Cb[4]                                  | Cr[4]               | Cb[4]                                   | Y <sub>0</sub> [4]  | Cr[4]  | Y <sub>1</sub> [4]  |
| VP[11] | R[3]  | Cr[3]       | Cb[3]                                  | Cr[3]               | Cb[3]                                   | Y <sub>0</sub> [3]  | Cr[3]  | Y <sub>1</sub> [3]  |
| VP[10] | R[2]  | Cr[2]       | Cb[2]                                  | Cr[2]               | Cb[2]                                   | Y <sub>0</sub> [2]  | Cr[2]  | Y <sub>1</sub> [2]  |
| VP[9]  | B[11] | Cb[11]      | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[8]  | B[10] | Cb[10]      | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[7]  | B[9]  | Cb[9]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[6]  | B[8]  | Cb[8]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[5]  | B[7]  | Cb[7]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[4]  | B[6]  | Cb[6]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[3]  | B[5]  | Cb[5]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[2]  | B[4]  | Cb[4]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[1]  | B[3]  | Cb[3]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[0]  | B[2]  | Cb[2]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |

[1] Z = high-impedance; L = LOW-level; depending on the driver configuration.

Table 14. Output in 10-bit video port format (mapping example 2)

| Signal | RGB   | YCbCr 4:4:4 | YCbCr 4:2:2 semi-planar <sup>[1]</sup> |                     | YCbCr 4:2:2 ITU-R BT.656 <sup>[1]</sup> |                     |        |                     |
|--------|-------|-------------|----------------------------------------|---------------------|-----------------------------------------|---------------------|--------|---------------------|
| VP[29] | B[11] | Cb[11]      | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[28] | B[10] | Cb[10]      | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[27] | B[9]  | Cb[9]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[26] | B[8]  | Cb[8]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[25] | B[7]  | Cb[7]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[24] | B[6]  | Cb[6]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[23] | B[5]  | Cb[5]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[22] | B[4]  | Cb[4]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[21] | B[3]  | Cb[3]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[20] | B[2]  | Cb[2]       | Z/L                                    | Z/L                 | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[19] | G[11] | Y[11]       | Y <sub>0</sub> [11]                    | Y <sub>1</sub> [11] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[18] | G[10] | Y[10]       | Y <sub>0</sub> [10]                    | Y <sub>1</sub> [10] | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[17] | G[9]  | Y[9]        | Y <sub>0</sub> [9]                     | Y <sub>1</sub> [9]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[16] | G[8]  | Y[8]        | Y <sub>0</sub> [8]                     | Y <sub>1</sub> [8]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[15] | G[7]  | Y[7]        | Y <sub>0</sub> [7]                     | Y <sub>1</sub> [7]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[14] | G[6]  | Y[6]        | Y <sub>0</sub> [6]                     | Y <sub>1</sub> [6]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[13] | G[5]  | Y[5]        | Y <sub>0</sub> [5]                     | Y <sub>1</sub> [5]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[12] | G[4]  | Y[4]        | Y <sub>0</sub> [4]                     | Y <sub>1</sub> [4]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[11] | G[3]  | Y[3]        | Y <sub>0</sub> [3]                     | Y <sub>1</sub> [3]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[10] | G[2]  | Y[2]        | Y <sub>0</sub> [2]                     | Y <sub>1</sub> [2]  | Z/L                                     | Z/L                 | Z/L    | Z/L                 |
| VP[9]  | R[11] | Cr[11]      | Cb[11]                                 | Cr[11]              | Cb[11]                                  | Y <sub>0</sub> [11] | Cr[11] | Y <sub>1</sub> [11] |
| VP[8]  | R[10] | Cr[10]      | Cb[10]                                 | Cr[10]              | Cb[10]                                  | Y <sub>0</sub> [10] | Cr[10] | Y <sub>1</sub> [10] |
| VP[7]  | R[9]  | Cr[9]       | Cb[9]                                  | Cr[9]               | Cb[9]                                   | Y <sub>0</sub> [9]  | Cr[9]  | Y <sub>1</sub> [9]  |
| VP[6]  | R[8]  | Cr[8]       | Cb[8]                                  | Cr[8]               | Cb[8]                                   | Y <sub>0</sub> [8]  | Cr[8]  | Y <sub>1</sub> [8]  |
| VP[5]  | R[7]  | Cr[7]       | Cb[7]                                  | Cr[7]               | Cb[7]                                   | Y <sub>0</sub> [7]  | Cr[7]  | Y <sub>1</sub> [7]  |
| VP[4]  | R[6]  | Cr[6]       | Cb[6]                                  | Cr[6]               | Cb[6]                                   | Y <sub>0</sub> [6]  | Cr[6]  | Y <sub>1</sub> [6]  |
| VP[3]  | R[5]  | Cr[5]       | Cb[5]                                  | Cr[5]               | Cb[5]                                   | Y <sub>0</sub> [5]  | Cr[5]  | Y <sub>1</sub> [5]  |
| VP[2]  | R[4]  | Cr[4]       | Cb[4]                                  | Cr[4]               | Cb[4]                                   | Y <sub>0</sub> [4]  | Cr[4]  | Y <sub>1</sub> [4]  |
| VP[1]  | R[3]  | Cr[3]       | Cb[3]                                  | Cr[3]               | Cb[3]                                   | Y <sub>0</sub> [3]  | Cr[3]  | Y <sub>1</sub> [3]  |
| VP[0]  | R[2]  | Cr[2]       | Cb[2]                                  | Cr[2]               | Cb[2]                                   | Y <sub>0</sub> [2]  | Cr[2]  | Y <sub>1</sub> [2]  |

[1] Z = high-impedance; L = LOW-level; depending on the driver configuration.

Table 15. Output in 8-bit video port format (mapping example 1)

| Signal | RGB   | YCbCr 4:4:4 <sup>[1]</sup> | YCbCr 4:2:2 semi-planar <sup>[1]</sup> | YCbCr 4:2:2 ITU-R BT.656 <sup>[1]</sup> |        |                     |        |                     |
|--------|-------|----------------------------|----------------------------------------|-----------------------------------------|--------|---------------------|--------|---------------------|
| VP[29] | G[11] | Y[11]                      | Y <sub>0</sub> [11]                    | Y <sub>1</sub> [11]                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[28] | G[10] | Y[10]                      | Y <sub>0</sub> [10]                    | Y <sub>1</sub> [10]                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[27] | G[9]  | Y[9]                       | Y <sub>0</sub> [9]                     | Y <sub>1</sub> [9]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[26] | G[8]  | Y[8]                       | Y <sub>0</sub> [8]                     | Y <sub>1</sub> [8]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[25] | G[7]  | Y[7]                       | Y <sub>0</sub> [7]                     | Y <sub>1</sub> [7]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[24] | G[6]  | Y[6]                       | Y <sub>0</sub> [6]                     | Y <sub>1</sub> [6]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[23] | G[5]  | Y[5]                       | Y <sub>0</sub> [5]                     | Y <sub>1</sub> [5]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[22] | G[4]  | Y[4]                       | Y <sub>0</sub> [4]                     | Y <sub>1</sub> [4]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[21] | R[11] | Cr[11]                     | Cb[11]                                 | Cr[11]                                  | Cb[11] | Y <sub>0</sub> [11] | Cr[11] | Y <sub>1</sub> [11] |
| VP[20] | R[10] | Cr[10]                     | Cb[10]                                 | Cr[10]                                  | Cb[10] | Y <sub>0</sub> [10] | Cr[10] | Y <sub>1</sub> [10] |
| VP[19] | R[9]  | Cr[9]                      | Cb[9]                                  | Cr[9]                                   | Cb[9]  | Y <sub>0</sub> [9]  | Cr[9]  | Y <sub>1</sub> [9]  |
| VP[18] | R[8]  | Cr[8]                      | Cb[8]                                  | Cr[8]                                   | Cb[8]  | Y <sub>0</sub> [8]  | Cr[8]  | Y <sub>1</sub> [8]  |
| VP[17] | R[7]  | Cr[7]                      | Cb[7]                                  | Cr[7]                                   | Cb[7]  | Y <sub>0</sub> [7]  | Cr[7]  | Y <sub>1</sub> [7]  |
| VP[16] | R[6]  | Cr[6]                      | Cb[6]                                  | Cr[6]                                   | Cb[6]  | Y <sub>0</sub> [6]  | Cr[6]  | Y <sub>1</sub> [6]  |
| VP[15] | R[5]  | Cr[5]                      | Cb[5]                                  | Cr[5]                                   | Cb[5]  | Y <sub>0</sub> [5]  | Cr[5]  | Y <sub>1</sub> [5]  |
| VP[14] | R[4]  | Cr[4]                      | Cb[4]                                  | Cr[4]                                   | Cb[4]  | Y <sub>0</sub> [4]  | Cr[4]  | Y <sub>1</sub> [4]  |
| VP[13] | B[11] | Cb[11]                     | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[12] | B[10] | Cb[10]                     | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[11] | B[9]  | Cb[9]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[10] | B[8]  | Cb[8]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[9]  | B[7]  | Cb[7]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[8]  | B[6]  | Cb[6]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[7]  | B[5]  | Cb[5]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[6]  | B[4]  | Cb[4]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[5]  | Z/L   | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[4]  | Z/L   | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[3]  | Z/L   | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[2]  | Z/L   | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[1]  | Z/L   | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[0]  | Z/L   | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |

[1] Z = high-impedance; L = LOW-level; depending on the driver configuration.



Table 16. Output in 8-bit video port format (mapping example 2)

| Signal | RGB <sup>[1]</sup> | YCbCr 4:4:4 <sup>[1]</sup> | YCbCr 4:2:2 semi-planar <sup>[1]</sup> | YCbCr 4:2:2 ITU-R BT.656 <sup>[1]</sup> |        |                     |        |                     |
|--------|--------------------|----------------------------|----------------------------------------|-----------------------------------------|--------|---------------------|--------|---------------------|
| VP[29] | B[11]              | Cb[11]                     | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[28] | B[10]              | Cb[10]                     | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[27] | B[9]               | Cb[9]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[26] | B[8]               | Cb[8]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[25] | B[7]               | Cb[7]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[24] | B[6]               | Cb[6]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[23] | B[5]               | Cb[5]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[22] | B[4]               | Cb[4]                      | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[21] | G[11]              | Y[11]                      | Y <sub>0</sub> [11]                    | Y <sub>1</sub> [11]                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[20] | G[10]              | Y[10]                      | Y <sub>0</sub> [10]                    | Y <sub>1</sub> [10]                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[19] | G[9]               | Y[9]                       | Y <sub>0</sub> [9]                     | Y <sub>1</sub> [9]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[18] | G[8]               | Y[8]                       | Y <sub>0</sub> [8]                     | Y <sub>1</sub> [8]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[17] | G[7]               | Y[7]                       | Y <sub>0</sub> [7]                     | Y <sub>1</sub> [7]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[16] | G[6]               | Y[6]                       | Y <sub>0</sub> [6]                     | Y <sub>1</sub> [6]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[15] | G[5]               | Y[5]                       | Y <sub>0</sub> [5]                     | Y <sub>1</sub> [5]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[14] | G[4]               | Y[4]                       | Y <sub>0</sub> [4]                     | Y <sub>1</sub> [4]                      | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[13] | R[11]              | Cr[11]                     | Cb[11]                                 | Cr[11]                                  | Cb[11] | Y <sub>0</sub> [11] | Cr[11] | Y <sub>1</sub> [11] |
| VP[12] | R[10]              | Cr[10]                     | Cb[10]                                 | Cr[10]                                  | Cb[10] | Y <sub>0</sub> [10] | Cr[10] | Y <sub>1</sub> [10] |
| VP[11] | R[9]               | Cr[9]                      | Cb[9]                                  | Cr[9]                                   | Cb[9]  | Y <sub>0</sub> [9]  | Cr[9]  | Y <sub>1</sub> [9]  |
| VP[10] | R[8]               | Cr[8]                      | Cb[8]                                  | Cr[8]                                   | Cb[8]  | Y <sub>0</sub> [8]  | Cr[8]  | Y <sub>1</sub> [8]  |
| VP[9]  | R[7]               | Cr[7]                      | Cb[7]                                  | Cr[7]                                   | Cb[7]  | Y <sub>0</sub> [7]  | Cr[7]  | Y <sub>1</sub> [7]  |
| VP[8]  | R[6]               | Cr[6]                      | Cb[6]                                  | Cr[6]                                   | Cb[6]  | Y <sub>0</sub> [6]  | Cr[6]  | Y <sub>1</sub> [6]  |
| VP[7]  | R[5]               | Cr[5]                      | Cb[5]                                  | Cr[5]                                   | Cb[5]  | Y <sub>0</sub> [5]  | Cr[5]  | Y <sub>1</sub> [5]  |
| VP[6]  | R[4]               | Cr[4]                      | Cb[4]                                  | Cr[4]                                   | Cb[4]  | Y <sub>0</sub> [4]  | Cr[4]  | Y <sub>1</sub> [4]  |
| VP[5]  | Z/L                | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[4]  | Z/L                | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[3]  | Z/L                | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[2]  | Z/L                | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[1]  | Z/L                | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |
| VP[0]  | Z/L                | Z/L                        | Z/L                                    | Z/L                                     | Z/L    | Z/L                 | Z/L    | Z/L                 |

[1] Z = high-impedance; L = LOW-level; depending on the driver configuration.

## 14. Example of supported video formats

Table 17. Example of supported video formats

| Standard            | Format                               | Total pixels × total lines | Horizontal rate (kHz) | Pixel clock rate (MHz) <sup>[1]</sup> |
|---------------------|--------------------------------------|----------------------------|-----------------------|---------------------------------------|
| 576i <sup>[2]</sup> | 1440 × 576i 50 Hz                    | 1728 × 625                 | 15.750                | 27.000 <sup>[3]</sup>                 |
| 480i <sup>[4]</sup> | 1440 × 480i 59.94 Hz                 | 1716 × 525                 | 15.734                | 27.000 <sup>[3]</sup>                 |
|                     | 1440 × 480i 60 Hz                    | 1716 × 525                 | 15.750                | 27.027 <sup>[3]</sup>                 |
| 576p                | 720 × 576p 50 Hz                     | 864 × 625                  | 31.250                | 27.000                                |
| 480p                | 720 × 480p 59.94 Hz                  | 858 × 525                  | 31.469                | 27.000                                |
|                     | 720 × 480p 60 Hz                     | 858 × 525                  | 31.500                | 27.027                                |
| 720p                | 1280 × 720p 50 Hz                    | 1980 × 750                 | 37.500                | 74.250                                |
|                     | 1280 × 720p 59.94 Hz                 | 1650 × 750                 | 44.955                | 74.176                                |
|                     | 1280 × 720p 60 Hz                    | 1650 × 750                 | 45.000                | 74.250                                |
| 1080i               | 1920 × 1080i 50 Hz                   | 2640 × 1125                | 28.125                | 74.250                                |
|                     | 1920 × 1080i 59.94 Hz                | 2200 × 1125                | 33.716                | 74.176                                |
|                     | 1920 × 1080i 60 Hz                   | 2200 × 1125                | 33.750                | 74.250                                |
| 1080p               | 1920 × 1080p 50 Hz <sup>[5]</sup>    | 2640 × 1125                | 56.250                | 148.500                               |
|                     | 1920 × 1080p 59.94 Hz <sup>[5]</sup> | 2200 × 1125                | 67.433                | 148.352                               |
|                     | 1920 × 1080p 60 Hz <sup>[5]</sup>    | 2200 × 1125                | 67.500                | 148.500                               |
| 0.31M3 VGA          | 640 × 480p 60 Hz                     | 800 × 525                  | 31.469                | 25.175                                |
|                     | 640 × 480p 72 Hz                     | 832 × 520                  | 37.861                | 31.500                                |
|                     | 640 × 480p 75 Hz                     | 840 × 500                  | 37.500                | 31.500                                |
|                     | 640 × 480p 85 Hz                     | 832 × 509                  | 43.269                | 36.000                                |
| 0.48M3 SVGA         | 800 × 600p 56 Hz                     | 1024 × 625                 | 35.156                | 36.000                                |
|                     | 800 × 600p 60 Hz                     | 1056 × 628                 | 37.879                | 40.000                                |
|                     | 800 × 600p 72 Hz                     | 1040 × 666                 | 48.077                | 50.000                                |
|                     | 800 × 600p 75 Hz                     | 1056 × 625                 | 46.875                | 49.500                                |
|                     | 800 × 600p 85 Hz                     | 1048 × 631                 | 53.674                | 56.250                                |
| 0.48M3-R            | 800 × 600p 120 Hz                    | 960 × 636                  | 76.302                | 73.250                                |
| 0.41M9              | 848 × 480p 60 Hz                     | 1088 × 517                 | 31.020                | 33.750                                |
| 0.79M3 XGA          | 1024 × 768p 43 Hz                    | 1264 × 817                 | 35.522                | 44.900                                |
|                     | 1024 × 768p 60 Hz                    | 1344 × 806                 | 48.363                | 65.000                                |
|                     | 1024 × 768p 70 Hz                    | 1328 × 806                 | 56.476                | 75.000                                |
|                     | 1024 × 768p 75 Hz                    | 1312 × 800                 | 60.023                | 78.750                                |
|                     | 1024 × 768p 85 Hz                    | 1376 × 808                 | 68.677                | 94.500                                |
| 0.79M3-R XGA        | 1024 × 768p 120 Hz                   | 1184 × 813                 | 97.551                | 115.500                               |
| 1.00M3              | 1152 × 864p 75 Hz                    | 1600 × 900                 | 67.500                | 108.000                               |
| 0.98M9-R            | 1280 × 768p 60 Hz                    | 1440 × 790                 | 47.396                | 68.250                                |
|                     | 1280 × 768p 120 Hz <sup>[5]</sup>    | 1440 × 813                 | 97.396                | 140.250                               |
| 0.98M9              | 1280 × 768p 60 Hz                    | 1664 × 798                 | 47.776                | 79.500                                |
|                     | 1280 × 768p 75 Hz                    | 1696 × 805                 | 60.289                | 102.250                               |
|                     | 1280 × 768p 85 Hz                    | 1712 × 809                 | 68.633                | 117.500                               |

Table 17. Example of supported video formats ...continued

| Standard                | Format                            | Total pixels × total lines | Horizontal rate (kHz) | Pixel clock rate (MHz) <sup>[1]</sup> |
|-------------------------|-----------------------------------|----------------------------|-----------------------|---------------------------------------|
| 1.02MA-R                | 1280 × 800p 60 Hz                 | 1440 × 823                 | 49.306                | 71.000                                |
|                         | 1280 × 800p 120 Hz <sup>[5]</sup> | 1440 × 847                 | 101.563               | 146.250                               |
| 1.02MA                  | 1280 × 800p 60 Hz                 | 1680 × 831                 | 49.702                | 83.500                                |
|                         | 1280 × 800p 75 Hz                 | 1696 × 838                 | 62.795                | 106.500                               |
|                         | 1280 × 800p 85 Hz                 | 1712 × 843                 | 71.554                | 122.500                               |
| 1.23M3                  | 1280 × 960p 60 Hz                 | 1800 × 1000                | 60.000                | 108.000                               |
|                         | 1280 × 960p 85 Hz <sup>[5]</sup>  | 1728 × 1011                | 85.938                | 148.500                               |
| 1.31M4 SXGA             | 1280 × 1024p 60 Hz                | 1688 × 1066                | 63.981                | 108.000                               |
|                         | 1280 × 1024p 75 Hz                | 1688 × 1066                | 79.976                | 135.000                               |
|                         | 1280 × 1024p 85 Hz <sup>[5]</sup> | 1728 × 1072                | 91.146                | 157.500                               |
| 1.04M9                  | 1360 × 768p 60 Hz                 | 1792 × 795                 | 47.712                | 85.500                                |
| 1.04M9-R                | 1360 × 768p 120 Hz <sup>[5]</sup> | 1520 × 813                 | 97.533                | 148.250                               |
| 1.47M3-R                | 1400 × 1050p 60 Hz                | 1560 × 1080                | 64.744                | 101.000                               |
| 1.47M3                  | 1400 × 1050p 60 Hz                | 1864 × 1089                | 65.317                | 121.750                               |
|                         | 1400 × 1050p 75 Hz <sup>[5]</sup> | 1896 × 1099                | 82.278                | 156.000                               |
| 1.29MA-R                | 1440 × 900p 60 Hz                 | 1600 × 926                 | 55.469                | 88.750                                |
| 1.29MA                  | 1440 × 900p 60 Hz                 | 1904 × 934                 | 55.935                | 106.500                               |
|                         | 1440 × 900p 75 Hz <sup>[5]</sup>  | 1936 × 942                 | 70.635                | 136.750                               |
|                         | 1440 × 900p 85 Hz <sup>[5]</sup>  | 1952 × 948                 | 80.430                | 157.000                               |
| 1.92M3 UXGA             | 1600 × 1200p 60 Hz <sup>[5]</sup> | 2160 × 1250                | 75.000                | 162.000                               |
| 1.76MA-R                | 1680 × 1050p 60 Hz                | 1840 × 1080                | 64.674                | 119.000                               |
| 1.76MA                  | 1680 × 1050p 60 Hz <sup>[5]</sup> | 2240 × 1089                | 65.290                | 146.250                               |
| 2.30MA-R <sup>[6]</sup> | 1920 × 1200p 60 Hz <sup>[5]</sup> | 2080 × 1235                | 74.038                | 154.000                               |

[1] Pixel clock rate corresponds to VCLK output for 4:4:4 format and 4:2:2 semi-planar; VCLK / 2 for 4:2:2 ITU-R BT.656 format. The pixel clock rate can be determined by:

- a) Total pixels × total lines × frame rate for the progressive format.
- b) Total pixels × total lines × frame rate / 2 for the interlaced format.

[2] Also referred to as PAL (Phase Alternating Line).

[3] Pixel-doubling.

[4] Also referred to as NTSC (National Television Standards Committee).

[5] Only supports Deep Color mode 10-bit.

[6] Sometimes also referred to as WUXGA (Wide Ultra eXtended Graphics Array).

15. Application information

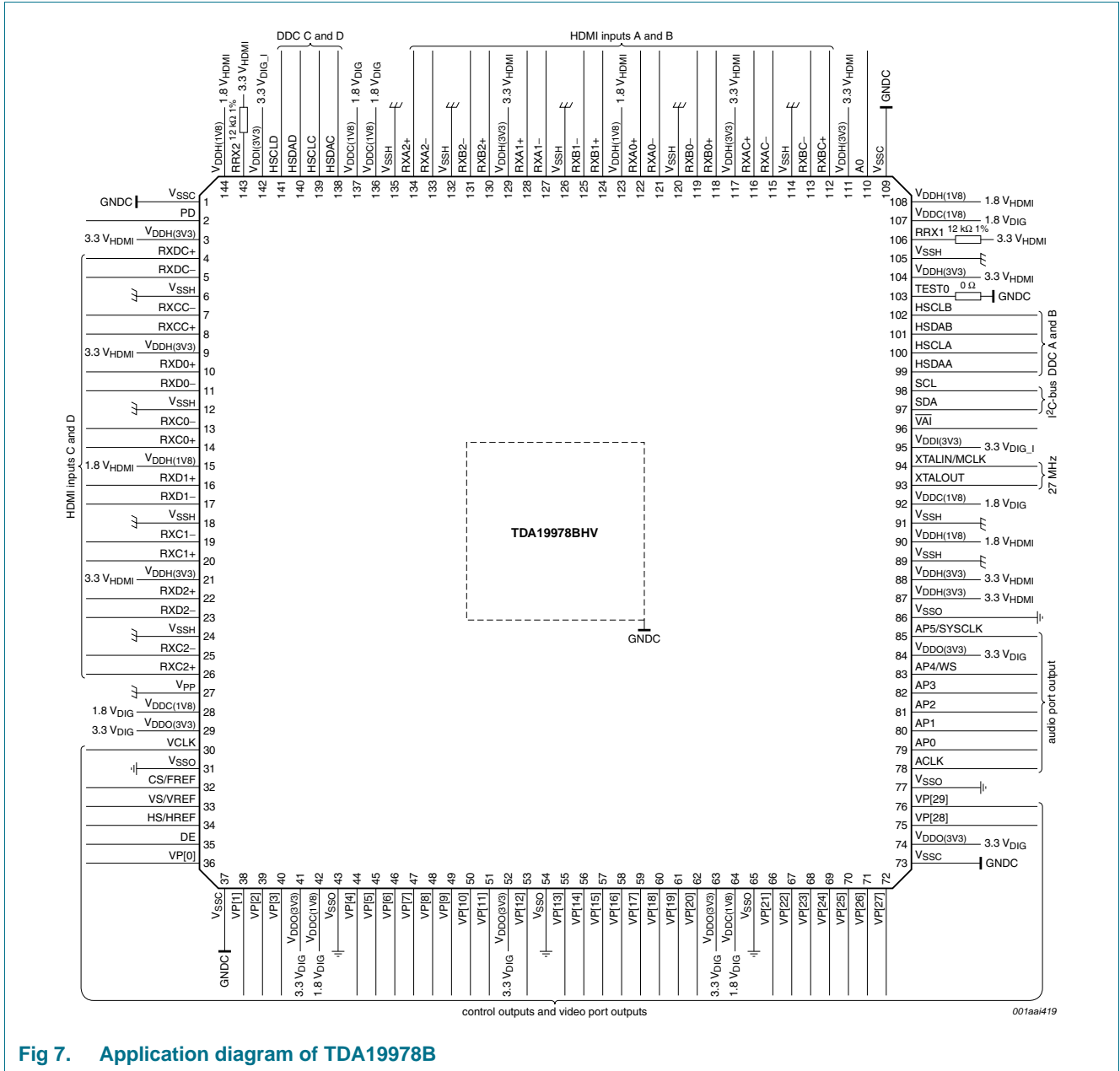


Fig 7. Application diagram of TDA19978B

16. Package outline

HLQFP144: plastic thermal enhanced low profile quad flat package; 144 leads;  
body 20 x 20 x 1.4 mm; exposed die pad

SOT612-3

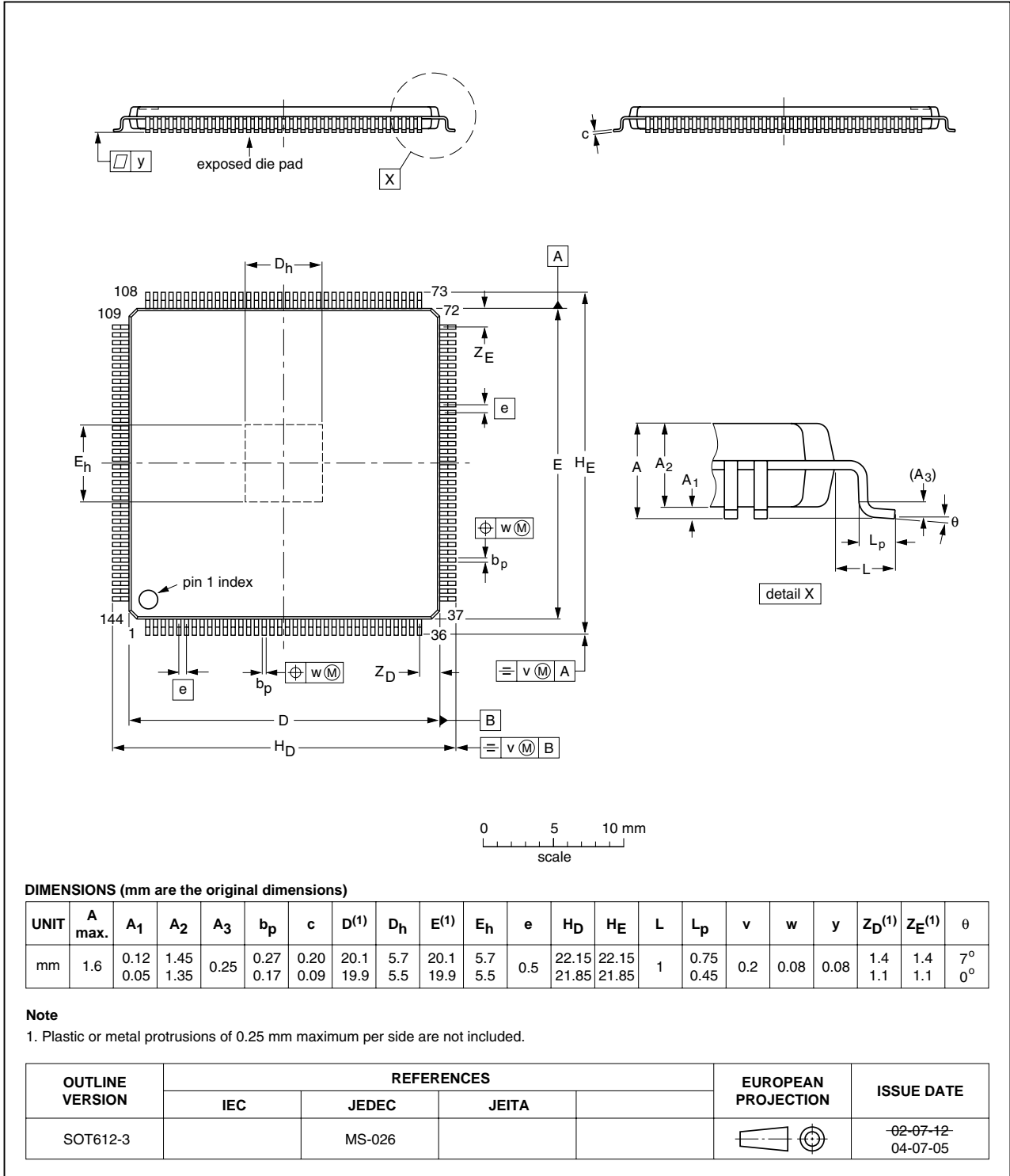


Fig 8. Package outline SOT612-3 (HLQFP144)

## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 9](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 18](#) and [19](#)

**Table 18. SnPb eutectic process (from J-STD-020C)**

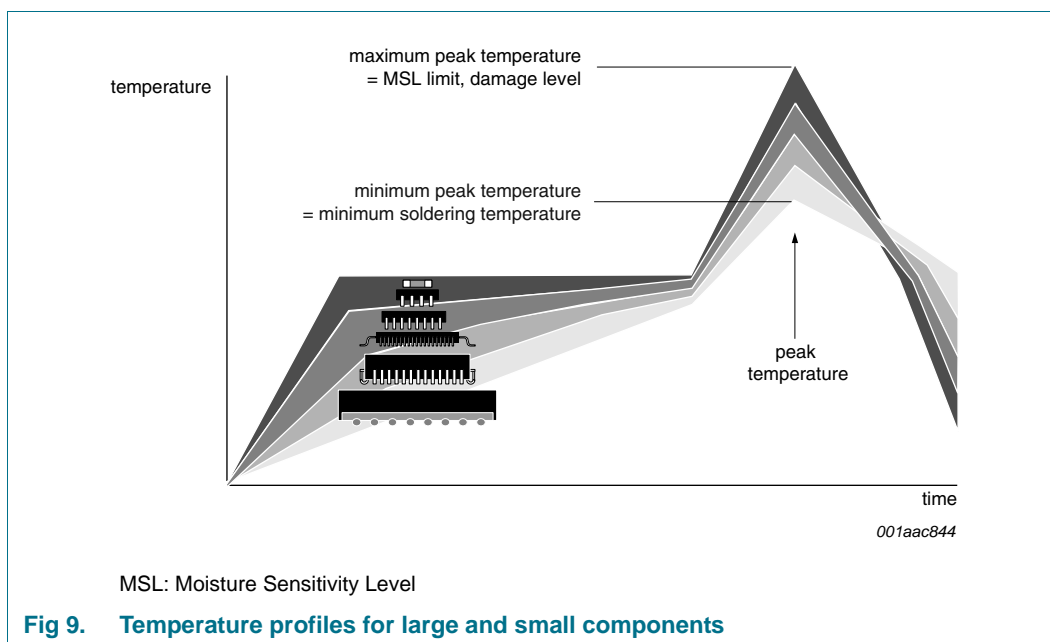
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 19. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 9](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 18. Abbreviations

**Table 20. Abbreviations**

| Acronym | Description                               |
|---------|-------------------------------------------|
| ACR     | Audio Clock Regeneration                  |
| AVR     | Audio Video Receiver                      |
| AWG     | American Wire Gauge                       |
| CMOS    | Complementary Metal Oxide Semiconductor   |
| DAC     | Digital-to-Analog Converter               |
| DDC-bus | Display Data Channel bus                  |
| DSD     | Direct Stream Digital                     |
| DST     | Direct Stream Transfer                    |
| DTS-HD  | Digital Theater Systems High-Definition   |
| DVD     | Digital Versatile Disc                    |
| DVI     | Digital Video Interface                   |
| EDID    | Extended Display Identification Data      |
| HBM     | Human Body Model                          |
| HBR     | High Bit Rate                             |
| HD      | High-Definition                           |
| HDCP    | High-bandwidth Digital Content Protection |
| HDMI    | High-Definition Multimedia Interface      |
| HDTV    | High-Definition TeleVision                |
| L-PCM   | Linear-Pulse Code Modulation              |



Table 20. Abbreviations ...continued

| Acronym | Description                                      |
|---------|--------------------------------------------------|
| LSB     | Least Significant Bit                            |
| LV-TTL  | Low Voltage Transistor-Transistor Logic          |
| NTSC    | National Television Standards Committee          |
| OBA     | One Bit Audio                                    |
| OTP     | One Time Programmable                            |
| PAL     | Phase Alternating Line                           |
| PLL     | Phase-Locked Loop                                |
| RGB     | Red Green Blue                                   |
| SACD    | Super Audio CD                                   |
| SVGA    | Super Video Graphics Array                       |
| SXGA    | Super eXtended Graphics Array                    |
| S/PDIF  | Sony/Philips Digital Interface Format            |
| TMDS    | Transition Minimized Differential Signaling      |
| UXGA    | Ultra eXtended Graphics Array                    |
| VGA     | Video Graphics Array                             |
| WUXGA   | Wide Ultra eXtended Graphics Array               |
| XGA     | eXtended Graphics Array                          |
| YCbCr   | Y = Luminance, Cb = Chroma blue, Cr = Chroma red |
| YUV     | Y = Luminance, U and V are chrominance signals   |

## 19. Revision history

Table 21. Revision history

| Document ID    | Release date | Data sheet status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Change notice | Supersedes  |
|----------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------|
| TDA19978B_2    | 20100510     | Product data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -             | TDA19978B_1 |
| Modifications: |              | <ul style="list-style-type: none"> <li>• <a href="#">Section 1 "General description"</a>: replaced 2.25 gigasamples per second by 2.05 gigasamples per second</li> <li>• <a href="#">Section 1 "General description"</a>: updated the Deep Color mode in 12-bit</li> <li>• <a href="#">Section 2 "Features and benefits"</a>: replaced 225 MHz by 205 MHz</li> <li>• <a href="#">Table 1 "Quick reference data"</a>: updated</li> <li>• <a href="#">Section 8.5 "Activity detection"</a>: replaced 225 MHz by 205 MHz</li> <li>• <a href="#">Table 10 "Characteristics"</a>: updated</li> <li>• <a href="#">Table 17 "Example of supported video formats"</a>: updated</li> </ul> |               |             |
| TDA19978B_1    | 20080807     | Product data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -             | -           |

## 20. Legal information

### 20.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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