DATA SHEET

ELPIDA

MOS INTEGRATED CIRCUIT

MC-45V8AB642KS

8M-WORD BY 64-BIT VirtualChannel™ DYNAMIC RAM MODULE (SO DIMM)

Description

The MC-45V8AB642KS is a 8,388,608 words by 64 bits VirtualChannel dynamic RAM module (small outline DIMM) on which 4 pieces of 128M VirtualChannel DRAM : μPD45V128161 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 64 bits organization
- Clock frequency and access time from CLK

Part number	Read latency	Clock frequency MHz (MAX.)	Access time from CLK ns (MAX.)	Maximum supply current mA				
				Operating			Refresh	
				Prefetch	Restore	Channel read / write (Burst)	Auto	Self
MC-45V8AB642KS-A75	2	133	5.4	600		300	920	8

- Fully Standard Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by BA0 (Bank Select)
- Programmable wrap sequence (interleave)
- Programmable burst length (4)
- Read latency (2)
- Prefetch read latency (4)
- Auto precharge and without auto precharge
- Auto refresh and self refresh
- Single 3.3 V ± 0.3 V power supply
- Interface: LVTTL
- Refresh cycle: 4K cycles/64 ms
- 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

Document No. E0028N11 (Ver. 1.1)
(Previous No. M15239EJ1V0DS00)
Date Published April 2001 CP (K)
Printed in Japan

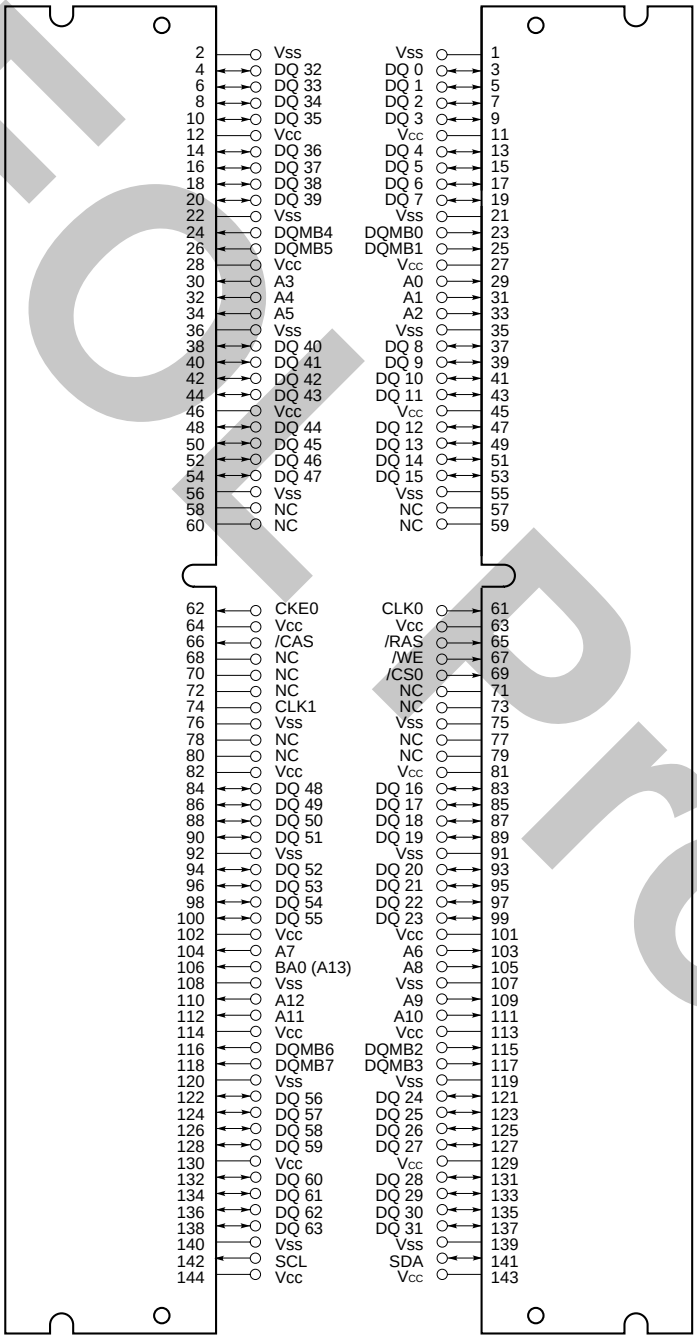
Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

Ordering Information

Part number	Clock frequency MHz (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
MC-45V8AB642KS-A75	133	2	4	144-pin Small Outline DIMM (Socket Type) Edge connector : Gold plated 25.4 mm height	4 pieces of μPD45V128161G5 (10.16 mm (400) TSOP (II))

Pin Configuration

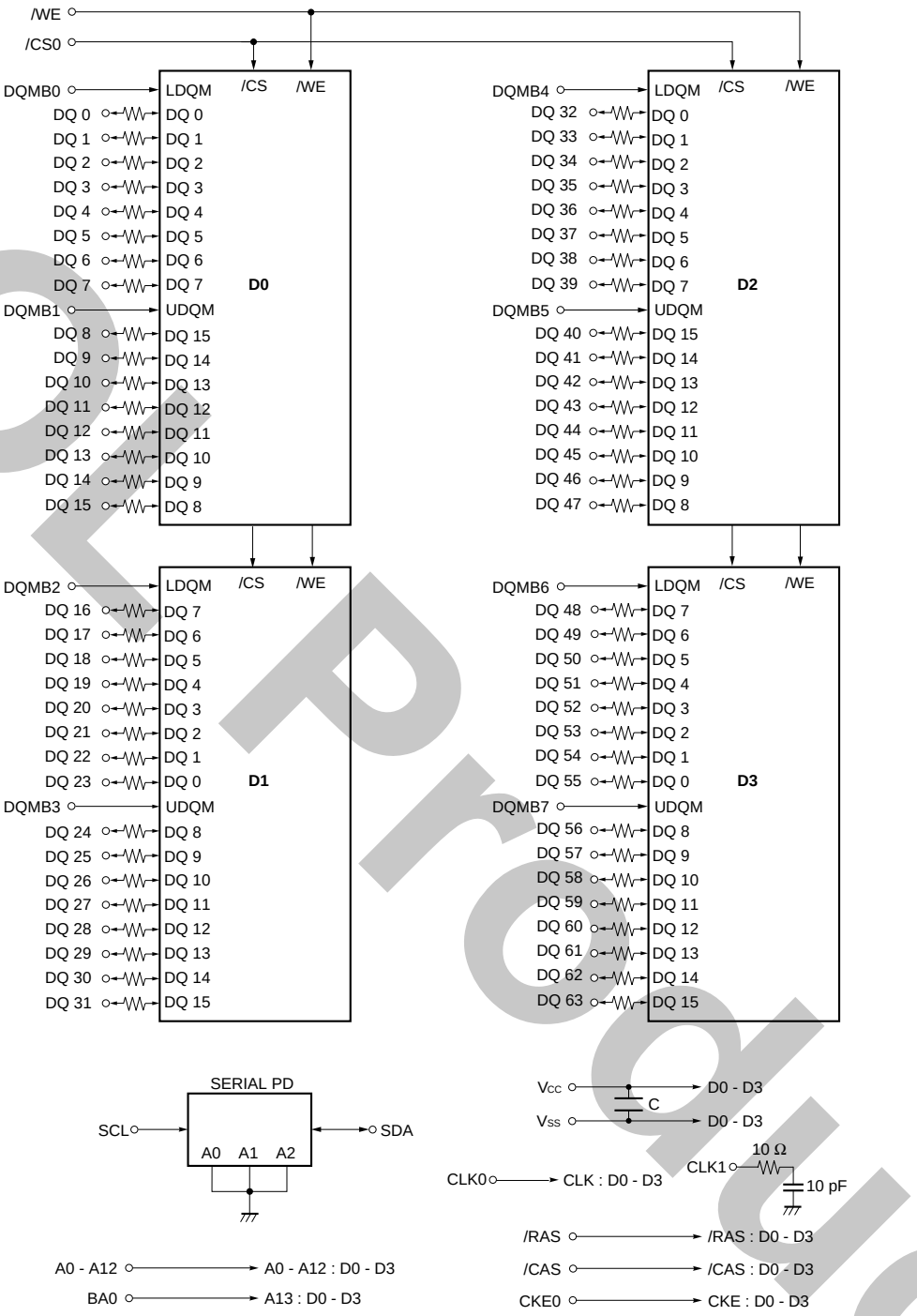
144-pin Small Outline Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

A0 - A12	: Address Inputs
[Row: A0 - A12, Column: A0 - A6]	
BA0 (A13)	: VirtualChannel DRAM Bank Select
DQ0 - DQ63	: Data Inputs/Outputs
CLK0, CLK1	: Clock Input
CKE0	: Clock Enable Input
/CS0	: Chip Select Input
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQMB0 - DQMB7	: DQ Mask Enable
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
Vcc	: Power Supply
Vss	: Ground
NC	: No Connection

Block Diagram



Remark D0 - D3: μPD45V128161 (4M words × 16 bits × 2 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A12, BA0 (A13), /RAS, /CAS, /WE	15		30	pF
	C_{I2}	CLK0	23		37	
	C_{I3}	CKE0	15		26	
	C_{I4}	/CS0	15		26	
	C_{I5}	DQMB0 - DQMB7	5		10	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63	5		12	pF

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current (Prefetch mode at one bank active)	$I_{CC1}P$	$t_{RC} \geq t_{RC\ (MIN.)}$ Prefetch is executed one time during t_{RC}.	-A75		600	mA	1
Operating current (Restore mode at one bank active)	$I_{CC1}R$	$t_{RC} \geq t_{RC\ (MIN.)}$	-A75		600	mA	1
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			4.8	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			4.8		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			80	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞ , Input signals are stable.			40		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			24	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			24		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			120	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.			80		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA Background : precharge standby	-A75		300	mA	2
Auto Refresh current	I_{CC5}	$t_{RCF} \geq t_{RCF\ (MIN.)}$	-A75		920	mA	3
Self refresh current	I_{CC6}	CKE ≤ 0.2 V	-A75		8	mA	
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V		–4	+4	μA	
Output leakage current	$I_{O\ (L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V		–1.5	+1.5	μA	
High level output voltage	V_{OH}	I_O = –4.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.0 mA			0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

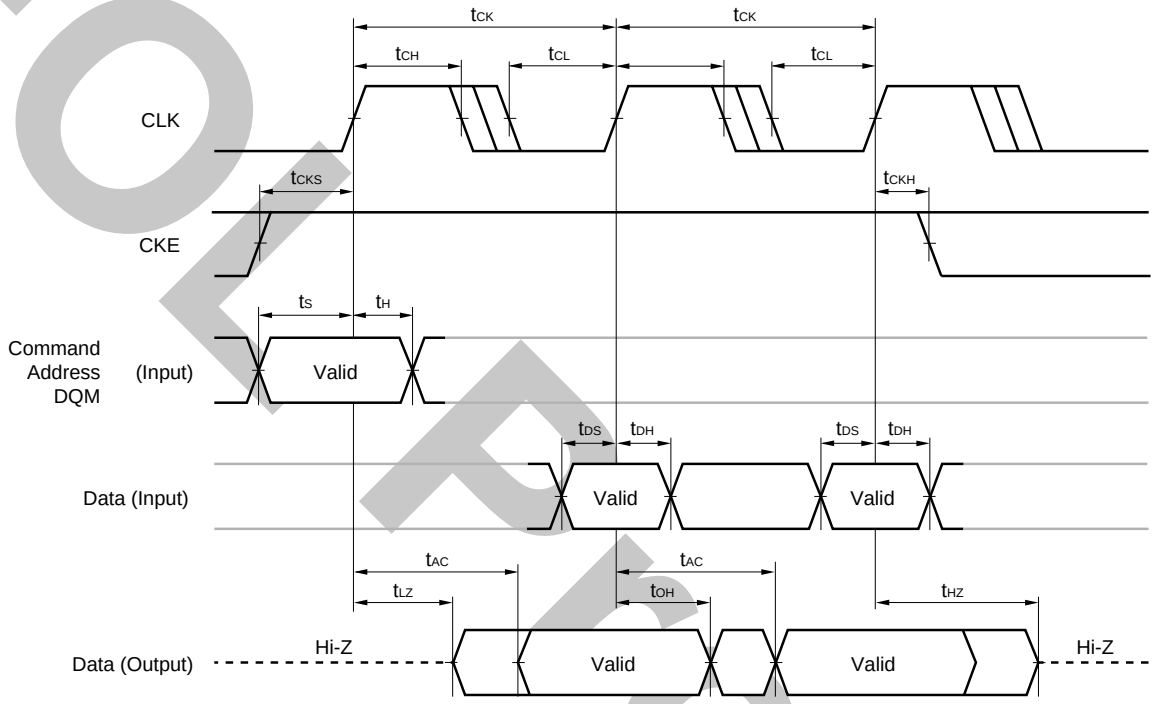
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

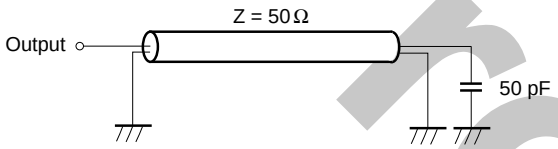
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$.
- An access time is measured at 1.4 V.



AC characteristics

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
Clock cycle time	t_{CK2}	7.5	–	ns	
Access time from CLK	t_{AC2}	–	5.4	ns	1
CLK high level width	t_{CH}	2.5	–	ns	
CLK low level width	t_{CL}	2.5	–	ns	
Data-out hold time	t_{OH}	2.7	–	ns	1
Data-out low-impedance time	t_{LZ}	0	–	ns	
Data-out high-impedance time	t_{HZ2}	2.5	5.4	ns	
Data-in setup time	t_{DS}	1.5	–	ns	
Data-in hold time	t_{DH}	0.8	–	ns	
Address, Command, DQM setup time	t_S	1.5	–	ns	
Address, Command, DQM hold time	t_H	0.8	–	ns	
CKE setup time	t_{CKS}	1.5	–	ns	
CKE hold time	t_{CKH}	0.8	–	ns	
CKE setup time (Power down exit)	t_{CKSP}	1.5	–	ns	
Transition time	t_T	0.5	30	ns	
Refresh time (4,096 refresh cycle)	t_{REF}	–	64	ms	
Mode register set cycle time	t_{RSC}	2	–	CLK	

Note 1. Output load.



AC characteristics (Background to Background operation)

Parameter	Symbol	-A75		Unit	Notes
		MIN.	MAX.		
Same Bank Operation					
ACT to ACT/REF Command period	t_{RC}	67.5	–	ns	
REF to REF/ ACT Command period	t_{RCF}	67.5	–	ns	
ACT to PRE Command period	t_{RAS}	52.5	120,000	ns	
PRE to ACT / REF Command period	t_{RP}	20	–	ns	
ACT to PFC/PFCA Command delay time	t_{APD}	15	–	ns	
ACT to PFR Command delay time (Prefetch Read Operation)	t_{APRD}	15	–	ns	
PFC to PRE Command delay time	t_{PPL}	22.5	–	ns	
PFCA / PFR to ACT/REF Command delay time	t_{PAL}	45	–	ns	
RST / RSTA to ACT(R) Note1 Command delay time	t_{RAD}	7.5	30	ns	2
Same, Other Bank Operation					
ACT(R) Note1 to PFC/PFCA/PFR Command delay time	t_{RPD}	37.5	–	ns	
PFC to PFC / PFCA Command delay time	t_{PPD}	22.5	–	ns	
Other Bank Operation					
ACT to ACT/ACT(R) or ACT(R) to ACT Command delay time	t_{RRD}	15	–	ns	
ACT(R) to ACT(R) Command delay time	t_{RRDR}	30	–	ns	
PFC /PFCA to RST /RSTA Command delay time	t_{PRD}	22.5	–	ns	

Notes 1. ACT (R) command is ACT command after RST command.

2. The another background operation and same channel foreground operation are illegal while t_{RAD} period.

AC characteristics (Foreground to Foreground operation)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
READ/WRITE to READ/WRITE Command delay time	t_{CCD}	7.5	–	ns	

AC characteristics (Background to Foreground operation)
(after same channel Prefetch/Restore)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
PFC/PFCA to READ/WRITE Command delay time	t_{PCD}	15	–	ns	
ACT(R) to READ/WRITE Command delay time	t_{RCD}	30	–	ns	1

Note 1. ACT (R) command is ACT command after RST command.

Serial PD (1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		08H	0	0	0	0	1	0	0	0	VC DRAM
3	Number of row addresses		0DH	0	0	0	0	1	1	0	1	13 rows
4	Number of column addresses		07H	0	0	0	0	0	1	1	1	7 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		40H	0	1	0	0	0	0	0	0	64 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface standard		01H	0	0	0	0	0	0	0	1	LVTTL
9	Read latency (/CAS latency) = 2 cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
10	Read latency (/CAS latency) = 2 access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type		00H	0	0	0	0	0	0	0	0	None
12	Refresh rate / type		80H	1	0	0	0	0	0	0	0	Normal
13	VC DRAM width		10H	0	0	0	1	0	0	0	0	×16
14	Error checking DRAM width		00H	0	0	0	0	0	0	0	0	None
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		04H	0	0	0	0	0	1	0	0	4
17	Number of banks on each VC DRAM		02H	0	0	0	0	0	0	1	0	2 banks
18	Read latency (/CAS latency) supported		02H	0	0	0	0	0	0	1	0	2
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	VC DRAM module attributes		00H	0	0	0	0	0	0	0	0	
22	VC DRAM device attributes : general		0EH	0	0	0	0	1	1	1	0	
23-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP\ (MIN.)}$	-A75	14H	0	0	0	1	0	1	0	0	20 ns
28	$t_{RRD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	$t_{APD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
30	$t_{RAS\ (MIN.)}$	-A75	34H	0	0	1	1	0	1	0	0	52.5 ns

(2/2)

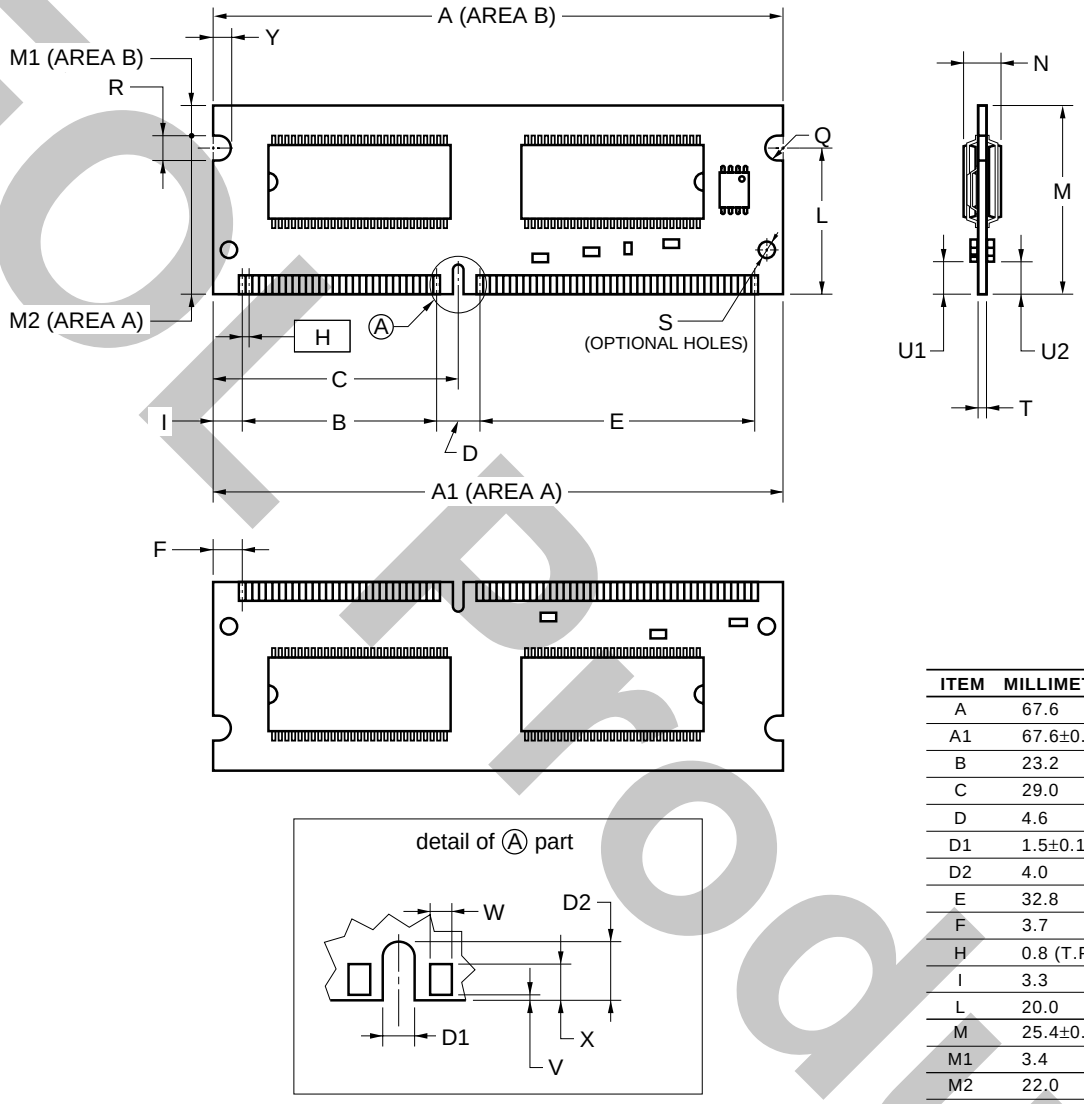
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
31	Module bank density		10H	0	0	0	1	0	0	0	0	64M bytes
32	Address and command signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Address and command signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time	-A75	15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time	-A75	08H	0	0	0	0	1	0	0	0	0.8 ns
36	Prefetch read latency	-A75	04H	0	0	0	0	0	1	0	0	4 clocks
37	$t_{PCD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
38	Number of segment addresses		02H	0	0	0	0	0	0	1	0	2 bits
39	Number of channels		04H	0	0	0	0	0	1	0	0	16
40	Depth of channels		07H	0	0	0	0	0	1	1	1	128 bits
41-61												
62	SPD revision		02H	0	0	0	0	0	0	1	0	2.0
63	Checksum for bytes 0 - 62	-A75	2AH	0	0	1	0	1	0	1	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											

Timing Charts

Please refer to the ***μ*PD45V128421, 45V128821, 45V128161 Data sheet** (E0025N).

Package Drawing

144-PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	67.6
A1	67.6±0.15
B	23.2
C	29.0
D	4.6
D1	1.5±0.10
D2	4.0
E	32.8
F	3.7
H	0.8 (T.P.)
I	3.3
L	20.0
M	25.4±0.15
M1	3.4
M2	22.0
N	3.8 MAX.
Q	R2.0
R	4.0±0.10
S	ϕ1.8
T	1.0±0.1
U1	3.2 MIN.
U2	4.0 MIN.
V	0.25 MAX.
W	0.6±0.05
X	2.55 MIN.
Y	2.0 MIN.

Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of edition	Location
NEC Corporation (M15239E)				
1st edition / Dec.2000	–	–	–	–
Elpida Memory, Inc. (E0028N)				
1st edition / Jan. 2001	–	–	–	Republished by Elpida Memory, Inc.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The names of the companies, products, and logos described herein are the trademarks or registered trademarks of each company.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

- **The information in this document is current as of April, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of Elpida's data sheets or data books, etc., for the most up-to-date specifications of Elpida semiconductor products. Not all products and/or types are available in every country. Please check with an Elpida Memory, Inc. for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of Elpida. Elpida assumes no responsibility for any errors that may appear in this document.
- Elpida does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of Elpida semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of Elpida or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. Elpida assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While Elpida endeavours to enhance the quality, reliability and safety of Elpida semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in Elpida semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- Elpida semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of Elpida semiconductor products is "Standard" unless otherwise expressly specified in Elpida's data sheets or data books, etc. If customers wish to use Elpida semiconductor products in applications not intended by Elpida, they must contact an Elpida Memory, Inc. in advance to determine Elpida's willingness to support a given application.
  (Note)
  (1) "Elpida" as used in this statement means Elpida Memory, Inc. and also includes its majority-owned subsidiaries.
  (2) "Elpida semiconductor products" means any semiconductor product developed or manufactured by or for Elpida (as defined above).

M8E 00.4