Highly Programmble Voltage Supervisory Circuit

FEATURES

- **User Programmable Device Configuration**
- **Guaranteed Reset Valid to VCC = 1V**
- **Immune to Short Negative VCC Transients**
- **Six Unique Pin Configurations**
- **User Programmable Feature Options:**
  - **Reset Threshold Voltages**
  - **Reset Pulse Widths**
  - **Programmable Watchdog Timeouts**
  - **Programmable Over- or Under-Voltage Sensing**
- **High Reliability**
  - **Endurance: 100,000 erase/write cycles**
  - **Data retention: 100 years**

INTRODUCTION

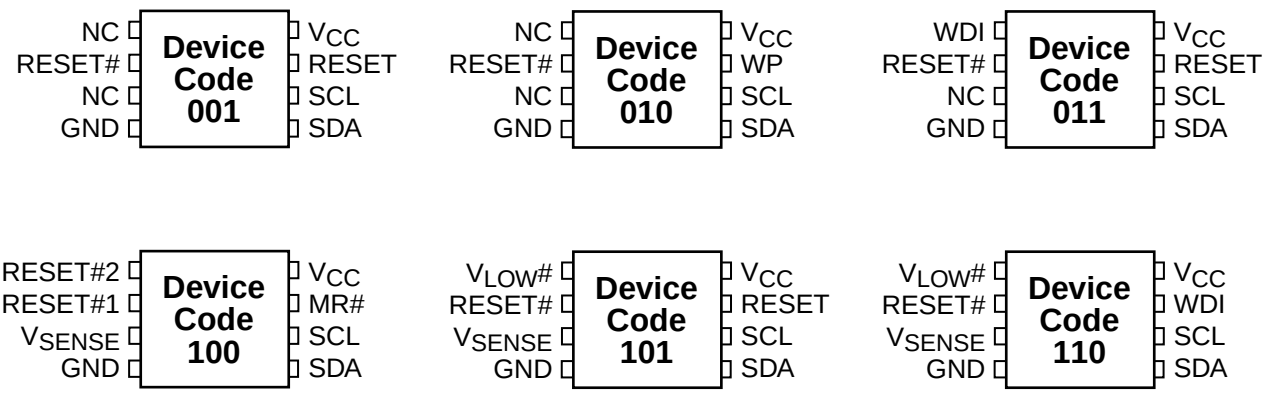
The SMS24 is a configurable and in-system programmable second generation 8 pin supervisory circuit. This single device is adaptable to provide the optimum functionality for a given system or sub-system. User programmable functions available — reset pulse width, watchdog delays, and voltage monitor thresholds — eliminate external components and allow standardization to enhance system reliability. Additionally, 4K bits of general purpose EEPROM is available on all configurations. The SMS24 is available in six pin configurations, and is compatible with all Summit programmable devices and other I2C components.

Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

DEVICE TYPES

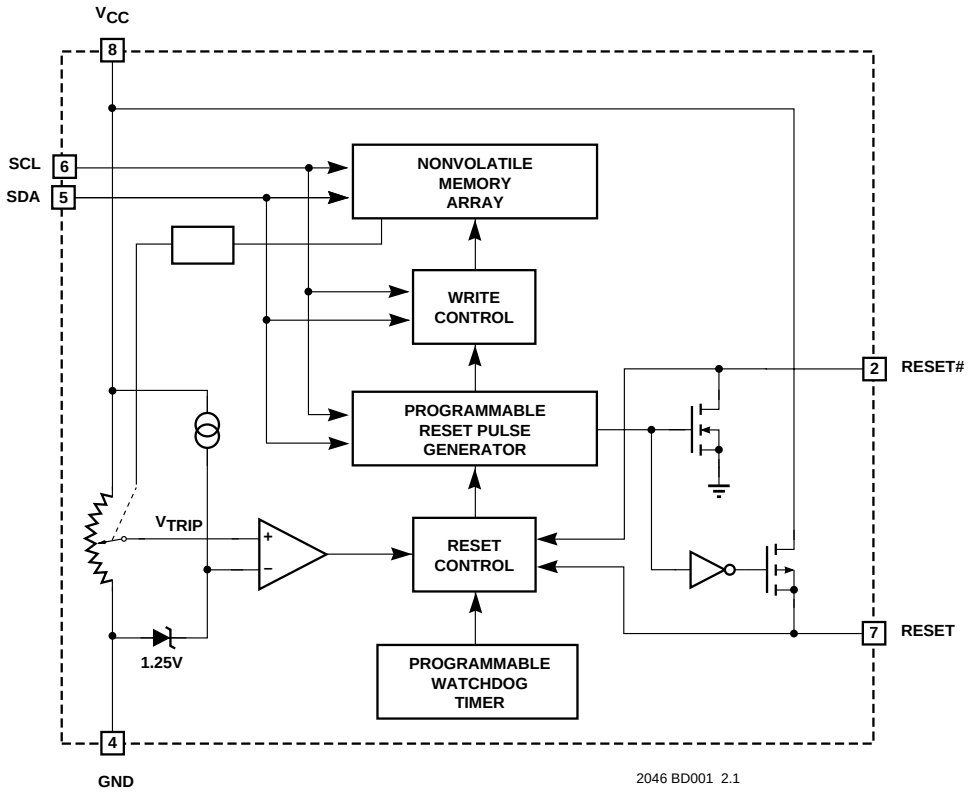
Device Code	Function								
	Reset#	Reset	Watchdog	Software WDI	WDI Pin	Write Protect Pin	2nd Voltage Monitor	Manual Reset Input	NV Memory
001	✔	✔	✔	✔					✔
010	✔		✔	✔		✔			✔
011	✔	✔	✔		✔				✔
100	✔		✔	✔				✔	✔
101	✔	✔	✔	✔			✔		✔
110	✔		✔		✔		✔		✔

2048 DTTable 2.1

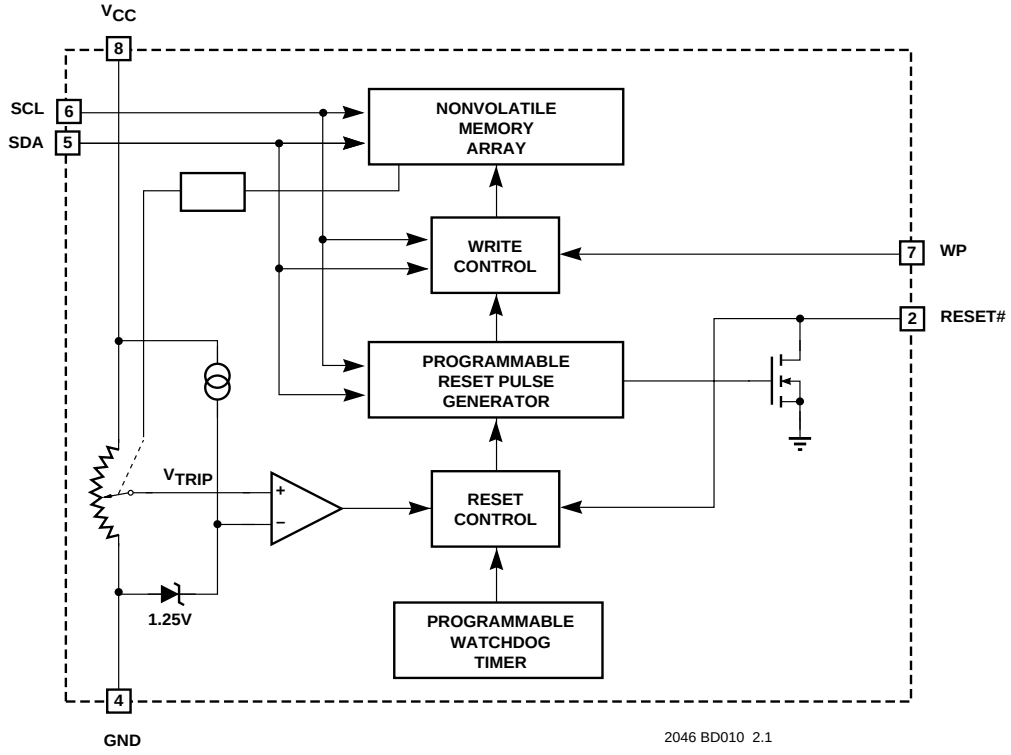


2046 DT 1.0

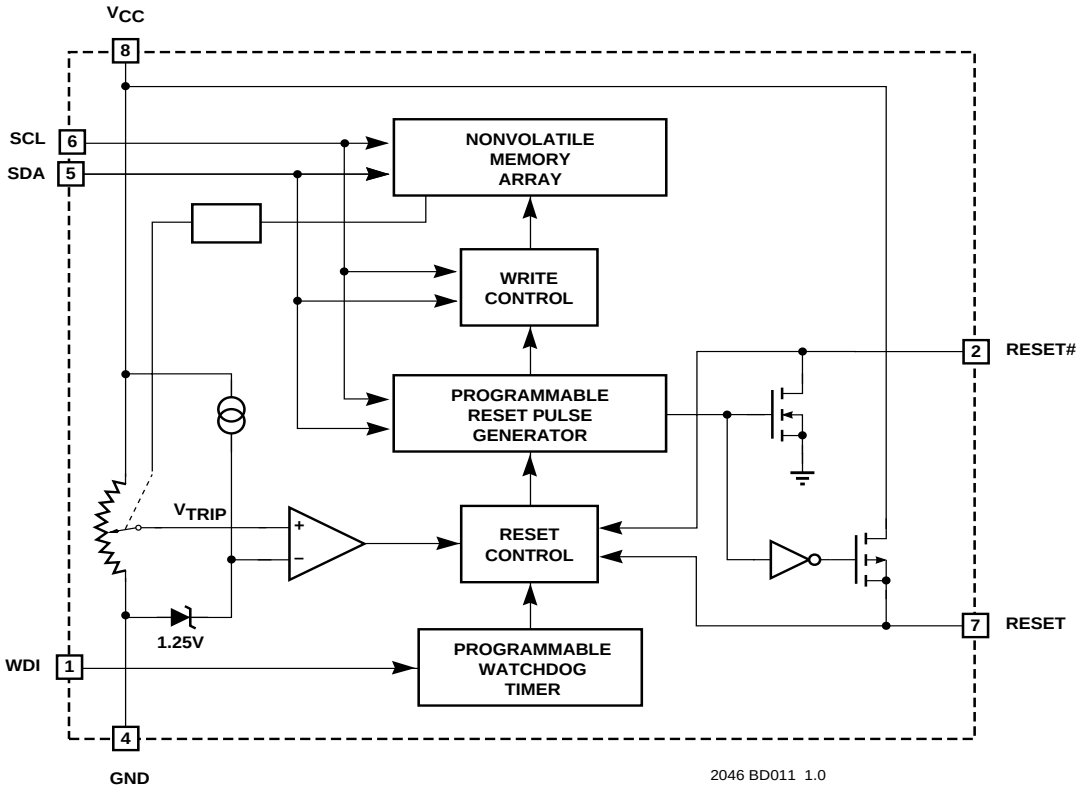
FUNCTIONAL BLOCK DIAGRAMS



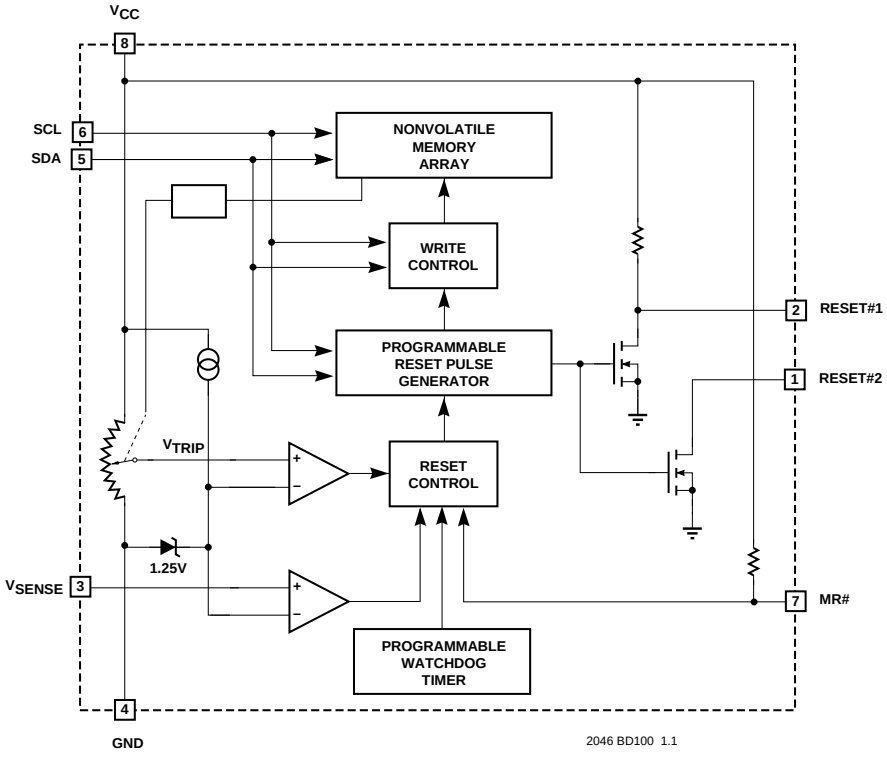
Block Diagram Device Code 001



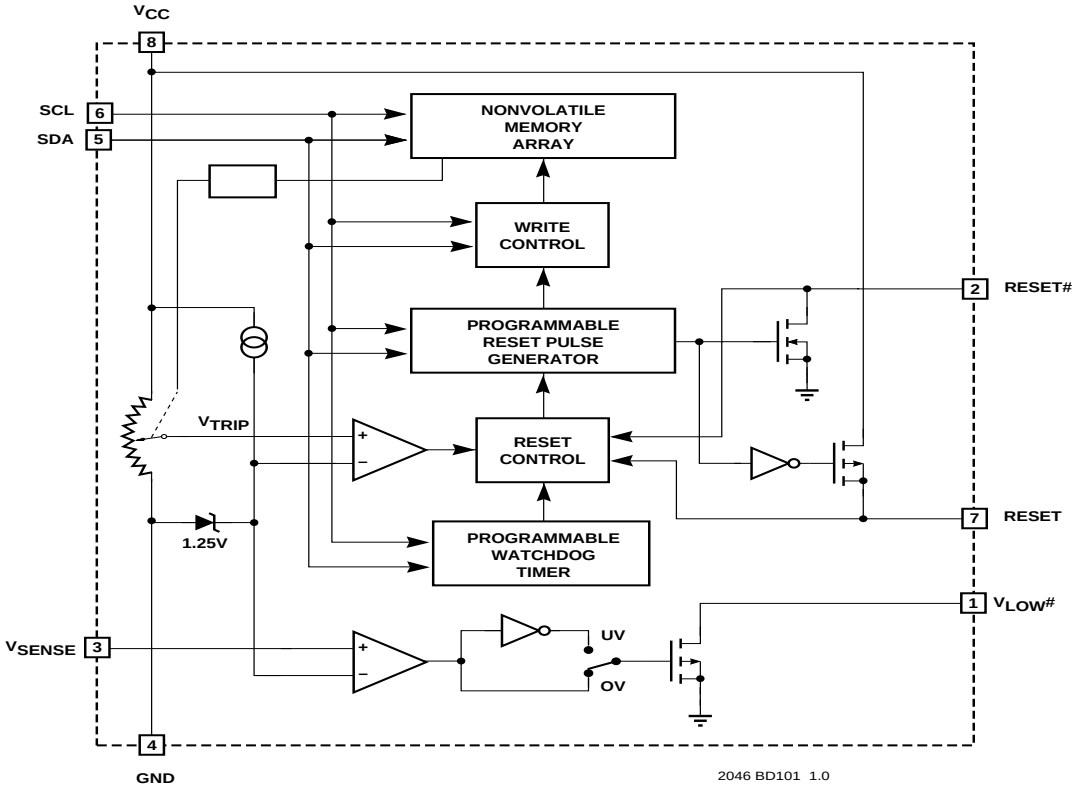
Block Diagram Device Code 010



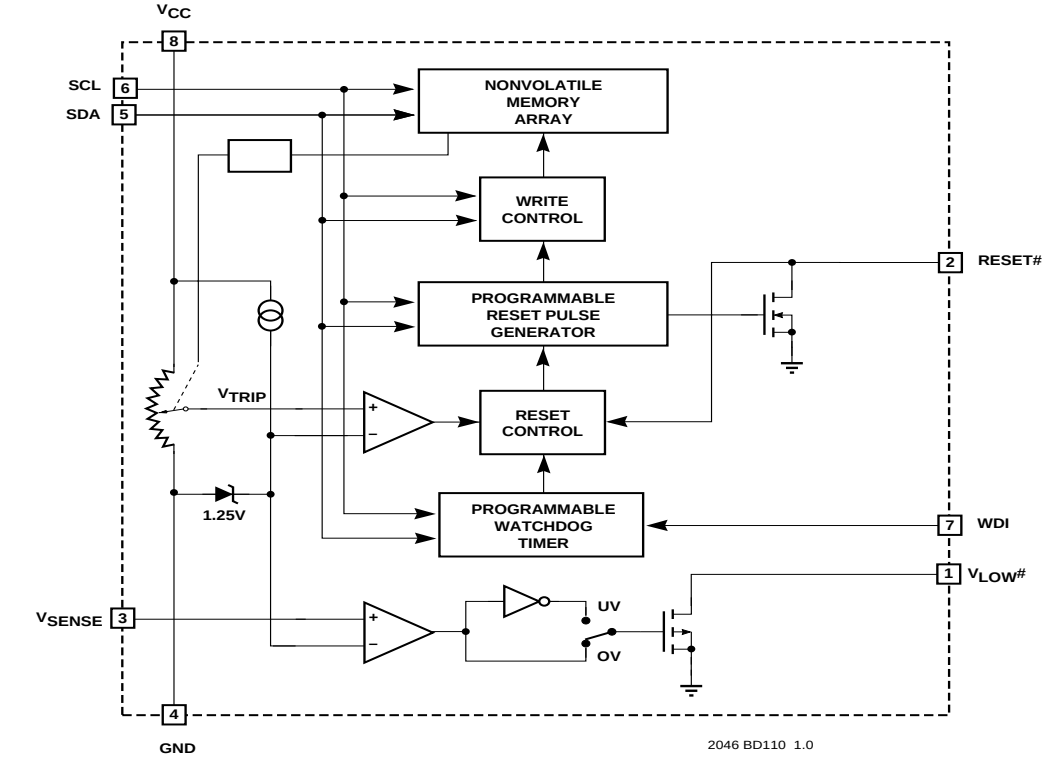
Block Diagram Device Code 011



Block Diagram Device Code 100



Block Diagram Device Code 101



Block Diagram Device Code 110

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to 125°C
Storage Temperature ..... -65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300 °C
Terminal Voltage with Respect to GND:
V_{CC} ..... -0.3V to 6.0V
All Others ..... -0.3V to 6.0V

***COMMENT**

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Operating supply voltage	Valid RESET# output	1		5.5	V
		Memory operaton	2.7		5.5	V
I_{CC}	Supply current	3.6V < V_{CC} < 5.5V			50	µA
		2.7V < V_{CC} < 3.6V			20	µA
		Memory access			3	µA
V_{PRST}	Programmable reset threshold	RR4 RR3 RR2 RR1 RR0				
		0 0 0 0 1	2.075	2.15	2.25	V
		0 0 0 1 0	2.55	2.65	2.7	V
		0 0 1 0 0	2.8	2.9	3.0	V
		0 1 0 0 0	4.25	4.375	4.5	V
		1 0 0 0 0	4.5	4.625	4.75	V
V_T	V_{SENSE} input threshold		1.23	1.25	1.27	V
V_{OL}	RESET#1, RESET#2, V_{LOW}#: output voltage	I_{SINK} = 1.2mA, V_{CC} = V_{PRST} min.			0.3	V
		I_{SINK} = 200mA, V_{CC} = 1.2V			0.3	V
I_{MR}	MR# pullup current			100		µA
V_{IL}	Noise rejection on V_{CC}				$0.3 \times V_{CC}$	V
V_{IH}	Delay threshold crossing to RESET out		$0.7 \times V_{CC}$			V

2046 DCElect Table 2.0

RECOMMENDED OPERATING CONDITIONS

Temperature	–40°C to 85°C.
Voltage	2.7V to 5.5V

ENDURANCE AND DATA RETENTION

The SMS24 is designed for applications requiring 100,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 100,000 erase/write cycles.

PIN DESCRIPTIONS

RESET#

This signal is an active-low open drain I/O. Whenever the voltage on V_{CC} is below the programmed threshold voltage the RESET# pin will be driven low. After V_{CC} passes through the threshold (in a positive direction) the RESET# output will continue to be driven for the programmed time-out period (t_{PTO}). In most configurations RESET# is also an input. Whenever it is driven low it will activate the reset timer. The RESET# output will then be driven low by the device for the programmed period. If the input pulse is of shorter duration than t_{PTO}, RESET# will continue to be driven. If it is longer than t_{PTO}, RESET# will be released and follow the input back high.

RESET

This signal is an active-high open drain I/O. Whenever the voltage on V_{CC} is below the programmed threshold voltage the RESET pin will be driven high. After V_{CC} passes through the threshold (in a positive direction) the RESET output will continue to be driven for the programmed time-out period. In all configurations using RESET it is also an input. Whenever it is driven high it will activate the reset timer. The RESET output will then be driven high by the device for the programmed period. If the input pulse is of shorter duration than t_{PTO}, RESET will continue to be driven. If it is longer than t_{PTO}, RESET will be released and follow the input back low.

RESET#1 & RESET#2

These signals are active-low open drain outputs (not I/Os). These outputs are only available to Device Code 100, and are both set to a low state by any one of three events: V_{CC} below trip level, V_{SENSE} < 1.25V, or MR# strobed low.

MR#

Manual Reset input is an active low input. Whenever it is taken low it will generate a reset time-out.

V_{SENSE}

This is a second voltage sense input connected to its own comparator that has reference of 1.25V. The comparator can be programmed to activate the V_{LOW}# output either for an over-voltage or under-voltage condition.

V_{LOW}#

This is an active-low open-drain output that can be wire-ORed with the RESET# output or tied directly to an interrupt input.

WDI

This is the Watchdog Interrupt input. Whenever a transition occurs on WDI the watchdog timer will be cleared. If the device does not receive an interrupt before t_{WDTO} the device will drive the reset output(s). The period t_{WDTO} is programmable for four basic values. It can also be placed into an idle mode, facilitating system debug, and allowing a system time to configure itself after a power-on.

WP

This is an auxilliary Write lockout input pin. When held high no writes will occur.

SCL

The serial interface clock input.

SDA

The serial interface data I/O.

DEVICE OPERATION

REGISTERS

Configuration Register

The configuration Register, located at address 00, is illustrated in Table 1. The Configuration Bits (6, 5, & 4) select the basic Device Code, and are referred to as Con2, Con1, and Con0. Bit 7 is the Lock Bit, and when set to 1 locks the contents of the register.

Note: The Threshold Trim Bits are set at the factory. Before modifying them you must read the contents and save the value so that it can be written back into the device. After configuring them Bit 7 should be set to a 1 to prevent inadvertent modification.*

Table 1. Configuration Register

MSB 7	6	5	4	3	2	1	LSB 0
LOCK	**Con2**	**Con1**	**Con0**	**T3**	**T2**	**T1**	**T0**
x	Valid Device Codes			Threshold Trim *			
	0	0	1				
	0	1	0				
	0	1	1				
	1	0	0				
	1	0	1				
	1	1	0				
0	Configuration Register Open						
1	Configuration Locked (non-volatile)						

2046 Table01 2.0

Programming Registers

Once the device has been configured it is a simple matter of writing to the two Programming Registers to prepare the device for operation.

Table 2. Programming Register 0

MSB 7	6	5	4	3	2	1	LSB 0
x	**RT1**	**RT0**	**RR4**	**RR3**	**RR2**	**RR1**	**RR0**
	Reset Threshold Volts		**Reset Threshold Bits**				
	2.15V →		0	0	0	0	1
	2.65V →		0	0	0	1	0
	2.90V →		0	0	1	0	0
	4.375V →		0	1	0	0	0
	4.625V →		1	0	0	0	0
	Reset Timeout Bits		Reset Timeout Seconds				
	0	0	← 25ms				
	0	1	← 50ms				
	1	0	← 100ms				
	1	1	← 200ms				

2046 Table02 2.0

Table 3. Programming Register 1

<table>
<tr><th>MSB
7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>LSB
0</th></tr>
<tr><td rowspan="11">x</td><td>LOCK</td><td>OV</td><td>Add</td><td>DT</td><td>WD2</td><td>WD1</td><td>WD0</td></tr>
<tr><td colspan="4">Watchdog Timeout Seconds</td><td colspan="3">Watchdog Timeout Bits</td></tr>
<tr><td colspan="4">OFF or Idle Mode →</td><td>0</td><td>0</td><td>x</td></tr>
<tr><td colspan="4">0.4s →</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td colspan="4">0.8s →</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">1.6s →</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td colspan="4">3.2s →</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">6.4s →</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td rowspan="5">x</td><td rowspan="3">x</td><td rowspan="2">x</td><td>0</td><td colspan="3">Device Type Address 1010</td></tr>
<tr><td>1</td><td colspan="3">Device Type Address 1011</td></tr>
<tr><td>0</td><td colspan="2">Responds to Address Pin Bias</td><td rowspan="3">x</td></tr>
<tr><td>1</td><td colspan="2">Ignores Address Pin Bias</td></tr>
<tr><td>0</td><td colspan="2">V_{SENSE} Triggers > Threshold (1.25V)</td><td rowspan="3">x</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">V_{SENSE} Triggers < Threshold (1.25V)</td></tr>
<tr><td>0</td><td colspan="3">PR Registers Open for Writing</td><td rowspan="2">x</td></tr>
<tr><td>1</td><td colspan="3">PR Registers Writing Lockout</td></tr>
</table>

2048 Table03 2.0

MEMORY OPERATION

The SMS24 memory is configured as a 2K x 8 array. Data is received and transmitted via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus

Input Data Protocol

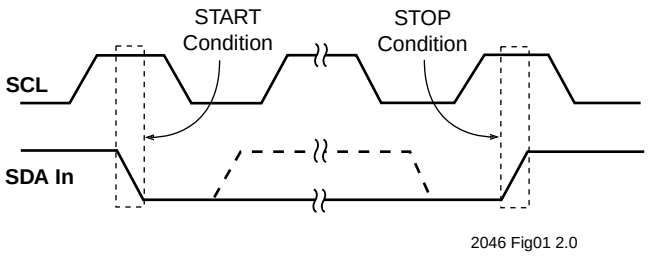
Configuring and programming the SMS24 is done using the 2-wire serial interface. The device type address for this operation is 1001_{BIN}.

The protocol defines any device that sends data onto the bus as a "transmitter" and any device that receives data as a "re ceiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases the SMS24 will be a "slave" device, since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time because changes on the data line while SCL is high will be interpreted as a start or a stop condition.

START and STOP Conditions

When both the data and clock lines are high, the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high is defined as the "START" condition. A low-to-high transition on the data line while the clock is high is defined as the "STOP" condition.



2046 Fig01 2.0

Figure 1. START and STOP Conditions

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to ACKnowledge that it received the eight bits of data.

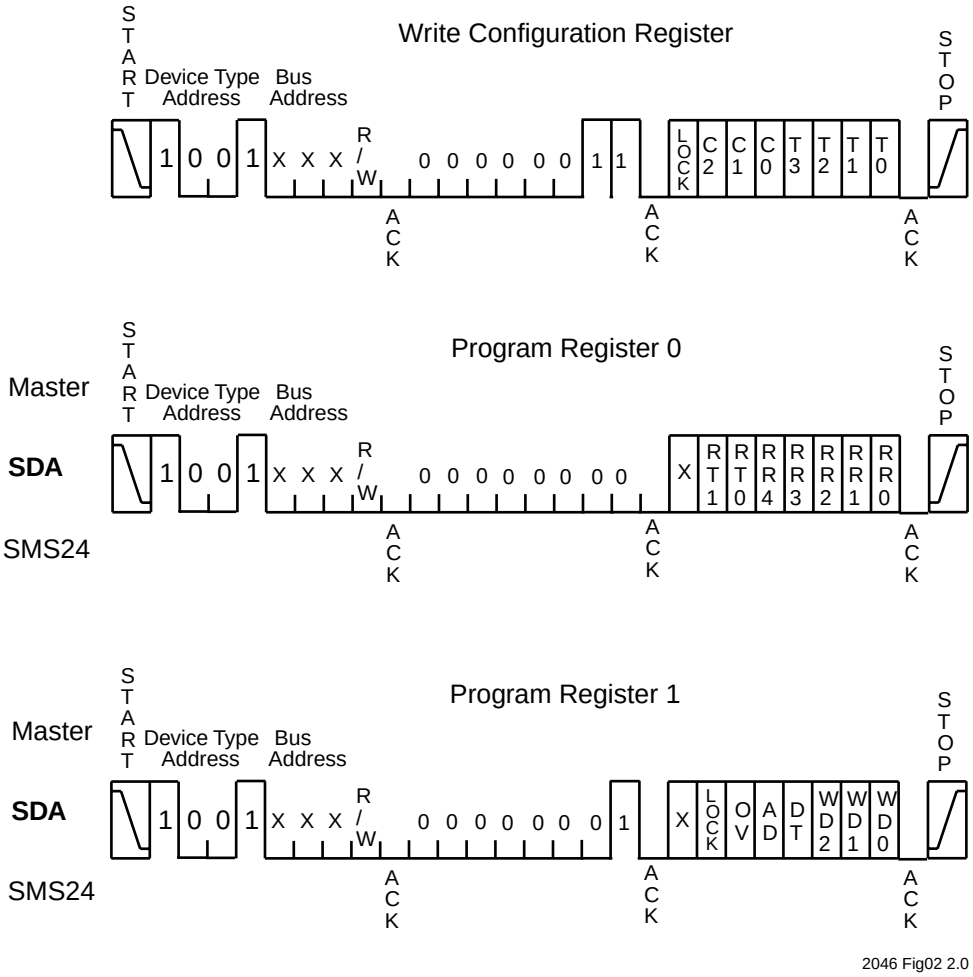


Figure 2. Programming the SMS24

The SMS24 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected the SMS24 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word. In the READ mode the SMS24 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and if no STOP condition is generated by the master, the SMS24 will continue to transmit data. If an ACKnowledge is not detected the SMS24 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier. For the SMS24 this is be 1010_{BIN} or 1011_{BIN} depending upon the DT bit of PR1. The configuration and Program Registers have a device type address of 1001.

The next three bits are the high order address bits.

The last bit of the data stream defines the operation to be performed. When set to “1” a read operation is selected. When set to “0” a write operation is selected.

WRITE OPERATIONS

The SMS24 allows two types of write operations: byte write and page write. A byte write operation writes a single byte during the nonvolatile write period (tWR). The page write operation allows up to 16 bytes in the same page to be written during tWR.

Table 4. Device Addressing

Device Identifier Bits				Memory Address			R / W
				A10	A9	A8	
					Read →		1
					Write →		0
				x	x	x	x
1	0	1	0	← Default Memory Device			
1	0	1	1	← Alternate Memory Device			
1	0	0	1	← Configuration Register Device			

2046 Table04 2.0

Byte Write

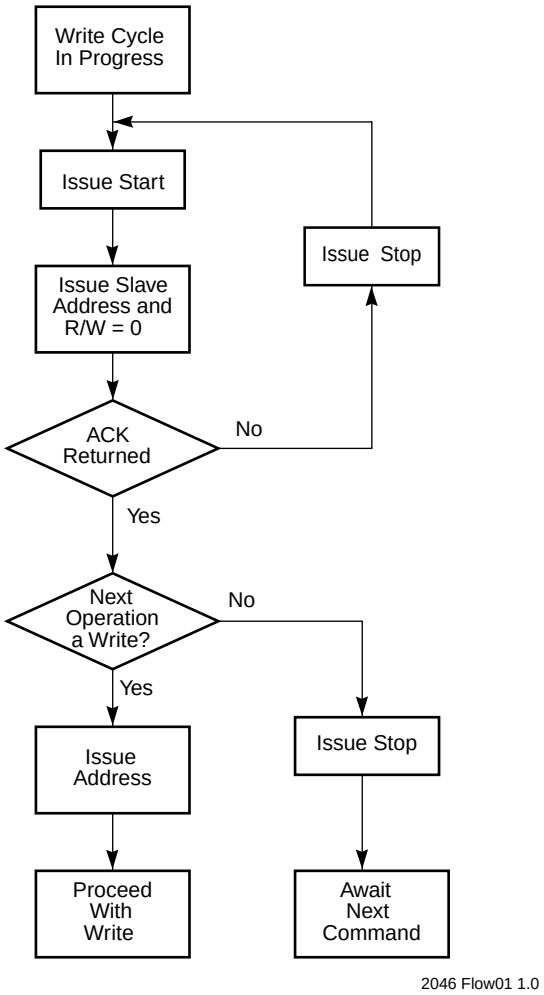
After the slave address is sent an ACKnowledge is generated and then the balance of the address is transmitted. Upon receipt of the word address the SMS24 responds with an ACKnowledge. After receiving the next byte of data it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS24 begins the internal write cycle. While the internal write cycle is in progress the SMS24 inputs are disabled and the device will not respond to any requests from the master.

Page Write

The SMS24 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte the SMS24 will respond with an ACKnowledge. The SMS24 automatically increments the address for subsequent data words. After the receipt of each word the low order address bits are internally incremented by one. The high order bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will rollover, and the previously written data will be overwritten. As with the byte-write operation all inputs are disabled during the internal write cycle.

Acknowledge Polling

When the SMS24 is performing an internal WRITE operation it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete. See the flow diagram for the proper sequence of operations for polling.



2046 Flow01 1.0

Flow Diagram

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are two different read options: 1. Current Address Byte Read, or 2. Random Address Byte Read

Current Address Read

The SMS24 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and incre-

ment the current address pointer. When the SMS24 receives the slave address field with the R/W bit set to “1” it issues an acknowledge and transmits the 8-bit word stored at address location n+1. The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point the SMS24 discontinues data transmission.

Random Address Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS24 to the desired address. After the word address acknowlthe R/W bit set to READ. The SMS24 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point the master does not acknowledge the transmission but does generate the stop condition. The SMS24 discontinues data transmission and reverts to its standby power mode.

Sequential READ

Sequential reads can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS24. The SMS24 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP condition. During a sequential read operation the internal address counter is automatically incremented with each ACKnowledge signal. For read operations all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address the address counter will rollover and the memory will continue to output data.

IN-SYSTEM PROGRAMMING THE SMS24

The need for an in-system programming interface for a supervisory circuit is necessitated by the rapid change to both board designs (feature upgrades to a common design core) and the ICs resident on the boards. The SMS24 provides an ideal solution for maintaining currency with the change in boards and their power supplies as they shift from generation to generation.

Theory of Operation

The SMS24 can be designed-in with the simple addition of an inexpensive 9-pin 0.100" centerline header. Summit supports this configuration with the SMX3199-A programmer, and in the future will support this interface with the SMX3200. Depending upon the end use of the interface, prototyping vs. field support, the header can be placed anywhere on the board or as a right angle header at the back edge of the card (the side pointing outwards from a card cage).

The basic interface circuit is shown in Figure 3. In order to clearly illustrate the examples, all additional traces and series resistors are either bold or outlined in a dashed box.

Notes:

If the device appears to be ignoring attempts to be programmed ensure the supplied V_{CC} is above the programmed threshold. If V_{CC} is below the reset threshold all attempts to write to the device will be ignored.

If you are writing to the memory array and 'read-backs' show occasional rows not being written check the watchdog timer. Either disable the watchdog or insure WDI is being strobed (high to low) at intervals less than the programmed watchdog time out period.

Figure 3 is a block diagram illustration of the SMS24 configured as device code 110. The comments in bold italics indicate the programmable options for this code

Supporting the SMS24 is a programming module, the SMX3199-A. The hardware is a small printed circuit card that interfaces to a standard PC parallel printer port. A target programming cable is connected from this to the user's card. The software provides an intuitive configuration screen and also a memory test verification screen (examples of the screens are shown).

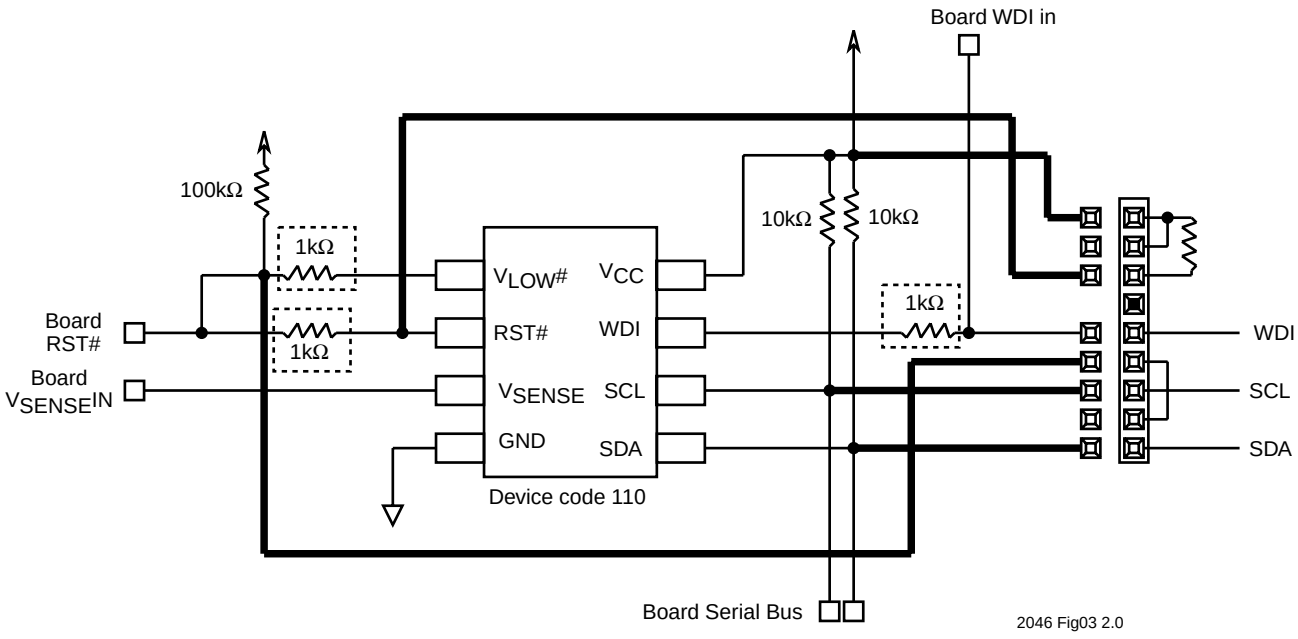


Figure 3. Basic Interface Circuit

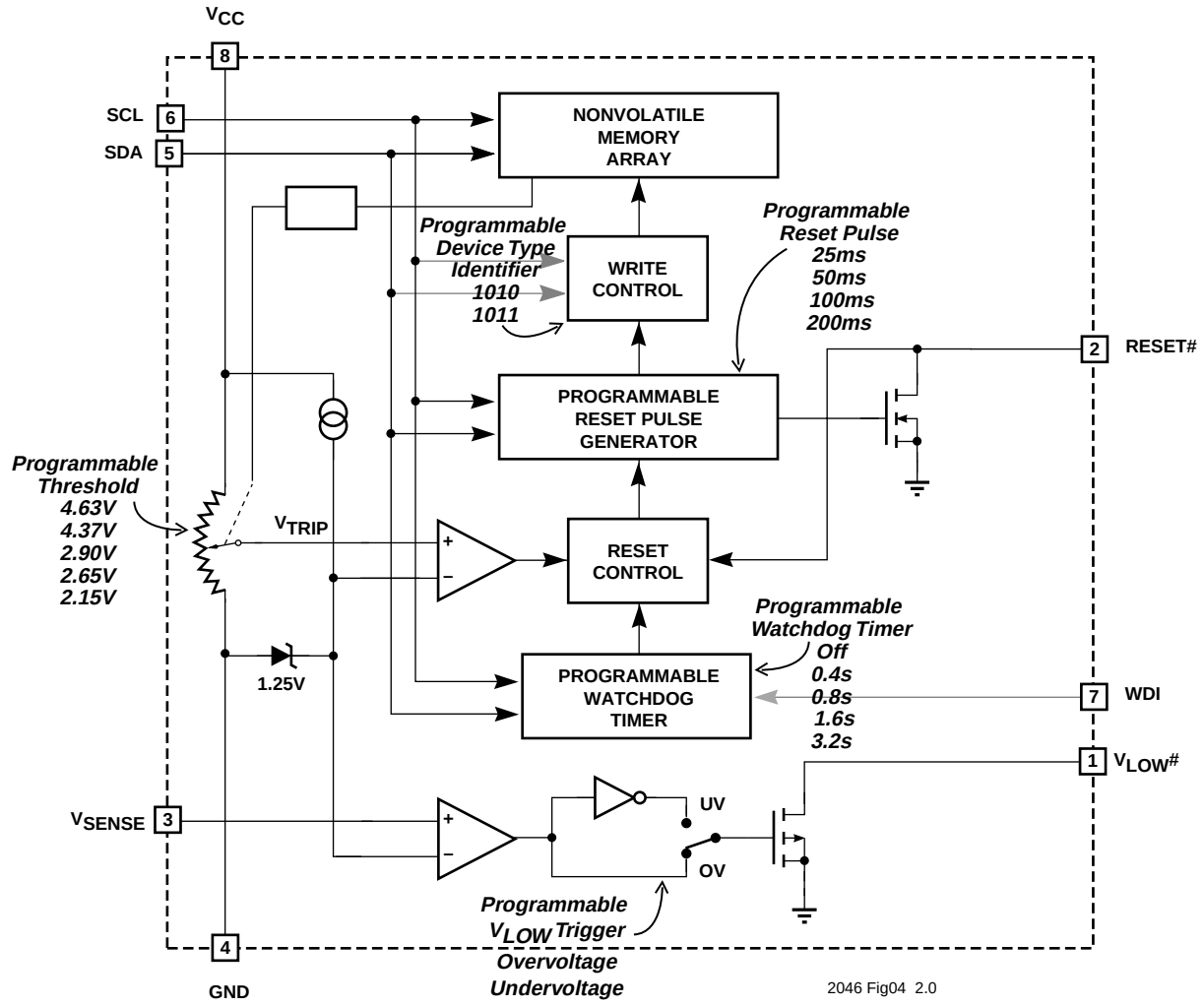


Figure 4. Programmable Options for Device Code 110

Figure 5. Configuration Screen

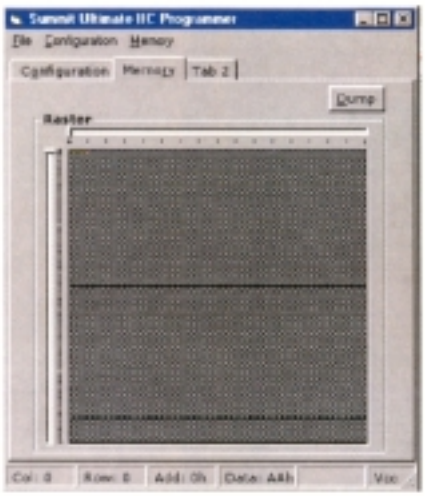


Figure 6. Memory Test Screen

Table 5. Memory AC Operating Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time			1000	ns
t_F	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

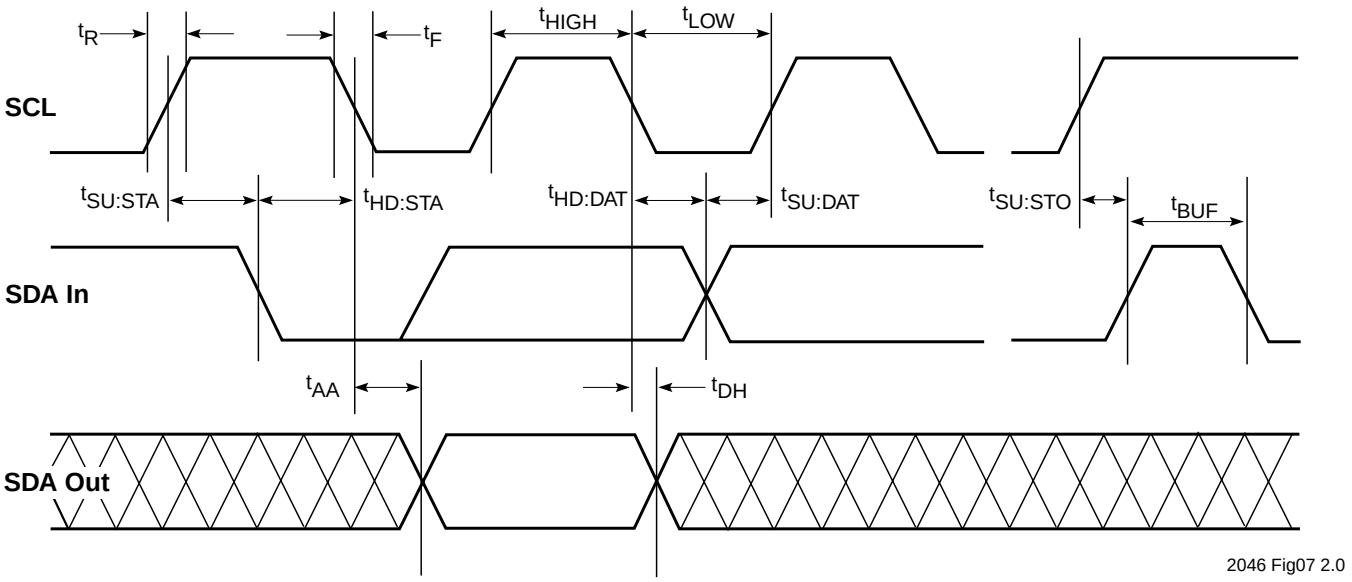
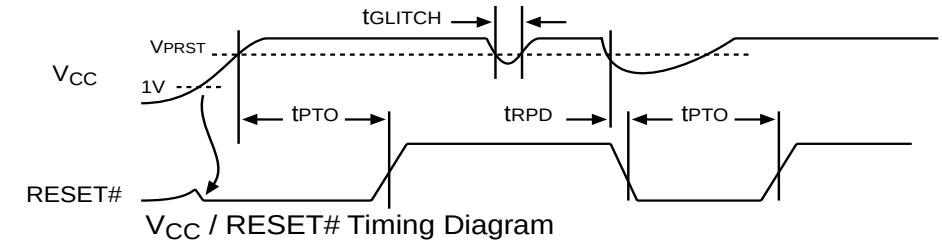
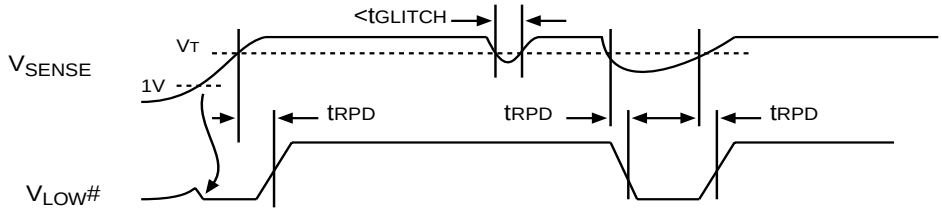


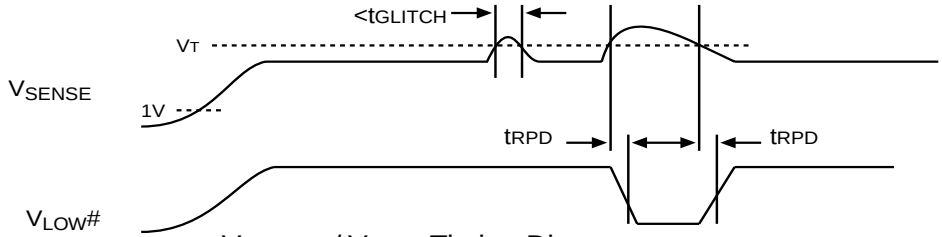
Figure 7. Memory Operating Characteristics



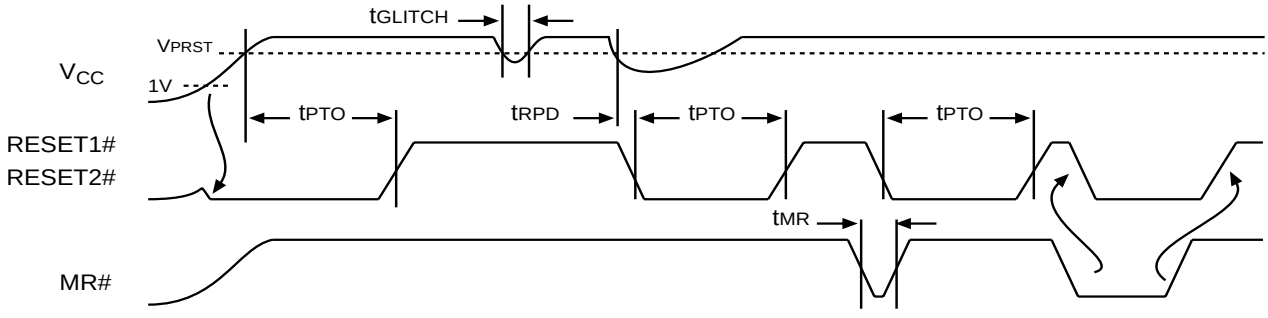
V_{CC} / RESET# Timing Diagram



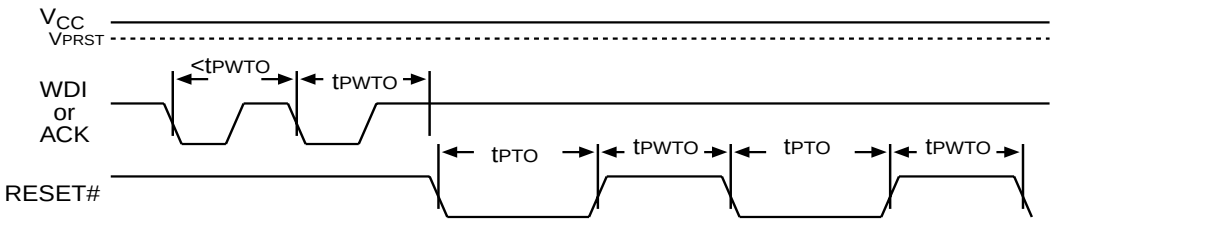
V_{SENSE} / V_{LOW} Timing Diagram
Device Codes 101 & 110 Only, Undervoltage Option



V_{SENSE} / V_{LOW} Timing Diagram
Device Codes 101 & 110 Only, Overvoltage Option



Manual Reset Operation Device Code 100 Only



Watchdog Timer Timing Diagram

2046 Fig08 2.0

Figure 8. System Timing Patterns

AC OPERATING CHARACTERISTICS

Under recommended Operating Conditions

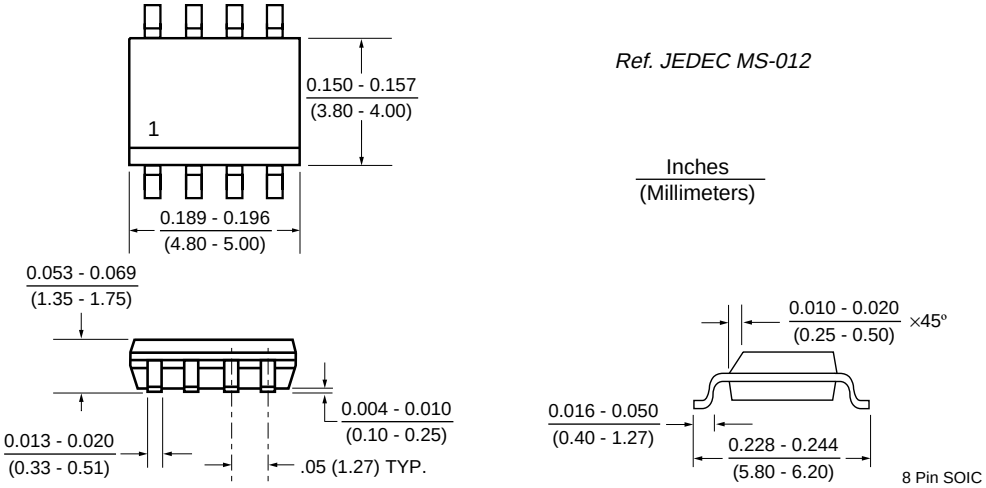
Symbol	Parameter	Condition			Min.	Typ.	Max.	Units
t_{PTO}	Programmable reset timeout period (Note 1)		RT1	RT0				
			0	0	20	25	30	ms
			0	1	35	50	65	ms
			1	0	65	100	135	ms
			1	1	130	200	270	ms
t_{PWTO}	Programmable watchdog timer timeout period	WD2	WD1	WD0				
		0	0	x		Off		
		0	1	1		0.4		s
		1	0	0		0.8		s
		1	0	1		1.6		s
		1	1	0		3.2		s
		1	1	1		6.4		s
t_{MR}	Minimum manual reset pulse width				50			ns
t_{GLITCH}	Noise rejecton on V_{CC}					30		ns
t_{RPD}	Delay threshold crossing to RESET out					5		µs

2046 ACElect Table 2.0

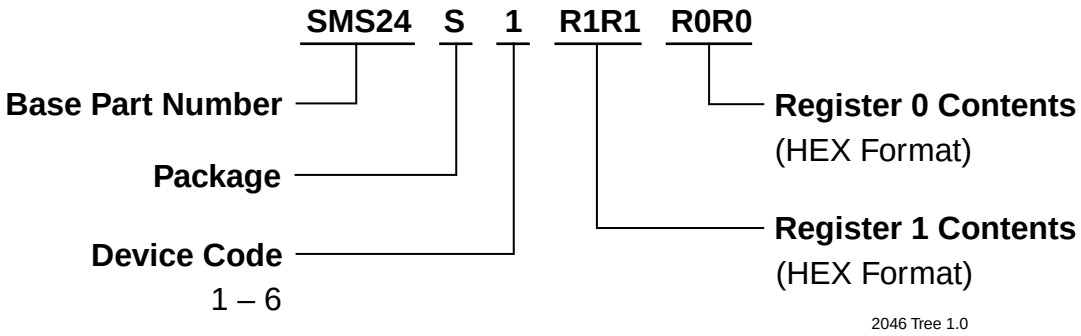
Note 1: Minimum and maximum values for these parameters may change without notice.

PACKAGE

8 PIN SOIC PACKAGE



ORDERING INFORMATION



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