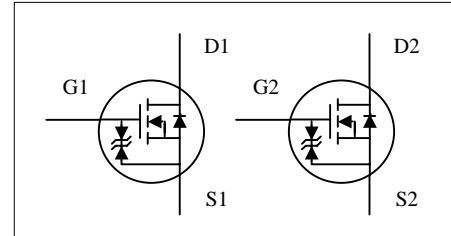


# N-CHANNEL ENHANCEMENT MODE POWER MOSFET

## PRODUCT SUMMARY

- Low on-resistance
- Capable of 2.5V gate drive
- Optimal DC/DC battery application

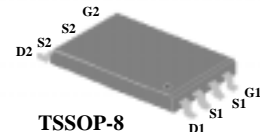


## DESCRIPTION

The Advanced Power MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.

$BV_{DSS}$	20V
$R_{DS(ON)}$	23m $\Omega$
$I_D$	5A

 **Pb-free; RoHS-compliant**



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D @ T_A = 25^\circ C$	Drain Current <sup>3</sup> , $V_{GS}$ @ 4.5V	5	A
$I_D @ T_A = 70^\circ C$	Drain Current <sup>3</sup> , $V_{GS}$ @ 4.5V	3.5	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	25	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	1	W
	Linear Derating Factor	0.008	W/ $^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

## THERMAL DATA

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 125	$^\circ C/W$

**ELECTRICAL CHARACTERISTICS** @T<sub>j</sub>=25° C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.02	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	-	-	23	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =2A	-	-	29	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.5	-	-	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =5A	-	21	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	uA
	Drain-Source Leakage Current (T <sub>j</sub> =70°C)	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±12V	-	-	±10	uA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =5A	-	15.9	-	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =10V	-	1.5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	7.4	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =10V	-	6.2	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =1A	-	9	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =4.5V	-	30	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =10Ω	-	11	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	530	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =20V	-	245	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	125	-	pF

**SOURCE-DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I <sub>S</sub>	Continuous Source Current ( Body Diode )	V <sub>D</sub> =V <sub>G</sub> =0V, V <sub>S</sub> =1.2V	-	-	0.83	A
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	T <sub>j</sub> =25°C, I <sub>S</sub> =5A, V <sub>GS</sub> =0V	-	-	1.2	V

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us , duty cycle ≤2%.
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board ; 208°C/W when mounted on Min. copper pad.

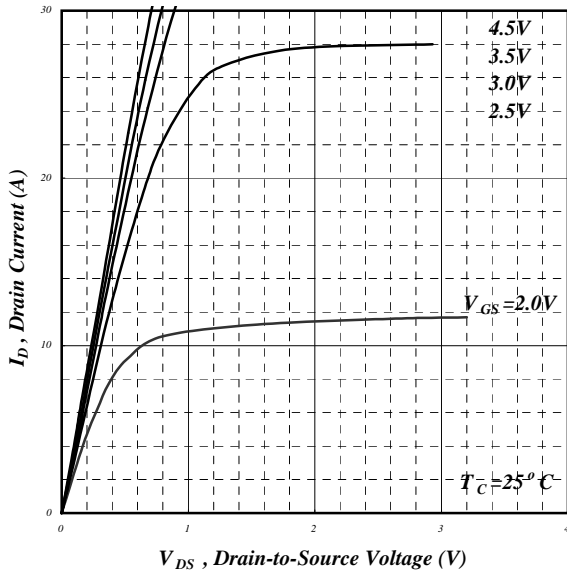


Fig 1. Typical Output Characteristics

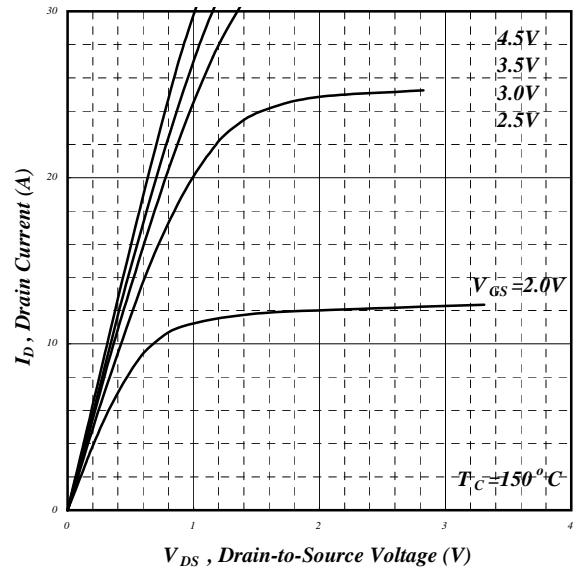


Fig 2. Typical Output Characteristics

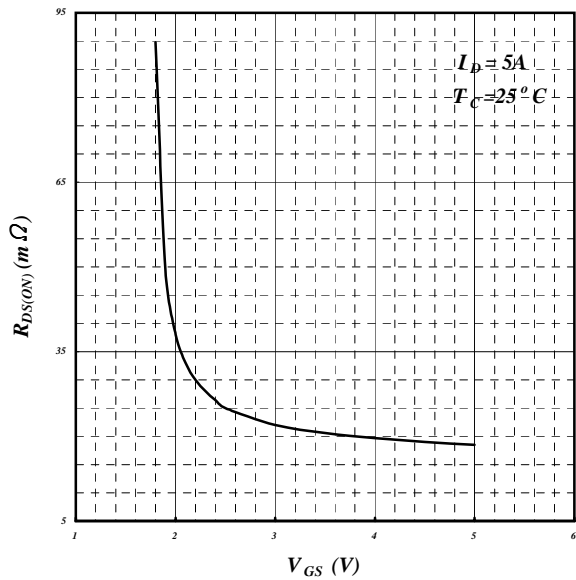


Fig 3. On-Resistance v.s. Gate Voltage

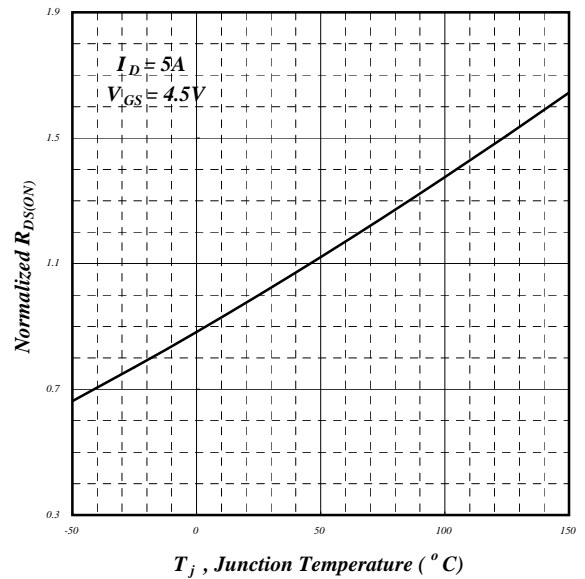


Fig 4. Normalized On-Resistance v.s. Junction Temperature

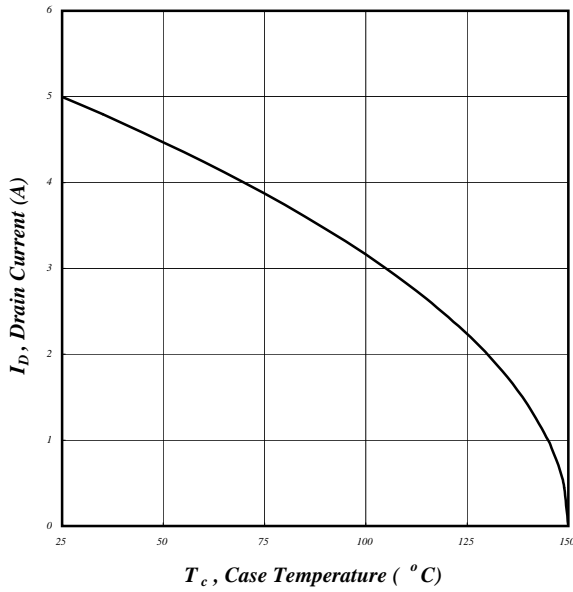


Fig 5. Maximum Drain Current v.s. Case Temperature

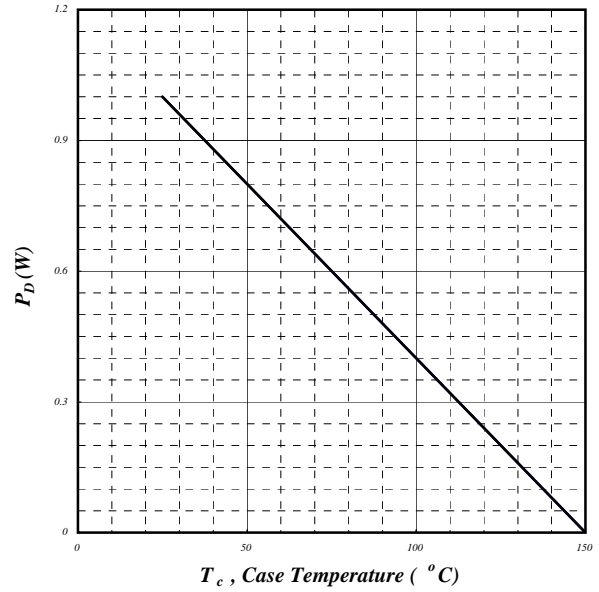


Fig 6. Typical Power Dissipation

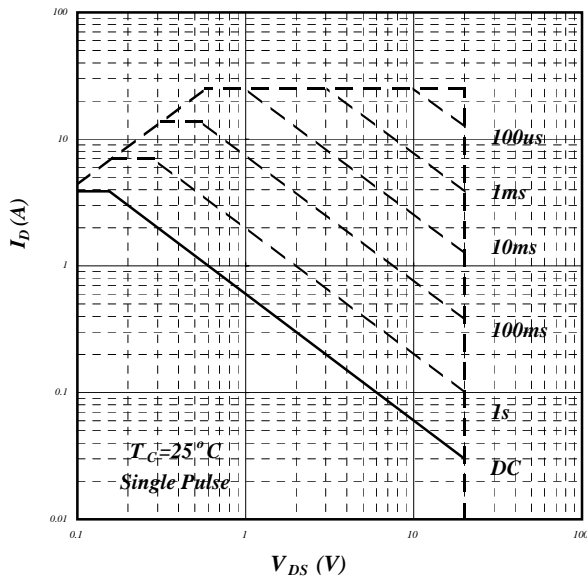


Fig 7. Maximum Safe Operating Area

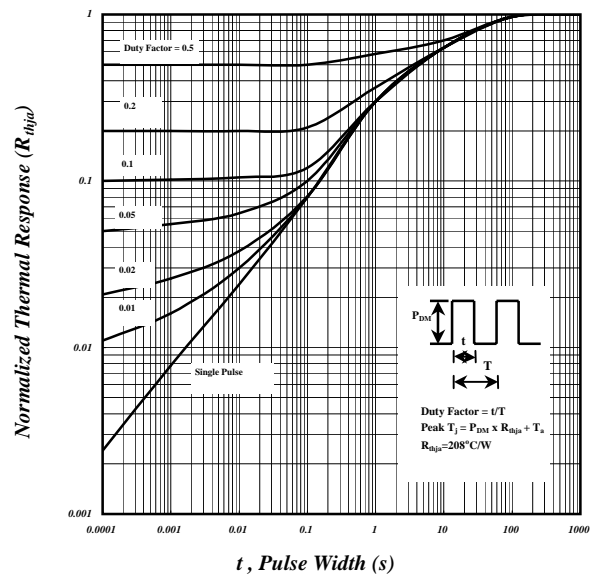


Fig 8. Effective Transient Thermal Impedance

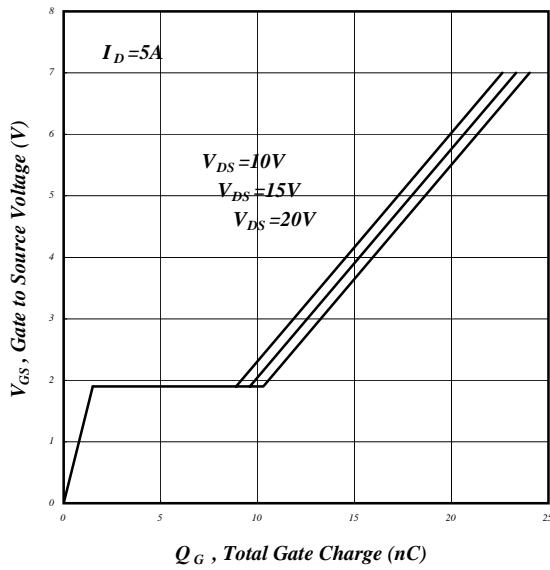


Fig 9. Gate Charge Characteristics

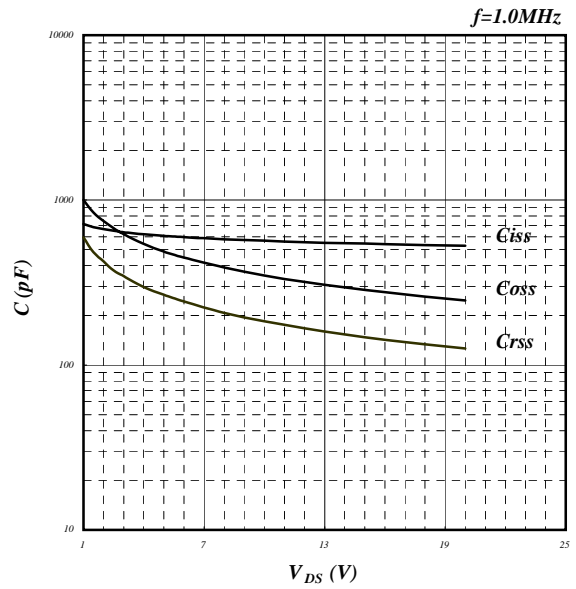


Fig 10. Typical Capacitance Characteristics

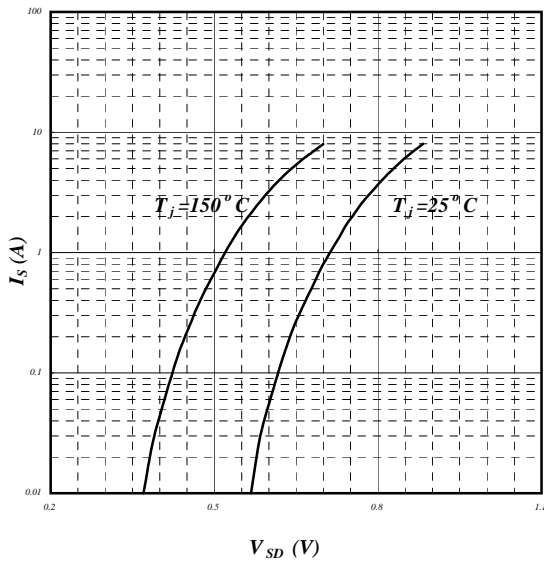


Fig 11. Forward Characteristic of Reverse Diode

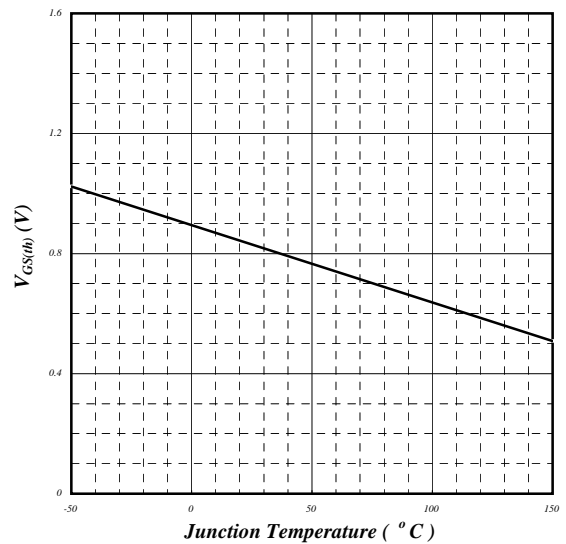


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

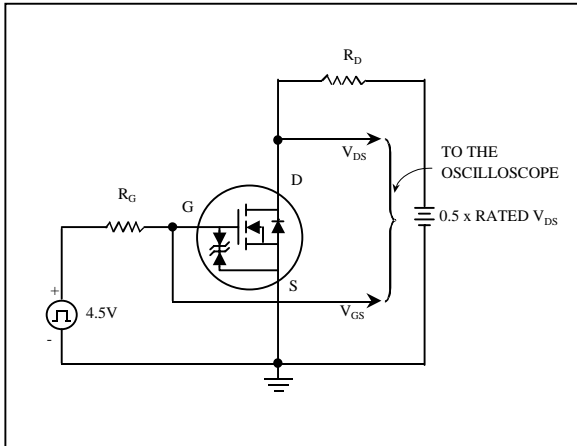


Fig 13. Switching Time Circuit

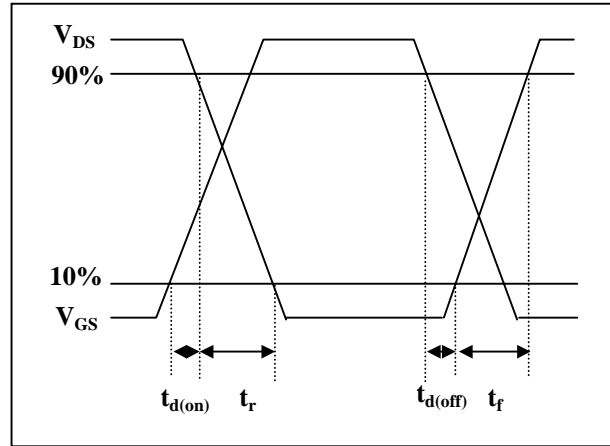


Fig 14. Switching Time Waveform

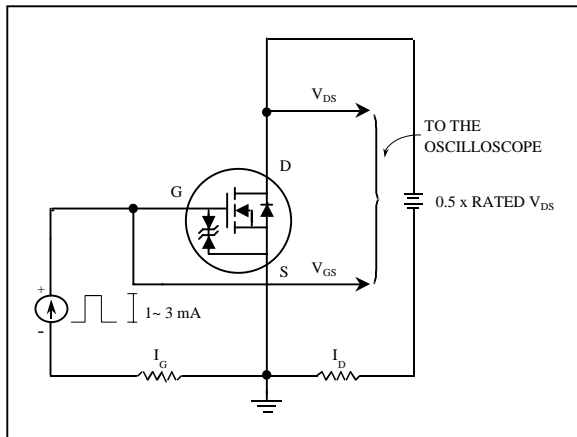


Fig 15. Gate Charge Circuit

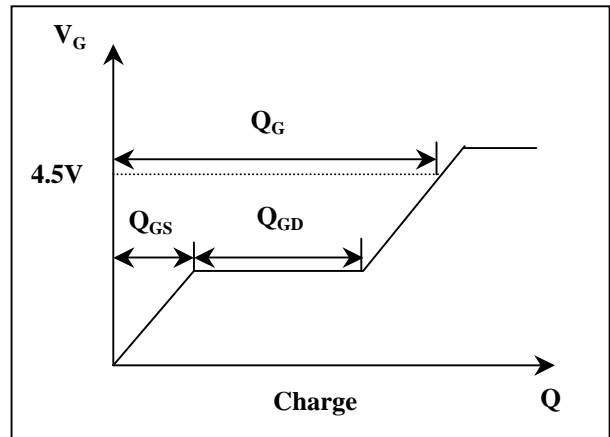


Fig 16. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, expressed or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.