

# PCS3P2191A

#### rev 0.1

#### **Spread Spectrum Clock Generator**

#### Features

- Generates four 4X low EMI spread spectrum clocks
- Input frequency: 15MHz
- Output frequency: 60MHz
- Internal loop filter minimizes external components
   and board space
- Selectable Centre Spread frequency deviation: ±0.5%, ±0.75%, ± 1.0%, ± 1.25%, ± 1.5%, ± 1.75% ± 2.0%
- 3.3V ± 0.3V Operating Voltage
- Commercial Temperature range
- Available in 16-pin TSSOP
- Advanced low power CMOS process

# offers seven selectable centre spread options of $\pm 0.5\%$ to $\pm 2.0\%$ , and a no spread option. (*Refer Spread Deviation Selection Table*). PCS3P2191A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The PCS3P2191A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, and shielding that are traditionally required to pass EMI regulations. The PCS3P2191A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

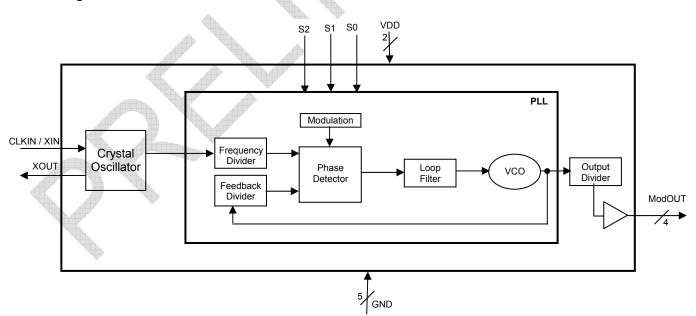
#### Application

PCS3P2191A is targetted for LCD panel application

#### **Product Description**

PCS3P2191A is a versatile spread spectrum frequency modulator that generates four low EMI 4x clocks at the output. PCS3P2191A

#### **Block Diagram**



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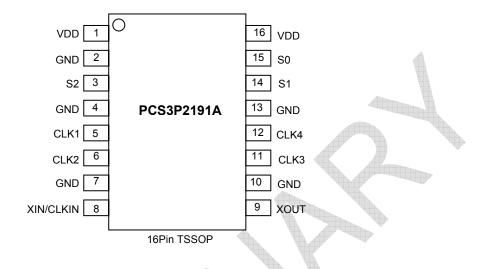


# PCS3P2191A

#### January 2007

## rev 0.1

#### **Pin Configuration**



#### **Pin Description**

Pin#	Pin Name	Туре	Description			
1	VDD	power	Power Supply Voltage Pin. Connect to +3.3V.			
2	GND	power	Ground Connection. Connect to system ground.			
3	S2	Input	Spread range select. Digital logic input used to select frequency deviation (Refer Spread Deviation Table). This pin has an internal pull-up resistor.			
4	GND	power	Ground Connection. Connect to system ground.			
5	CLK1	Output	Low EMI 4x clock output.			
6	CLK2	Output	Low EMI 4x clock output.			
7	GND	power	Ground Connection. Connect to system ground.			
8	XIN/CLKIN	Input	Crystal connection or external reference frequency input. It can be connected to a 15MHz fundamental mode crystal.			
9	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.			
10	GND	power	Ground Connection. Connect to system ground.			
11	CLK3	Output	Low EMI 4x clock output.			
12	CLK4	Output	Low EMI 4x clock output.			
13	GND	power	Ground Connection. Connect to system ground.			
14	S1	Output	Spread range select. Digital logic input used to select frequency deviation (Refer Spread Deviation Table). This pin has an internal pull-up resistor.			
15	SO	Output	Spread range select. Digital logic input used to select frequency deviation (Refer <i>Spread Deviation Table</i> ). This pin has an internal pull-up resistor.			
16	VDD	power	Power Supply Voltage Pin. Connect to +3.3V.			



# PCS3P2191A

rev 0.1

#### **Spread Deviation Selection Table**

S2	S1	S0	Deviation
0	0	0	OFF
0	0	1	± 0.5%
0	1	0	± 0.75%
0	1	1	± 1.0%
1	0	0	± 1.25%
1	0	1	± 1.5%
1	1	0	± 1.75%
1	1	1	± 2.0%

#### **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Unit			
VDD	Supply Voltage pin with respect to Ground	-0.5 to +4.6	V			
V <sub>IN</sub>	Input Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V			
V <sub>OUT</sub>	Output Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V			
T <sub>STG</sub>	Storage temperature	-55 to +125	°C			
Ts	Max. Soldering Temperature (10 sec)	260	°C			
TJ	Junction Temperature	150	°C			
$T_{DV}$	Static Discharge Voltage(As per JEDEC STD22- A114-B)	2	KV			
Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.						

#### **Recommended Operating Conditions**

Parameter	Description	Min	Тур	Max	Unit
VDD	Operating Voltage	3.0	3.3	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	0		+70	°C
CL	Load Capacitance			15	рF
CIN	Input Capacitance		5		pF



PCS3P2191A

rev 0.1

#### **DC Electrical Characteristics**

Symbol	P	Min	Тур	Мах	Unit		
VIL	Input low voltage	VSS – 0.3		0.8	V		
V <sub>IH</sub>	Input high voltage		2.0		VDD+ 0.3	V	
IIL	Input low current				-35	μA	
I <sub>IH</sub>	Input high current				+35	μA	
I <sub>XOL</sub>	$X_{\text{OUT}}$ output low current ( $\$	/ <sub>XOL</sub> @ 0.4V, VDD = 3.3V)		3		mA	
I <sub>XOH</sub>	$X_{\text{OUT}}$ output high current (	V <sub>XOH</sub> @ 2.5V, VDD = 3.3V)		3		mA	
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 12mA	VSS		0.4	V	
V <sub>он</sub>	Output high voltage	I <sub>OH</sub> = -12mA	2.5		VDD	V	
Icc	Dynamic supply current, 6		TBD	1	mA		
I <sub>DD</sub>	Static supply current stand			TBD	uA		
VDD	Operating voltage		3.0	3.3	3.6	V	
t <sub>on</sub>	Power up time (first locked	l clock cycle after power up)**			5	mS	
Z <sub>OUT</sub>	Clock output impedance			TBD		Ω	
C <sub>IN</sub>	Input Capacitance			5		рF	
CL	Load Capacitance				15	pF	
	*CLKIN pulled Low **VDD and CLKIN inputs are stable						

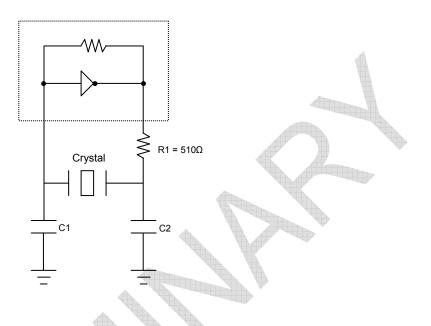
#### **AC Electrical Characteristics**

Symbol	Parameter	Min	Тур	Max	Unit		
XIN/ CLKIN	Input frequency		15		MHz		
CLKOUT	Output frequency (Pin 5,6,11,12)		60(SS)		MHz		
t <sub>LH</sub> *	Output rise time (Measured from 20% to 80%)		TBD		nS		
t <sub>HL</sub> *	Output fall time ( Measured from 80% to 20% )		TBD		nS		
t <sub>JC</sub> *	Cycle to cycle Jitter		TBD		pS		
t <sub>D</sub> *	Output duty cycle	45	50	55	%		
*t <sub>LH</sub> and t <sub>HL</sub> are measured with a capacitive load of 15pF							



rev 0.1

**Typical Crystal Oscillator Circuit** 



## **Typical Crystal Specifications**

Fundamental AT cut parallel resonant crystal				
Nominal frequency	15MHz			
Frequency tolerance	± 50 ppm or better at 25°C			
Operating temperature range	-25°C to +85°C			
Storage temperature	-40°C to +85°C			
Load capacitance	18pF			
Shunt capacitance	7pF maximum			
ESR	25Ω			

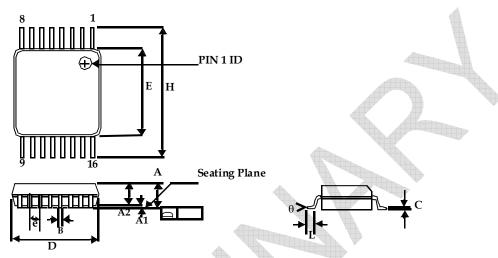
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PCS3P2191A



rev 0.1

Package Information



	Dimensions					
Symbol	Inch	ies	Millimeters			
	Min	Max	Min	Max		
А		0.043		1.20		
A1	0.002	0.006	0.05	0.15		
A2	0.031	0.041	0.80	1.05		
В	0.007	0.012	0.19	0.30		
С	0.004	0.008	0.09	0.20		
D	0.193	0.201	4.90	5.10		
E	0.169	0.177	4.30	4.50		
е	0.026	BSC	0.65 BSC			
Н	0.252 BSC		6.40 BSC			
L	0.020	0.030	0.50	0.75		
θ	0°	8°	0°	8°		

# 16-lead Thin Shrunk Small Outline Package (4.40-MM Body)

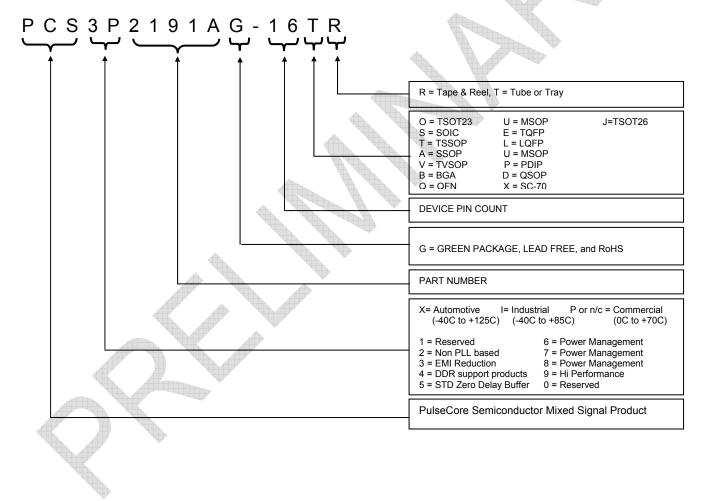


rev 0.1

#### **Ordering Codes**

Part Number	Marking	Package Type	Temperature
PCS3P2191AG-16TT 3P2191AG		16-Pin TSSOP, TUBE, Green	Commercial
PCS3P2191AG-16TR 3P2191AG		16-Pin TSSOP, TAPE & REEL, Green	Commercial
PCS3P2191AF-16TT	3P2191AF	16-Pin TSSOP, TUBE, Pb Free	Commercial
PCS3P2191AF-16TR	3P2191AF	16-Pin TSSOP, TAPE & REEL, Pb Free	Commercial

#### **Device Ordering Information**



Licensed under U.S Patent Nos 5,488,627 and 5,631,921



rev 0.1



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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