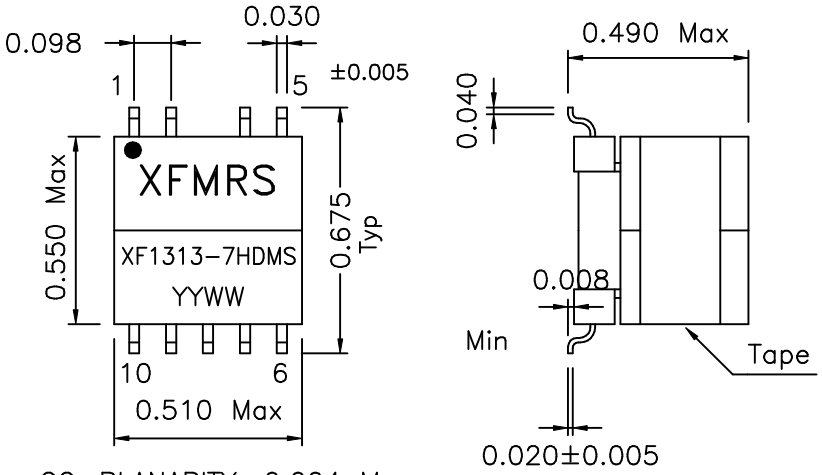
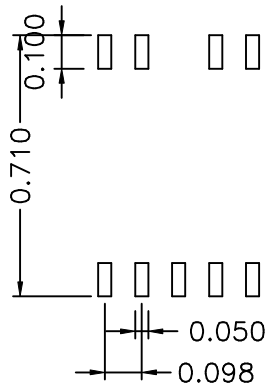
1. Mechanical Dimensions:

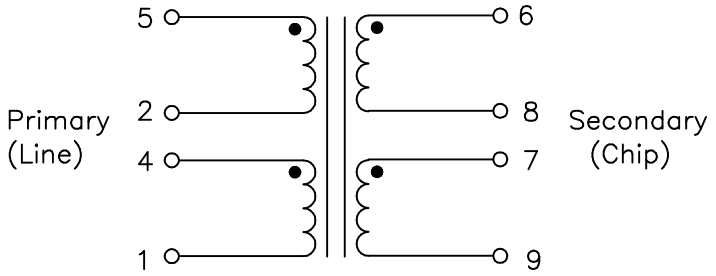


CO-PLANARITY: 0.004 Max



Suggested PCB Layout

2. Schematic:



3. Electrical Specifications:

OCL: (Pins 1-5) 2.0mH ±10% 10KHz, 1.0V 0/100mAdc
(Tie 2+4)

Leakage L: (Pins 1-5) 35.0uH Max 100KHz, 0.1V
Short Pins 9-6, tie 4+2

Cw/w: (Pins5-6) 60pF Max 100KHz, 0.1V
Tie (2+4, 7+8)

Turns Ratio: (5-1):(6-9) 2.3:1, Tie(2+4, 7+8), ±2%

DC Res: (Pins 1-4) 1.86 Ohms ±15%

DC Res.: (Pins 2-5) 1.86 Ohms ±15%

DC Res.: (Pins 6-9)Tie 7+8, 0.90 Ohms ±15%

Long. Bal.: 55dB Min, 20KHz - 560KHz

THD: -80dB Max, 20KHz, 4.95Vrms, 25.5 Ohm Load

HYPOT: 2000VAC Chip-Line

HYPOT: 2000VAC Wdgs-Core

Operating Temp.: -40 to +85°C

Note: Designed to meet the specifications of UL 1950 for supplementary insulation for a primary circuit with 250 working volts.

DOC. REV: A/1

XFMRS Inc	Title: HDSL2 TRANSFORMER		
UNLESS OTHERWISE SPECIFIED TOLERANCES: .xxx ±0.010 Dimensions in INCH	P/N: XF1313-7HDMS		REV. A
	DWN.	BW	Sep-29-99
	CHK.	AEI	Sep-29-99
SHEET 1 OF 1	APP.	Joe Huff	Oct-25-99