Power Operational Amplifiers

RoHS COMPLIANT

FEATURES

- Power Bandwidth 170 V_{P-P}, 2 MHz
- Output Voltage up to 180 Vp-p
- High Slew Rate 2500 V/µs Minimum with A_{CL} = 20
- High Gain Bandwidth Product 180 MHz
- High Output Current ±1.5 A Steady State Within SOA
- High Peak Output Current ±5 A

APPLICATIONS

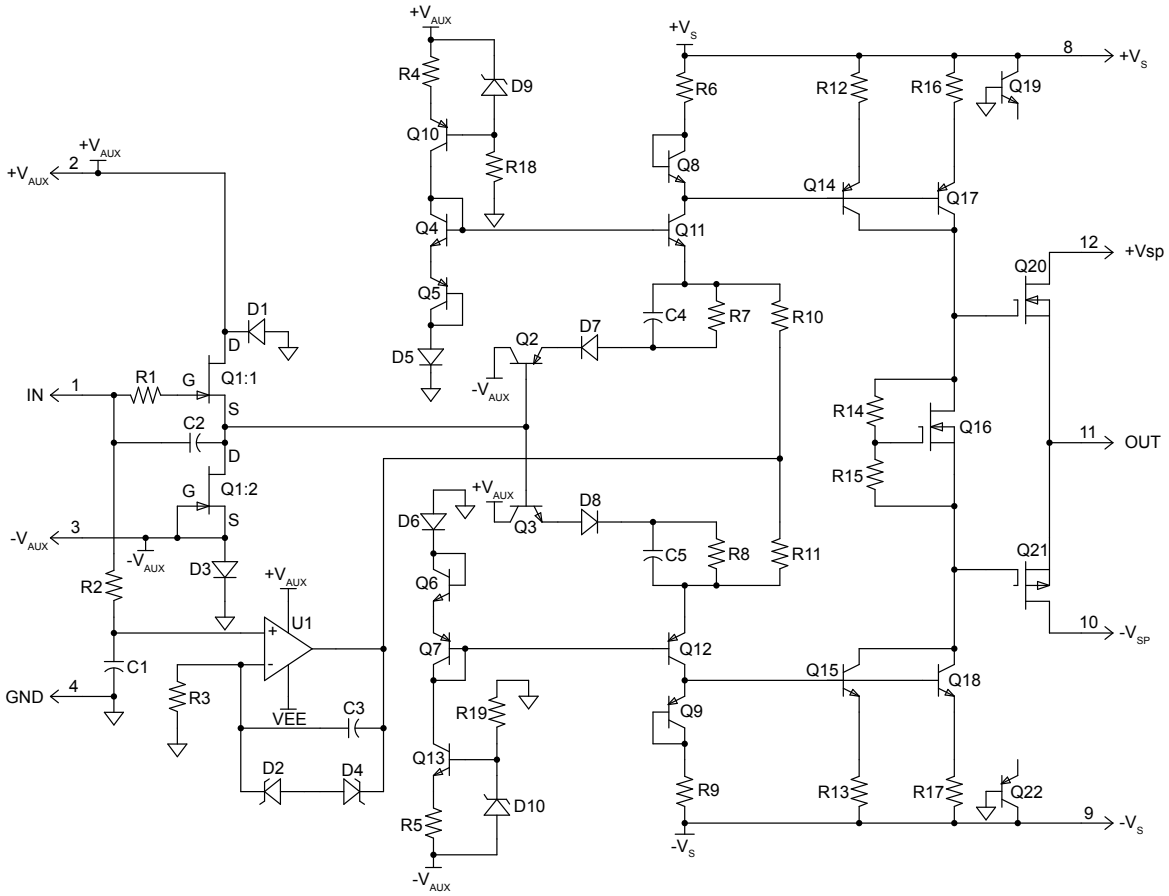
- Piezo Drive
- CRT Beam Intensity Control
- ATE Applications
- Line Driver

GENERAL DESCRIPTION

The PA107DP is a state of the art wideband high power operational amplifier designed to drive resistive, capacitive or inductive loads. For optimum linearity the output stage is biased for class A/B operation. Feed forward technology is used to obtain wide bandwidth and excellent DC performance, but constricts use to inverting mode only. External compensation allows the user to obtain both high gain and wide bandwidth. Use of a heatsink is required to realize the SOA.

This hybrid integrated circuit uses thick film resistors, ceramic capacitors, and semiconductors to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12 pin SIP package occupies only 2 square inches. The use of compressible insulation washers voids the warranty.

EQUIVALENT SCHEMATIC



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$		40	200	V
SUPPLY VOLTAGE, $-V_S$		-20	-100	V
SUPPLY VOLTAGE, $-V_{AUX}$ to $+V_{AUX}$		20	36	V
SUPPLY VOLTAGE, $-V_{AUX}$		-10	-18	V
OUTPUT CURRENT, Steady State, (Within SOA)			1.5	A
OUTPUT CURRENT, peak, (Within SOA)			5	A
POWER DISSIPATION, internal, DC			62.5	W
INPUT VOLTAGE		$-V_{AUX}$ + 2	$+V_{AUX}$ - 2	V
TEMPERATURE, pin solder, 10s			260	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE RANGE, storage		-40	+85	°C
OPERATING TEMPERATURE, case		-25	+85	°C

SPECIFICATIONS

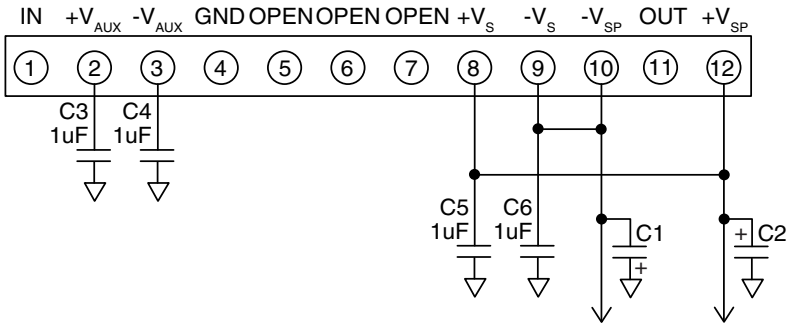
Parameter	Test Conditions	Min	Typ	Max	Units
	V_S = 100V, $-V_S$ = -100V, V_{AUX} = 15V, $-V_{AUX}$ = -15V				
INPUT					
OFFSET VOLTAGE			5	10	mV
OFFSET VOLTAGE vs. temperature			10		µV/°C
BIAS CURRENT, initial (Note 3)			300		pA
INPUT RESISTANCE, DC		13			GΩ
INPUT CAPACITANCE			2		pF
INPUT VOLTAGE RANGE		$-V_{AUX}$ + 2		$+V_{AUX}$ - 2	V
NOISE, RTI	1k source, 500 kHz BW, A_{CL} 101		13		nV/√Hz
GAIN					
OPEN LOOP GAIN @ DC			140		dB
OPEN LOOP GAIN @ 1MHz			40		dB
POWER BANDWIDTH, 170Vp-p	Full temperature range	2			MHz
OUTPUT					
VOLTAGE SWING	10MΩ in parallel with 10 pf		187		V_{P-P}
VOLTAGE SWING	I_O = 1.5A	$\pm V_S$ ±10			V
CURRENT, peak				±5	A
CURRENT, Steady State (within SOA)				±1.5	A
SLEW RATE, 25% to 75%		2500	3000		V/µS
SETTLING TIME to 0.1%			12		µS

Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY					
VOLTAGE, $+V_S$		20		100	V
VOLTAGE, $-V_S$		-100		-20	V
VOLTAGE, $+V_{AUX}$		10	15	18	V
VOLTAGE, $-V_{AUX}$		-18	-15	-10	V
CURRENT, QUIESCENT, $+V_S$		20	30	35	mA
CURRENT, QUIESCENT, $-V_S$		20	30	35	mA
CURRENT, QUIESCENT, $-V_{AUX}$			19	21	mA
CURRENT, QUIESCENT, $+V_{AUX}$			19	21	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 6)				1.5	°C/W
RESISTANCE, DC junction to case				2	°C/W
RESISTANCE, junction to air				30	°C/W
TEMPERATURE RANGE, case		-25		85	°C

NOTES:

1. All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. Doubles for every 10ºC of case temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stages.
5. $+V_{AUX}$ and $-V_{AUX}$ denote the positive and negative supply voltages to the input stages.
6. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

EXTERNAL CONNECTIONS

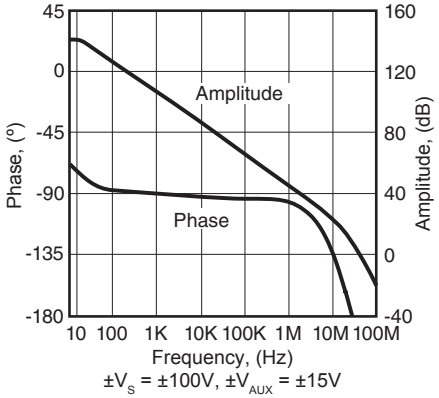


C1-2 = 10uF/A out (peak), electrolytic/tantalum, low frequency bypass.
C3-4 = 1uF 25V X7R ceramic capacitor recomended.
C5-6 = 1uF 200V X7R ceramic capacitor recomended.

12-pin SIP
Package Style DP
Formed leads available
See Package Style EE

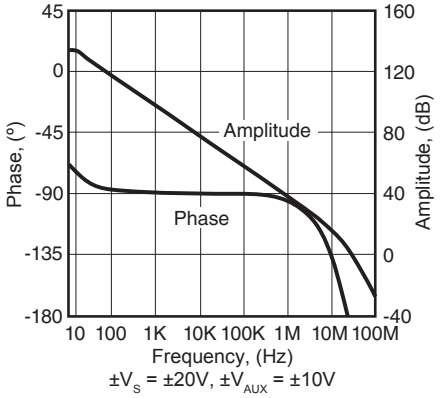
2. TYPICAL PERFORMANCE GRAPHS

HIGH VOLTAGE SMALL SIGNAL RESPONSE



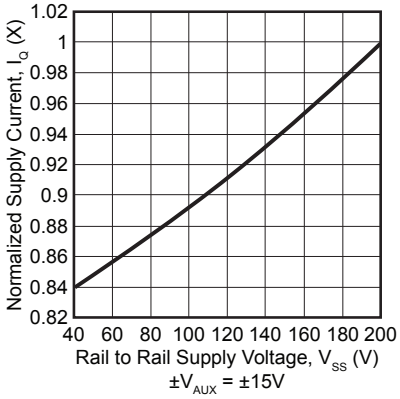
$\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

LOW VOLTAGE SMALL SIGNAL RESPONSE



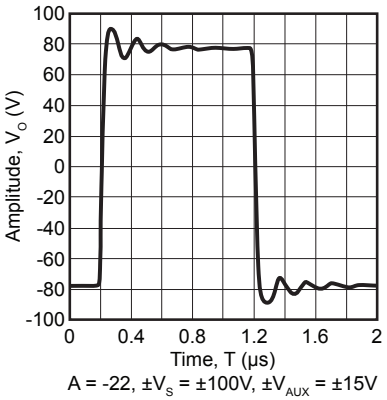
$\pm V_S$ = ±20V, $\pm V_{AUX}$ = ±10V

HIGH VOLTAGE SUPPLY CURRENT



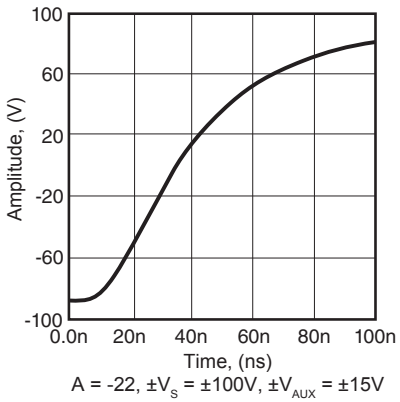
$\pm V_{AUX}$ = ±15V

RESPONSE to 500KHz SQUARE WAVE



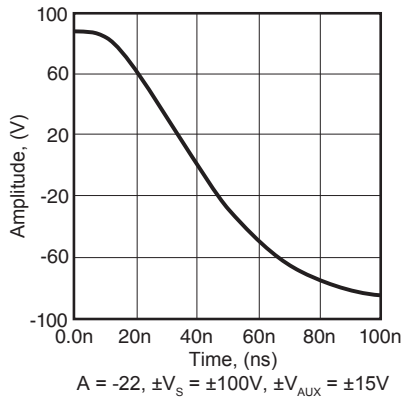
A = -22, $\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

POSITIVE SLEW



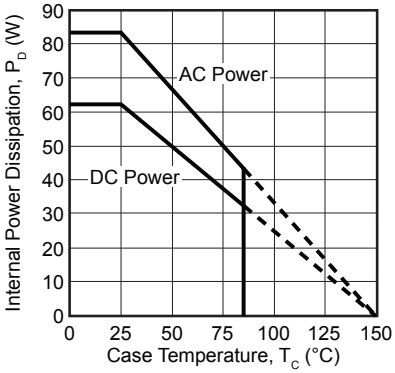
A = -22, $\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

NEGATIVE SLEW

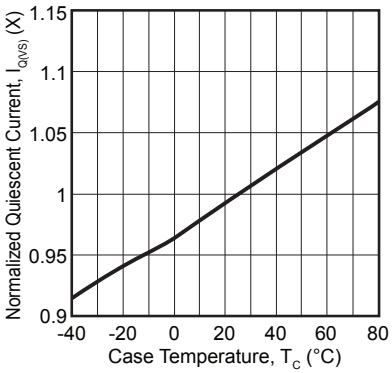


A = -22, $\pm V_S$ = ±100V, $\pm V_{AUX}$ = ±15V

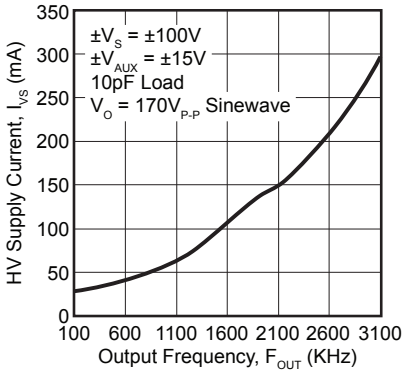
POWER DERATING



HIGH VOLTAGE CURRENT vs. TEMPERATURE



HIGH VOLTAGE CURRENT vs. FREQUENCY



PIN DESCRIPTIONS

Pin #	Pin name	Description
1	IN	Summing Junction Input for Inverting Operational Amplifier
2	$+V_{AUX}$	+10V to +18V Supply for Input Circuits
3	$-V_{AUX}$	-10V to -18V Supply for Input Circuits
4	GND	Ground
5		Open Pin
6		Open Pin
7		Open Pin
8	$+V_S$	+20V to +100V Supply for Gain and Gate Driver Circuits
9	$-V_S$	-20V to -100V Supply for Gain and Gate Driver Circuits
10	$-V_{SP}$	-20V to -100V Supply for Output Source Follower
11	OUT	High Power Output of Amplifier
12	$+V_{SP}$	+20V to +100V Supply for Output Source Follower

3. GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

CAUTION

In order to achieve the highest speed with limited space short circuit protection and thermal protection were sacrificed. Do not short the output. Note that if current limiting at 1.5 A could be used, and the output was shorted, internal dissipation would be 150 W. This would still destroy the amplifier, albeit more slowly.

4. INTERNAL POWER DISSIPATION AND HEATSINK SELECTION

With the unique combination of high voltage and speed of the PA107, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of this amplifier. To more accurately predict operating temperatures use Power Design1 revision 10 or higher, or use the following procedure:
Find internal dissipation (PD) resulting from driving the load. Use Power Design or refer to Apex Applications Note 1, General Operating Considerations, paragraph 7. Find total quiescent power (PD_Q) by multiplying 0.035 A by V_{SS} (total supply voltage), plus 0.021 times the total V_{AUX} ($+V_{AUX} + |-V_{AUX}|$). Find output stage quiescent power (PD_{QOUT}) by multiplying 0.001 by V_{SS}.
Calculate a heatsink rating which will maintain the case at 85°C or lower.

$$R_{\O SA} = \frac{T_C - T_A}{PD + PD_Q} \text{ -0.1°C/W}$$

Where:
T_C = maximum case temperature allowed
T_A = maximum ambient temperature encountered

$$R_{\O SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) \bullet R_{\O JC}}{PD + PD_Q} \text{ -0.1°C/W}$$

Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower.
Where:
T_J = maximum junction temperature allowed.
$R_{\O JC}$ = AC or DC thermal resistance from the specification table.
Use the larger heatsink of these two calculations.
Power Design is an Excel spreadsheet available free from www.cirrus.com

5. REACTIVE LOADS

The PA107DP is stable at a gain of 20 or above when driving either inductive or capacitive loads. However an inductor is essentially a short circuit at DC, therefore there must be enough resistance in series to keep low frequency power within ratings.

When driving a 1nF capacitive load with a 180 V_{P-P} square wave, the current peak is 1 A. Driving the same capacitor with a 2.3 MHz sine wave, the power bandwidth frequency, results in 2.6 A_{P-P}. The power dissipated in the amplifier while driving a purely capacitive load is given by the formula:

$$P = 2V_{PK}V_S/\pi X_C$$
$$P = 2I_{PK}V_S/\pi$$

Where:

V_{PK} = Peak Voltage
V_S = Supply Voltage
X_C = Capacitive Reactance

Notice that the power increases as V_{PK} increases, such that the maximum internal dissipation occurs when V_{PK} is maximum. The power dissipated in the amplifier while driving 1 nF at 2.3 MHz would be 82.76 W. This would not be a good thing to do! But driving 1 nF at 1 MHz at 180V_{P-P} would result in 36.0 W, which could be within the AC power rating.

This formula is optimistic; it is derived for an ideal class B amplifier output stage.

6. FEEDBACK CONSIDERATIONS

The output voltage of an unloaded PA107DP can easily go as high as 95 V. All of this voltage can be applied across the feedback resistor, so the minimum value of a ½ W resistor in the feedback is 18050Ω. Practically, 20K is the minimum value for a un-derated ½ W feedback resistor.

In order to provide the maximum slew rate, power bandwidth, and useable gain bandwidth; the PA107DP is not designed to be unity gain stable. It is necessary to add external compensation for gains less than 20. Often lower performance op-amps may be stabilized with a capacitor in parallel with the feedback resistor. This is because there is effectively one additional pole affecting the response. In the case of the PA107DP, however there are multiple poles clustered near 30 MHz, therefore this approach does not work. A method of compensation that works is to choose a feedback capacitor such that the time constant of the feedback capacitor times the feedback resistor is greater than 33 n-seconds. Also install a capacitor from pin 1 to ground, the summing junction, greater than 20 times as large as the feedback capacitor. The feedback capacitor or summing junction capacitor without the other will degrade stability and often cause oscillation. With the compensation described the closed loop bandwidth will be the reciprocal of $2\pi\tau_{FB}$.

Alternatively, at the expense of noise and offset, the amplifier can be stabilized by a resistor across the summing junction such that the parallel combination of the input resistor and summing junction resistor is less than a twentieth of the value of the feedback resistor. Note that this will increase noise and offset by to 20 times the RTI values, but with 10 mV max offset and 13 nV/$(Hz)^{1/2}$ noise, performance will be acceptable for many applications.

As seen by the very small values of capacitance used in compensation for low gain, stray feedback capacitance and/or summing junction capacitance can have a VERY large effect on performance. Therefore stray capacitance must be minimized in the layout. The summing junction lead must be as short as possible, and ground plane must be kept away from the summing junction lead.

7. SLEW RATE AND FULL POWER BANDWIDTH

In the PA107DP the slew rate is measured from the 25% point to the 75% point of a 180V_{P-P} square wave. Slew rate is measured with no load and with auxiliary supplies at a nominal ±15 V and V_S supplies at a maximum ±100V.

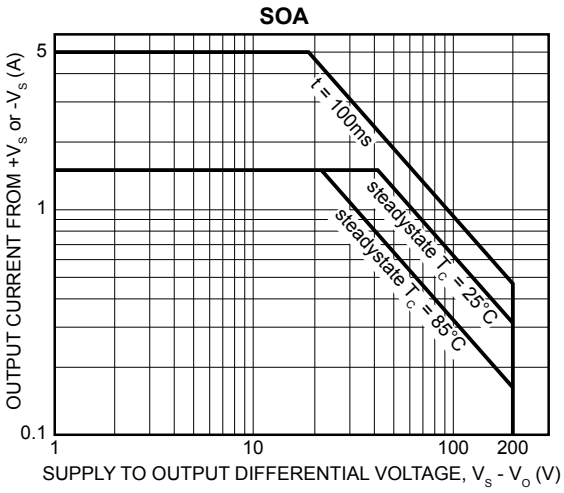
Power bandwidth is defined as the highest frequency at which an unloaded amplifier can have an undistorted sine wave at full power as its output. This frequency can be calculated as the slew rate divided by π times the peak to peak amplitude; which would be 4.7 MHz for the PA107DP. Unfortunately running full output at this frequency causes internal dissipation of up to 107 W, well over the power limits for the PA107DP. Cutting the frequency to 2 MHz reduces internal dissipation to 34 W, acceptable with a good heatsink.

8. SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

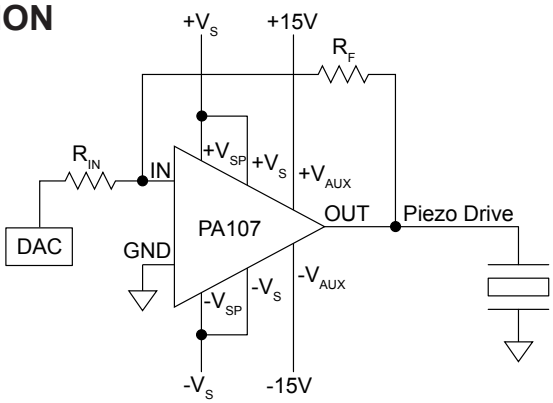
NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



9. SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

10. TYPICAL APPLICATION



CONTACTING CIRRUS LOGIC SUPPORT

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International customers can also request support by contacting their local Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com