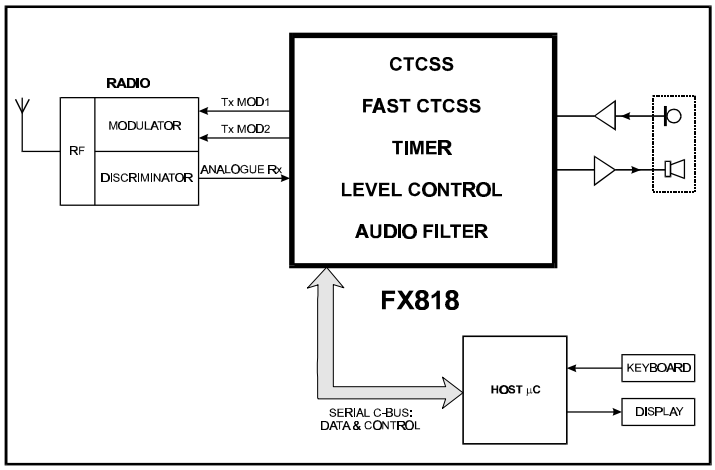
CML Semiconductor Products

CTCSS Signalling Processor FX818

D/818/4 July 1997
Provisional Issue

1.0 Features

- **Fast CTCSS Detection**
- **Non Predictive Tone Detection**
- **Low Power 3.3V/5V Operation**
- **Variable Gain Audio Filter**
- **Programmable Tone Decoder**
- **Programmable Modulator Drivers**
- **Programmable Tone Encoders**
- **Compact (SSOP and SOIC) Packaging**



1.1 Brief Description

The FX818 is an innovative CTCSS Codec designed for the latest generation of Land Mobile Radio equipment. The FX818 is full duplex and has many advanced features which assist the operation of modern CTCSS based systems. The FX818 is electrically, physically and software compatible with the FX828. It permits manufacturers to add new features to their equipment with minimal design changes.

The FX818 incorporates a programmable tone decoder which can be set to respond to between 1 and 15 CTCSS tones with minimum software intervention. In addition, a 'Fast' CTCSS detector can respond to a single programmed tone in 60ms, or can be used to provide an output if any CTCSS tone is present at the detector input. A high resolution tone encoder performs accurate generation of any CTCSS tone in current use. High pass and low pass filters are included to provide filtering for CTCSS and Voice band signals. On chip audio summation amplifier and digital adjustable modulator drivers ensure easy integration into equipment.

The FX818 along with the FX828 is offered in a choice of small SSOP and SOIC 24-pin packages. It may be used with 3.0 to 5.5 volt supply.

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Note: As this product is still in development, it is likely that a number of changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

1.2 Block Diagram

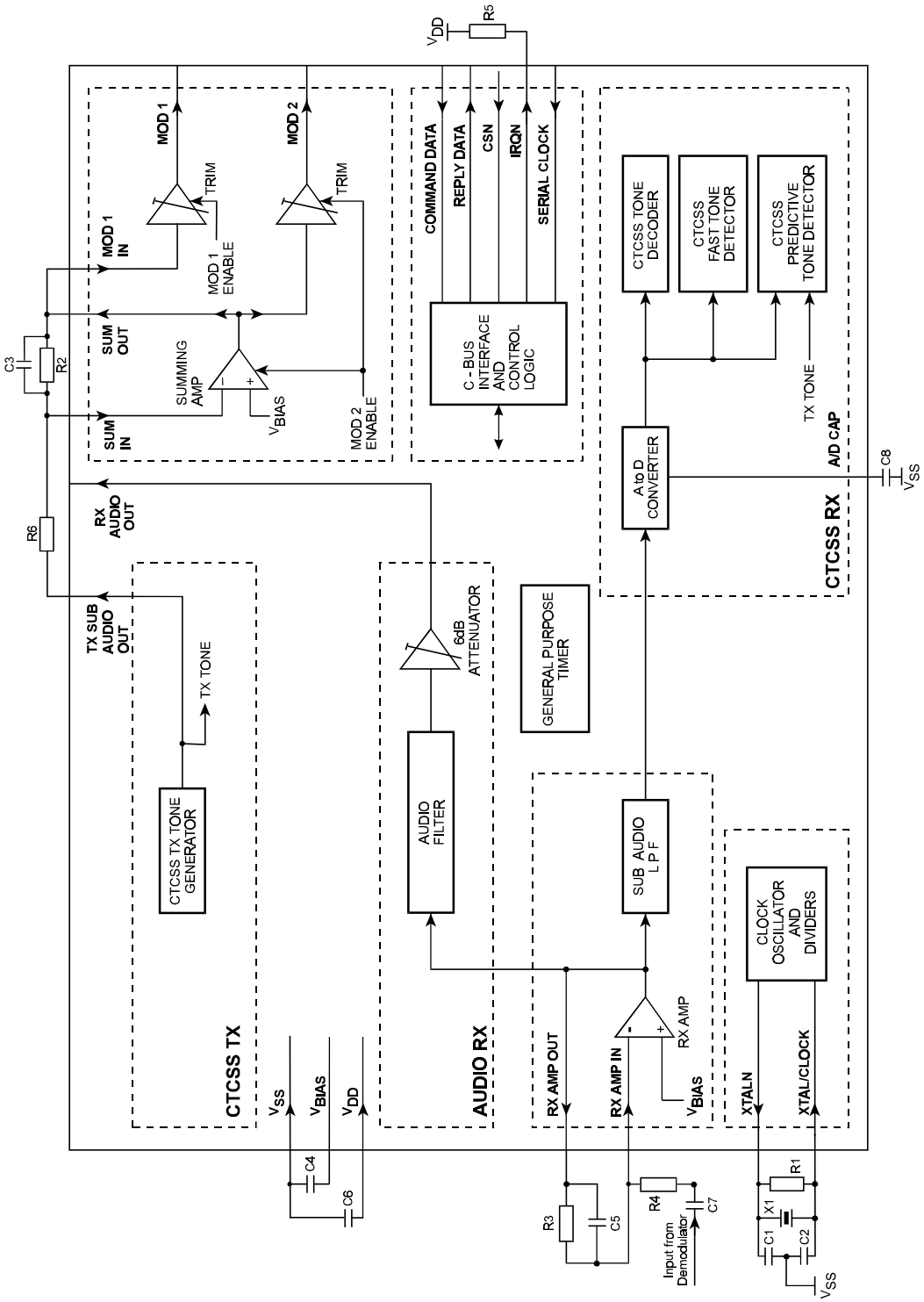

Figure 1 Block Diagram

1.3 Signal List

Package D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	I/P	The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See "C-BUS" Timing Diagram (Figure 4).
4	COMMAND DATA	I/P	The "C-BUS" serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronised to the SERIAL CLOCK. See "C-BUS" Timing Diagram (Figure 4).
5	REPLY DATA	O/P	The "C-BUS" serial data output to the µController. The transmission of REPLY DATA bytes is synchronised to the SERIAL CLOCK under the control of the CSN input. This 3-state output is held at high impedance when not sending data to the µController. See "C-BUS" Timing Diagram (Figure 4).
6	CSN	I/P	The "C-BUS" data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CSN signal. See "C-BUS" Timing Diagram (Figure 4).
7	IRQN	O/P	This output indicates an interrupt condition to the µController by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.

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1.3 Signal List (continued)

Package D2/D5	Signal		Description
Pin No.	**Name**	**Type**	
8 9	NC NC		) No internal connection. Do not make) any connection to these pins.
10	A/D CAP	O/P	An internal reference voltage for the A to D, decoupled to V_{SS} by an external capacitor.
11	NC		No internal connection. Do not make any connection to this pin.
12	V_{SS}	Power	The negative supply rail (ground).
13	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. This pin must be decoupled by a capacitor mounted close to the device pins.
14	RX AMP IN	I/P	The inverting input to the Rx input amplifier.
15	RX AMP OUT	O/P	The output of the Rx input amplifier and the input to the audio filter section.
16	RX AUDIO OUT	O/P	Output of the Rx audio filter section.
17	NC		No internal connection. Do not make any connection to this pin.
18	SUM IN	I/P	Input to the audio summing amplifier.
19	SUM OUT	O/P	Output of the audio summing amplifier.
20	MOD1 IN	I/P	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	O/P	Output of the CTCSS tone generator.
22	MOD1	O/P	Output of MOD1 audio gain control.
23	MOD2	O/P	Output of MOD2 audio gain control.
24	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes: I/P = Input
O/P = Output

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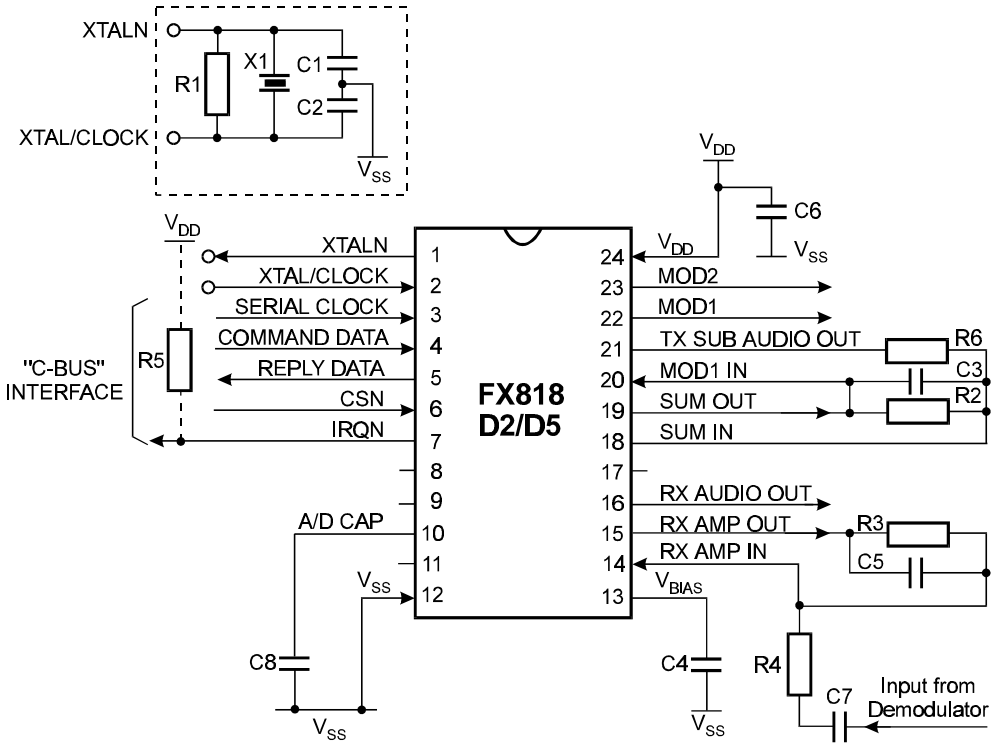
1.4 External Components



C1	22pF	±20%	R1	1MΩ	±5%	X1	4.032MHz	±100ppm
C2	22pF	±20%	R2	100kΩ	±10%			
C3	100pF	±20%	R3	100kΩ	±10%			
C4	0.1µF	±20%	R4	Note 2	±10%			
C5	100pF	±20%	R5	22kΩ	±10%			
C6	0.1µF	±20%	R6	Note 1	±10%			
C7	Note 2	±20%						
C8	0.1µF	±20%						

Notes: 1. R2, R6 and C3 form the gain components for the Summing Amplifier. R6 should be chosen as required from the system specification, using the following formula:

$$\text{Tx Sub Audio Gain} = -\frac{R2}{R6}$$

2. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:

$$\text{Gain} = -\frac{R3}{R4}$$

C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.

Figure 2 Recommended External Components

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1.5 General Description

The FX818 is a programmable CTCSS sub-audio encoder/decoder for use in land mobile radio equipment, see Figure 1.

The receiver section of the FX818 has a fast/predictive tone detector which operates in parallel with a tone decoder. The latter decodes a user-programmable set of up to 15 tones and performs a more accurate (but slower) analysis of the tones detected by the fast/predictive tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

The high pass audio filter is designed to filter out the CTCSS sub-audio tones. The summing and modulation amplifiers allow the audio modulation to be controlled digitally via the C-BUS. A general purpose timer is included.

Each function, and the routing of signals, is flexible and may be configured or controlled by the user's software.

1.5.1 Software Description

Address/Commands
Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 4.

Instruction and data transactions to and from the FX818 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data (1 or 2 bytes) or
(ii) a status or Rx data reply (1 byte)

8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SUB-AUDIO CONTROL	CTCSS TX ENABLE	CTCSS DECODER ENABLE	CTCSS FAST DETECT ENABLE	0	0	0	0	0
$82	SUB-AUDIO SET-UP	CTCSS DECODER BANDWIDTH MSB BIT 3	CTCSS DECODER BANDWIDTH BIT 2	CTCSS DECODER BANDWIDTH BIT 1	CTCSS DECODER BANDWIDTH LSB BIT 0	FAST CTCSS MODE DETECT/ PREDICTIVE	0	0	0
$88	GENERAL CONTROL	BPF ENABLE	**B**PF UN-MUTE	BPF 6dB PAD	0	0	0	TIMER ENABLE	TIMER RE-CYCLE
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER MSB BIT 7	GENERAL PURPOSE TIMER BIT 6	GENERAL PURPOSE TIMER BIT 5	GENERAL PURPOSE TIMER BIT 4	GENERAL PURPOSE TIMER BIT 3	GENERAL PURPOSE TIMER BIT 2	GENERAL PURPOSE TIMER BIT 1	GENERAL PURPOSE TIMER LSB BIT 0
$8E	IRQ MASK	0	GPT IRQ MASK	0	0	CTCSS IRQ MASK	CTCSS FAST IRQ MASK	0	0

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16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$83	CTCSS TX/ FAST RX FREQUENCY (1)	CTCSS (TX) NOTONE	0	0	CTCSS TX / FAST RX FREQUENCY MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/ FAST RX FREQUENCY (2)	CTCSS TX / FAST RX FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$84	CTCSS RX PROGRAM (1)	CTCSS TONE ADDRESS MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	CTCSS FREQUENCY MSB BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS RX PROGRAM (2)	CTCSS FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8A	AUDIO CONTROL (1)	0	0	MOD 1 ENABLE	MOD 1 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
	AUDIO CONTROL (2)	0	0	MOD 2 ENABLE	MOD 2 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Write Only Register Description

GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME	HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
SUB-AUDIO CONTROL	$80	0	0	0	0	0	0	0	0
SUB-AUDIO STATUS	$81	0	0	0	0	X	X	X	X
SUB-AUDIO SET-UP	$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX (1) FREQUENCY	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX (2) FREQUENCY		0	0	0	0	0	0	0	0
CTCSS RX PROGRAM (1)	$84	0	0	0	0	0	0	0	0
CTCSS RX PROGRAM (2)		0	0	0	0	0	0	0	0
GENERAL CONTROL	$88	0	0	0	0	0	0	0	0
AUDIO CONTROL (1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL (2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER	$8B	0	0	0	0	0	0	0	0
IRQ MASK	$8E	0	0	0	0	0	0	0	0
IRQ FLAG	$8F	0	0	0	0	0	0	0	0

X = undefined

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SUB-AUDIO CONTROL Register (Hex address $80)
This register is used to control the functions of the device as described below:

CTCSS TX ENABLE and DECODER ENABLE (Bits 7 and 6)

These two bits enable and disable the CTCSS decoder (Rx) or transmitter (Tx) according to the table below:

Tx Bit 7	Rx Bit 6	Function
0	0	Tx disabled, Rx disabled
0	1	Tx disabled, Rx enabled
1	0	Tx enabled, Rx disabled
1	1	Tx enabled, Rx enabled

CTCSS FAST DETECT ENABLE (Bit 5)

When this bit is "1", the "FAST CTCSS DETECT" or "FAST CTCSS PREDICTIVE" mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SUB-AUDIO SET-UP Register, $82). When this bit is "0", both "FAST CTCSS DETECT" and "FAST CTCSS PREDICTIVE" tone detectors are disabled.

(Bits 4, 3, 2, 1 and 0)

Reserved for future use. These bits should be set to "0".

SUB-AUDIO SET-UP Register (Hex address $82)
This register is used to define the CTCSS parameters, as described below:

CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4)

These four bits set the bandwidth of the CTCSS tone decoder according to the table below:

				BANDWIDTH	
Bit 7	Bit 6	Bit 5	Bit 4	Will Decode	Will Not Decode
1	0	0	0	±1.1%	±2.4%
1	0	0	1	±1.3%	±2.7%
1	0	1	0	±1.6%	±2.9%
1	0	1	1	±1.8%	±3.2%
1	1	0	0	±2.0%	±3.5%
1	1	0	1	±2.2%	±3.7%
1	1	1	0	±2.5%	±4.0%
1	1	1	1	±2.7%	±4.2%

FAST CTCSS MODE (Bit 3)

When CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is "1", this bit selects the "FAST CTCSS DETECT" or the "FAST CTCSS PREDICTIVE" mode, according to the table below:

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DETECT/ PREDICTIVE Bit 3	Function
0	DETECT mode
1	PREDICTIVE mode

If the CTCSS FAST DETECT ENABLE bit is "0" then both modes are deselected.

(Bits 2, 1 and 0) Reserved for future use. These should be set to "0".

GENERAL CONTROL Register (Hex address $88)
This register is used to control the functions of the device as described below:

BPF ENABLE (Bit 7) When this bit is "1" the audio band-pass filter is enabled. When this bit is "0" the audio band-pass filter is disabled (powersaved).

BPF UN-MUTE (Bit 6) When this bit is "1" the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is "0" the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state.

This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.

BPF 6dB PAD (Bit 5) When this bit is "1" a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is "0" the output of the audio band-pass filter is not attenuated.

(Bits 4, 3 and 2) Reserved for future use. These should be set to "0".

TIMER ENABLE (Bit 1) When this bit goes to a "1" the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is "0" the count down is disabled and the last pre-programmed value is retained in the timer's internal register.

TIMER RE-CYCLE (Bit 0) When this bit is "1" the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles.

When this bit is "0" the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B).

If this bit is switched from "1" to "0" whilst the timer is enabled then the timer will complete the present count before stopping.

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GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)
This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (1ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to "1". An interrupt is generated on the IRQN pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is "1" otherwise the GPT IRQ FLAG remains set to "1" and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is "1" then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is "0" then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with "0" will cause the timer circuitry to be disabled (i.e. powersaved).

IRQ MASK Register (Hex address $8E)
This register is used to control the interrupts (IRQs) as described below:

(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These should be set to "0".
GPT IRQ MASK (Bit 6)	When this bit is set to "1" it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
CTCSS IRQ MASK (Bit 3)	When this bit is set to "1" it enables an interrupt that occurs when CTCSS IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
CTCSS FAST IRQ MASK (Bit 2)	When this bit is set to "1" it enables an interrupt that occurs when CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.

CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)
This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, the bits 0 to 12 define the receive frequency the fast predictive detector is looking for according to the formula below.

When the CTCSS transmitter is enabled, the bits 0 to 12 control the frequency of the transmitted CTCSS tones according to the formula below.

When the fast detector and the transmitter are both enabled, the bits 0 to 12 define the receive frequency the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula below (i.e. Tx tone = predictive tone).

$$A = \frac{f_{XTAL}\,(Hz)}{16 \times f_{TONE}\,(Hz)}$$

where A is the binary number programmed into the 13 bits.

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When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT.

CTCSS RX PROGRAM Register (Hex address $84)
This is a 16-bit register. Byte (1) is sent first. The two bytes are used to program the centre frequencies of up to 15 tones in the sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								**Byte 2**							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	0	<---------- N ---------->				<---------- R ---------->							
0	0	0	1												
0	0	1	0												
0	0	1	1												
0	1	0	0												
0	1	0	1	N is the binary representation of the				R is the nearest 6-bit binary							
0	1	1	0	following decimal number (n):				representation of (r), where:							
0	1	1	1												
1	0	0	0	n = INT (948982 x f_{TONE} / f_{XTAL})				r = ((237245/f_{XTAL}) - (n/(4 x f_{TONE}))) x 8400							
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0												
1	1	0	1												
1	1	1	0												

Example: To program 100Hz when using the recommended 4.032MHz Xtal.

n = INT (948982 x 100 / 4.032 x 10^6)
= INT (23.536) = 23
N = 010111 (binary)

r = ((237245 / 4.032 x 10^6) - (23 / (4 x 100))) x 8400
= 11.26 (round up if exactly halfway)

R = 11
= 001011 (binary)

Thus the 12-bit code is 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

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AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the six least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

BYTE 1

5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

BYTE 2

5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte) When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved).

MOD2 ENABLE (Bit 5, second byte) When this bit is "1" the MOD2 attenuator and the SUMMER AMP are enabled. When this bit is "0" they are both disabled (i.e. powersaved).

(Bits 7 and 6, first and second bytes) Reserved for future use. These should be set to "0"

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8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$81	SUB-AUDIO STATUS	0	CTCSS FAST TONE	0	TONE DECODE	CTCSS RX TONE MSB BIT 3	BIT 2	BIT 1	LSB BIT 0
$8F	IRQ FLAG	0	GP TIMER IRQ FLAG	0	0	CTCSS IRQ FLAG	CTCSS FAST IRQ FLAG	0	0

Read Only Register Description

SUB-AUDIO STATUS Register (Hex address $81)
This register is used to indicate the status of the device as described below:

(Bit 7) Reserved for future use. This will be set to "0" but should be ignored by user's software.

CTCSS FAST TONE (Bit 6) When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to "1" if a periodic tone is detected. If no periodic tone is detected this bit will be "0".

When bits 5 and 3 are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to "1" if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX Register is detected. If no match is found this bit will be "0".

When Bit 5 in the SUB-AUDIO CONTROL Register is set to "0" this bit will be "0".

(Bit 5) Reserved for future use. This will be set to "0" but should be ignored by the user's software.

TONE DECODE (Bits 4) This bit indicates the status of the tone decoder. A "1" indicates a tone has been detected (TONE DECODE) and a "0" indicates the loss of the tone (NOTONE).

TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SUB-AUDIO SET-UP Register bits 7, 6, 5 and 4) and the CTCSS RX TONE number (See SUB-AUDIO STATUS Register bits 3, 2, 1 and 0).

When Bit 6 in the SUB-AUDIO CONTROL Register is set to "0" the TONE DECODE bit 4 will be set to "0".

Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of "1111" in bits 3, 2, 1 and 0; indicting a valid, but unrecognised, tone. Loss of tone will cause the NOTONE timer to be started. If loss of tone continues for the duration of the timeout period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.

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CTCSS RX TONE (Bits 3, 2, 1 and 0) These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the CTCSS tone decoded according to the tones programmed in the CTCSS RX PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SUB-AUDIO SET-UP Register, $82) and CTCSS FREQUENCY (Bits 11 - 0, CTCSS RX PROGRAM Register, $84).

IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as below:

(Bits 7, 5, 4, 1 and 0) Reserved for future use. These will be set to "0" but should be ignored by user's software.

GPT IRQ FLAG (Bit 6) When the general purpose timer has reached zero in its internal register, this bit will be set to "1" to indicate the timeout has expired. This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).

CTCSS IRQ FLAG (Bit 3) When CTCSS RX DECODE (Bit 4, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1".
This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).

CTCSS FAST IRQ FLAG (Bit 2) When CTCSS FAST TONE (Bit 6, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1".
This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).

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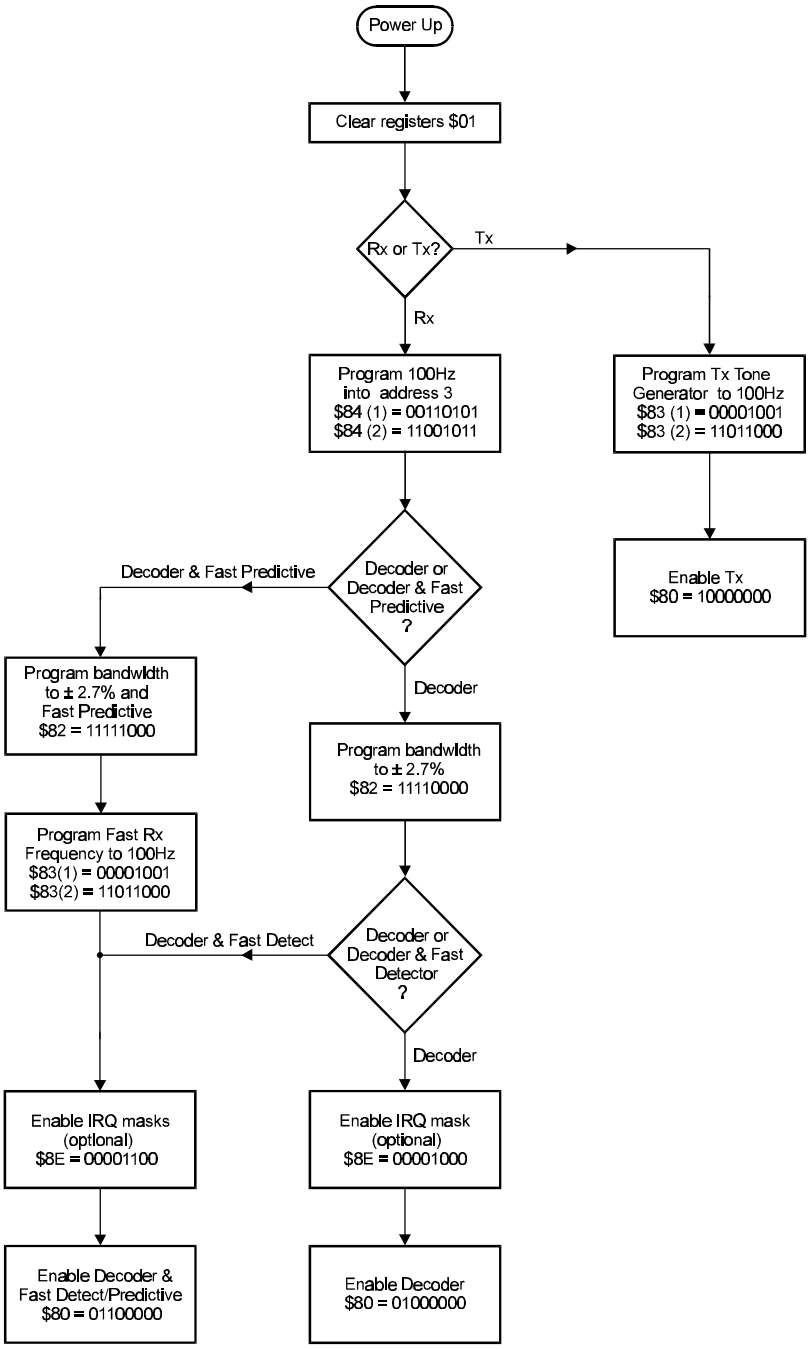
The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

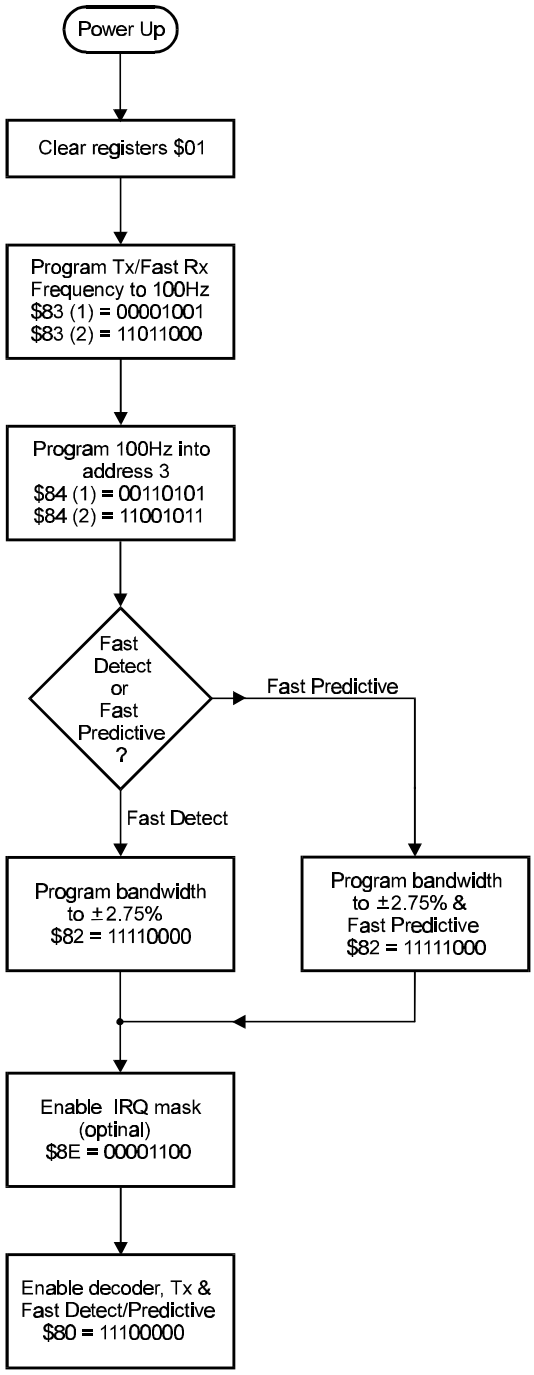
Note: $8X is the Hex address/command.



The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example:

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.



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1.6 Application Notes

1.6.1 General

The FX818 is intended for use in radio systems where sub-audio signalling is required for functions such as trunking, control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signalling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permits certainty and signal to noise performance to be traded when congestion or range limits the system performance.

1.6.2 Transmitter

The transmitter is enabled with Bit 7 in the "SUB-AUDIO CONTROL" register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX register ($83) using the formula below:

$$A = \frac{f_{XTAL}\,(Hz)}{16 \times f_{TONE}\,(Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT (Bits 7 and 5 in the "SUB-AUDIO CONTROL" register $80).

1.6.3 Receiver (Decode)

The CTCSS Receiver (Decoder) should first be set up according to the desired characteristics. This entails setting the CTCSS decoder bandwidth in the "SUB-AUDIO SET-UP" register ($82), also programming the centre frequencies of the desired tones in the "CTCSS RX PROGRAM" register ($84). (It can hold up to 15 different tones). Any tone can be in any location. During operation when the device is receiving, the tones are scanned in the sequence of their location, i.e. $0 first and $E last and once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The CTCSS IRQ MASK in the "IRQ MASK" register ($8E) should also be set as required.

The CTCSS DECODER ENABLE in the "SUB-AUDIO CONTROL" register ($80) should then be set to "1". Whilst in the Decode mode the FAST DETECT may be enabled (see below). (Bit 5 in the SUB-AUDIO CONTROL register $80).

When the receiver detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SUB-AUDIO STATUS register ($81) and if a tone is indicated by these bits then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

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1.6.4 Receiver (Fast/Predictive Detector)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimised for speed at the expense of frequency resolution.

It can operate in parallel to the Rx decoder. It is enabled using Bit 5 of the "SUB-AUDIO CONTROL" register ($80). It has an IRQ which may be unmasked with Bit 2 of the "IRQ MASK" register ($8E). The "FAST CTCSS MODE DETECT/PREDICTIVE" Bit 3 in the "SUB-AUDIO SET UP" register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the "CTCSS TX/FAST RX" register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG register ($8F), and the CTCSS FAST TONE Bit 6 in the SUB-AUDIO STATUS register ($81).

1.6.5 General Purpose Timer (GPT)

This may be used in conjunction with the Rx Decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value register "GENERAL PURPOSE TIMER" register ($8B) set in units of 1msec, an IRQ FLAG Bit 6 of the "IRQ FLAG" register ($8F) and an IRQ MASK Bit 6 "IRQ MASK" register ($8E).

1.6.6 Tx / Fast Rx Tone Table

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

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1.6.7 Rx Program Tone Table

The following table lists the commonly used CTCSS tones together with the values for programming the "CTCSS RX PROGRAM" register (Hex address $84).

N.B. The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

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1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D2 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D5 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

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Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz
Audio Level 0dB ref = 308mVrms at 1kHz
V_{DD} = 3.3V to 5.0V, Tamb = -40°C to +85°C.
Composite Signal = 308mVrms at 1kHz + 75mVrms Noise + 31mVrms Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
At V_{DD} = 3.3V						
I_{DD} (powersaved, V_{DD} = 5.0V)		1, 2	-	0.6	1.0	mA
I_{DD} (powersaved, V_{DD} = 3.3V)		1, 2	-	0.35	0.6	mA
I_{DD} (Tx/Rx Operating V_{DD} = 5.0V)		1, 2	-	3.5	6.0	mA
I_{DD} (Tx/Rx Operating V_{DD} = 3.3V)		1, 2	-	1.6	2.5	mA
"C-BUS" Interface						
Input Logic "1"			70%	-	-	V_{DD}
Input Logic "0"			-	-	30%	V_{DD}
Input Leakage Current (Logic "1" or "0")			-1.0	-	1.0	µA
Input Capacitance			-	-	7.5	pF
Output Logic "1" (I_{OH} = 120µA)			90%	-	-	V_{DD}
Output Logic "0" (I_{OL} = 360µA)			-	-	10%	V_{DD}
"Off" State Leakage Current (Vout = V_{DD})		6	-	-	10	µA
AC Parameters						
CTCSS Decoder						
Sensitivity	(Pure CTCSS Tone)	5	-	-26.0	-	dB
Response Time	(Composite Signal)		-	140	-	ms
De-Response Time	(Composite Signal)		-	145	-	ms
Frequency Range			60	-	253	Hz
CTCSS Detector - Fast Detect						
Sensitivity	(Pure CTCSS Tone)	5	-	-26.0	-	dB
Response Time	(Composite Signal)		-	56.0	-	ms
Frequency Range			60		253	Hz
CTCSS Detector - Fast Predictive						
Sensitivity	(Pure CTCSS Tone)	5	-	-26.0	-	dB
Response Time	(Composite Signal)	7	-	37.0	-	ms
Frequency Range			60	-	253	Hz
Decode Bandwidth			-	40	-	Hz
CTCSS Encoder						
Frequency Range			60	-	253	Hz
Tone Frequency Resolution			-	-	0.3	%
Tone Amplitude Tolerance		1	-1.0	0	+1.0	dB
Total Harmonic Distortion		9	-	2.0	-	%

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	Notes	Min.	Typ.	Max.	Units
Audio Band-Pass Filter					
Passband	8	300	-	3000	Hz
Passband Gain (at 1.0kHz)	8	-	0	-	dB
Passband Ripple (w.r.t. gain at 1.0kHz)	8	-2	-	+0.5	dB
Stopband Attenuation	8	33.0	-	-	dB
Residual Hum and Noise		-	-50.0	-	dBp
Alias Frequency		-	63	-	kHz
Output Impedances					
TX SUB-AUDIO OUT and (Enabled)		-	2.0	-	kΩ
RX AUDIO OUT (Disabled)		-	500	-	kΩ
Rx Amp and Summing Amp					
Open Loop Gain (I/P = 1mV at 100Hz)		-	70.0	-	dB
Unity Gain Bandwidth		-	5.0	-	MHz
Input Impedance (at 100Hz)		10	-	-	MΩ
Output Impedance (Open Loop)		-	6.0	-	kΩ
Transmitter Modulator Drives:					
Mod.1 Attenuator					
Attenuation (at 0dB)		-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		-1.0	-	1.0	dB
Output Impedance	3	-	600	-	Ω
Input Impedance (at 100Hz)		-	15.0	-	kΩ
Mod.2 Attenuator					
Attenuation (at 0dB)		-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		-0.6	-	0.6	dB
Output Impedance	3	-	600	-	Ω
General Purpose Timer					
Timing Period Range		1	-	242	ms
Count Interval		-	0.95	-	ms
Xtal/Clock Input					
Pulse Width ('High' or 'Low')	4	40.0	-	-	ns
Input Impedance (at 100Hz)		10.0	-	-	MΩ
Gain (I/P = 1mVrms at 100Hz)		20.0	-	-	dB

Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device pins by external circuitry.
3. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. IRQN pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD1 or MOD2 output.

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1.7.1 **Electrical Performance** (continued)

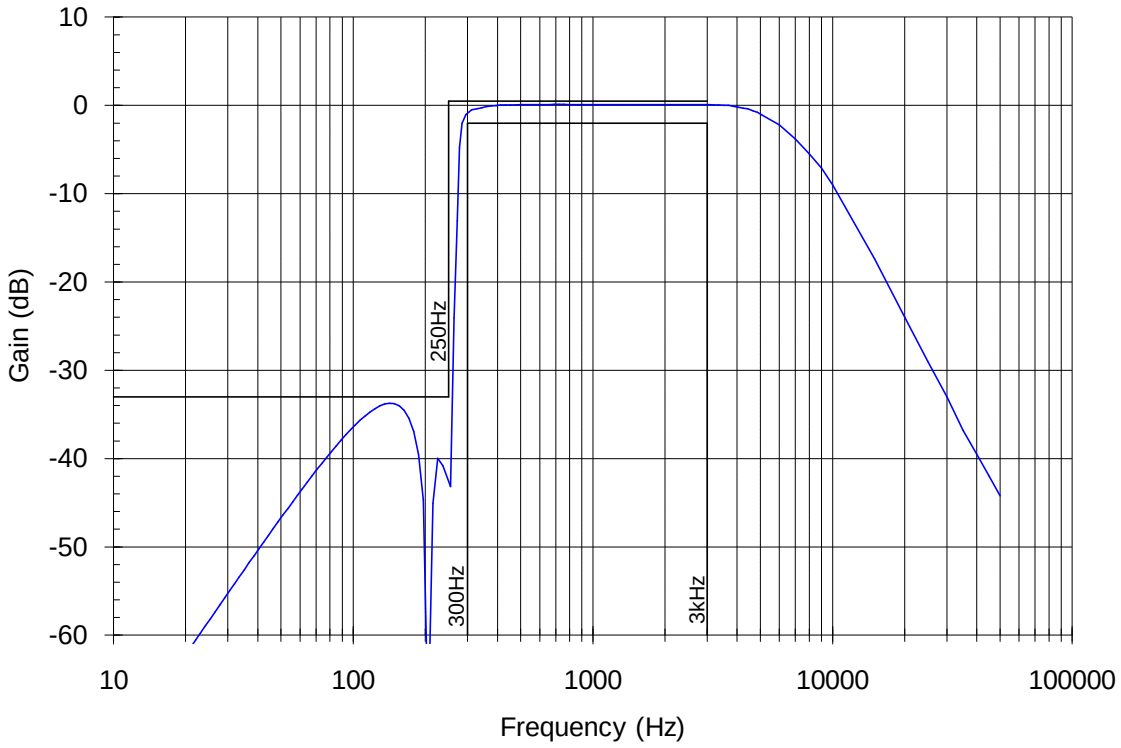

Figure 3 Audio Band-Pass Filter Frequency Response

1.7.1 Electrical Performance (continued)

Timing Diagrams

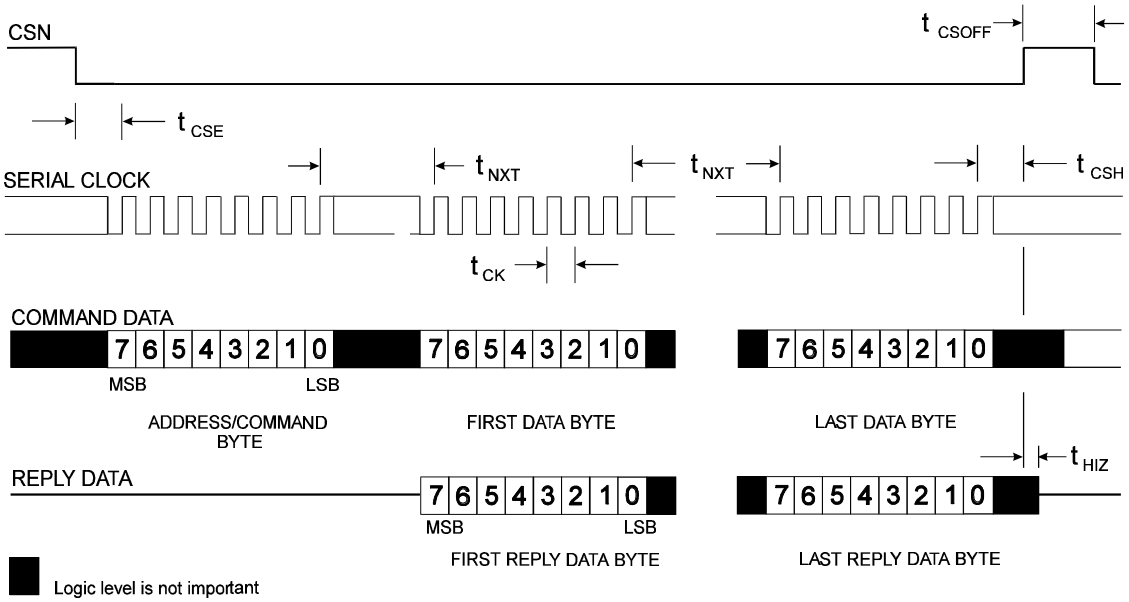

Figure 4 "C-BUS" Timing

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 3.3V to 5.0V, Tamb = -40°C to +85°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"		2.0		-	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0		-	µs
t_{HIZ}	"CS-High to Reply Output 3-state"		-		2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0		-	µs
t_{NXT}	"Inter-Byte" Time		4.0		-	µs
t_{CK}	"Clock-Cycle" time		2.0		-	µs

Notes:
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

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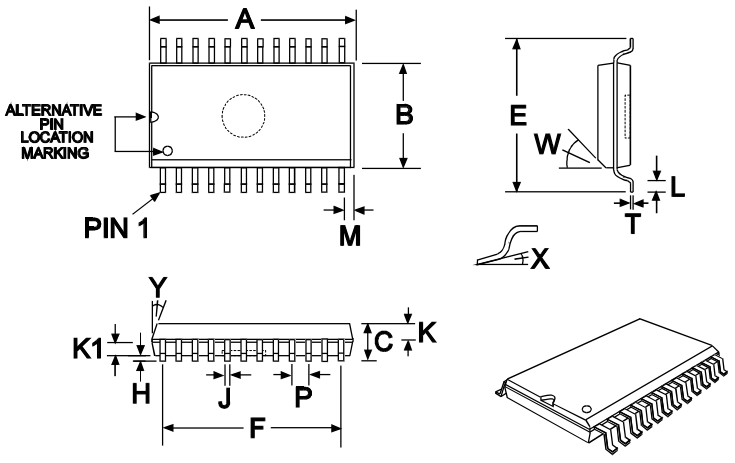
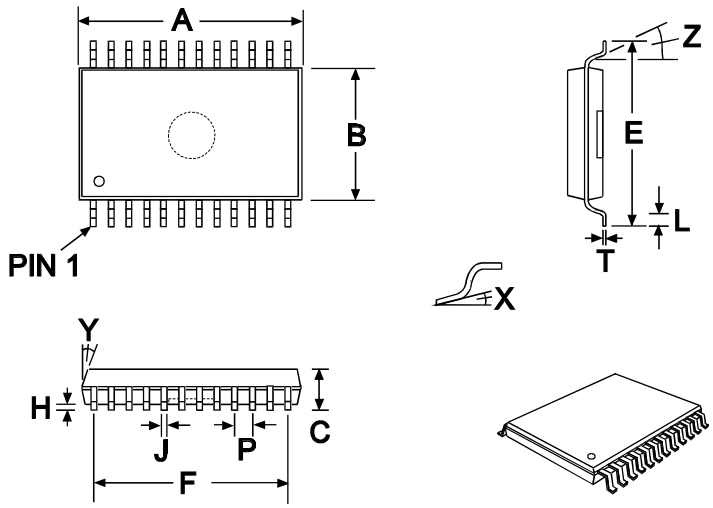
1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 5 Mechanical Outline: *Order as part no. FX818D2*



DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 6 Mechanical Outline: *Order as part no. FX818D5*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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