STANDARD
MICROSYSTEMS
CORPORATION

DBC98C51

SMBus Device Bay Controller

FEATURES

- 5 or 3.3 Volt Operation
- Supports 2 Device Bays
- ACPI Compliant
- Pin Selectable SMBus Address Allows up to Three Additional Controllers Providing up to 8 Device Bays in System
- Interrupt Notification of Device Bay Status Change Events
- 1/2 Hz (+/- 20%) Internal LED Flasher
- Provides Direct Drive Outputs (20mA) for Bipolar, Common Cathode Dual LEDs or Single LEDs
- Pin Selectable Lock Control Mode
- 14.318 MHz Clock Input
- 100 kHz SMBus Serial Clock
- 28 Pin SOIC Package

GENERAL DESCRIPTION

The DBC98C51 Device Bay Controller is intended to provide Device Bay GPIO support with host based USB and 1394. The DBC98C51 is a slave SMBus compatible device that uses ACPI methods to enable and control 1394 and USB devices in the newly proposed Device Bay physical form factors.

Placing the Device Bay status and control GPIOs on an SMBus device provides the greatest placement flexibility to the system designer for non-Remote Device Bay Controller solutions. Additionally, by keeping registers out of ISA, PCI, or LPC direct ACPI register space, conflicts are minimized and firmware methods remain transportable.

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80 Arkay Drive
Hauppauge, NY 11788
(516) 435-6000
FAX (516) 273-3123

PIN CONFIGURATION

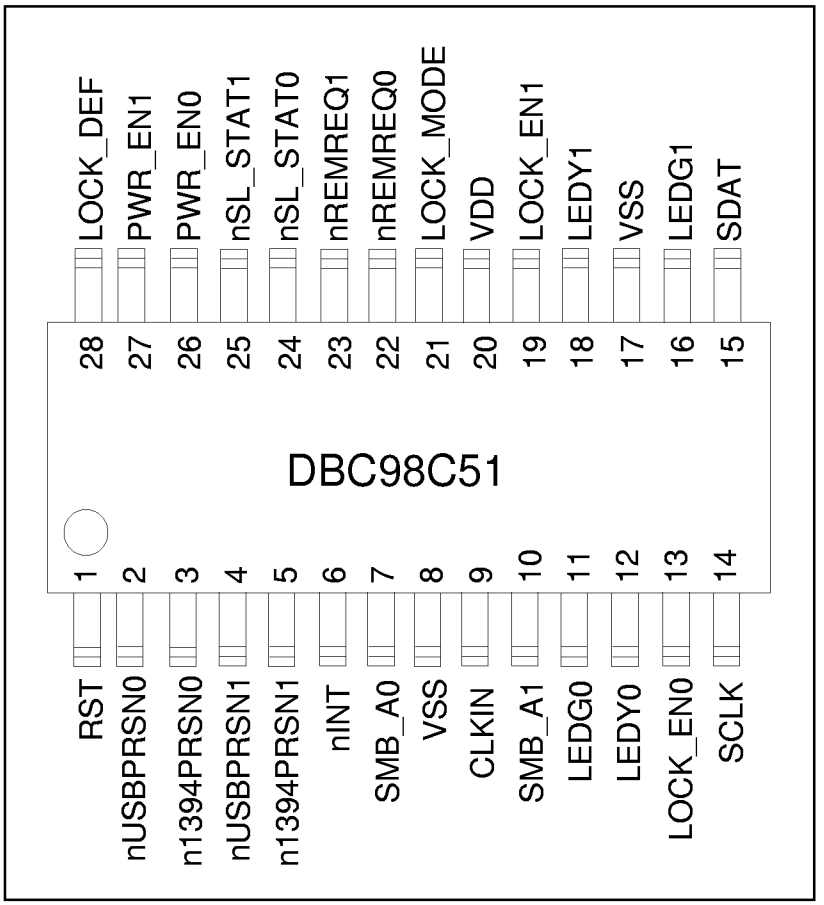


FIGURE 1 – DBC98C51 SOIC PIN CONFIGURATION

PIN DESCRIPTIONS

Table 1 - DESCRIPTION OF PIN FUNCTIONS

SOIC PIN #	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
DEVICE BAY INTERFACE				
5,3	1394 Device Presence Input	n1394PRSN [1:0]	I	A low (0) level on this pin indicates that the device bay [0 or 1] contains a 1394 device. This input is de-bounced since its assertion will cause an interrupt to be generated. An external pull-up resistor is required on this pin. This pin is de-bounced internally for 100ms before passing its state to the internal circuitry.
4,2	USB Device Presence Input	nUSBPRSN[1:0]	I	A low (0) level on this pin indicates that the device bay [0 or 1] contains a USB device. This input is de-bounced since its assertion will cause an interrupt to be generated. An external pull-up resistor is required on this pin. This pin is de-bounced internally for 100ms before passing its state to the internal circuitry.
16,11	Green LED Output	LEDG [1:0]	O24	This active high output indicates that its associated device bay is enabled (steady on) or its enable is pending (flashing at 1/2Hz rate). This output will not be active if the bay's associated LEDY output is active. A bipolar dual LED may be attached between this output and the LEDY output.
18,12	Yellow LED Output	LEDY [1:0]	O24	This active high output indicates that its associated device bay has a removal request pending (flashing at 1/2Hz rate). This output will not be active if the bay's associated LEDG output is active. A bipolar dual LED may be attached between this output and the LEDG output.

SOIC PIN #	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
19,13	Software Controlled Interlock Enable Output	LOCK_EN [1:0]	OD12	This signal operates in two modes (selected by the LOCK_MODE input pin). When LOCK_MODE is low (0) this output will reflect the state of the LOCK_CTL bit in the BCERx register. In this case when the output is active (float) it will cause an external electromechanical device to activate thereby physically locking the device into the bay; the external electromechanical device is disengaged when this output is negated (0). When LOCK_MODE is high (1), this output will be pulsed LOW (0) for a programmable period of time when the LOCK_CTL bit in the BCERx register transitions from 1 to 0. During the pulse period an external electromechanical device will be activated in order to physically unlock the device from the bay. The pulse duration is programmable to either 120msec, 500msec, 1sec or 2sec in via the Lock Enable Timing Register.
27,26	V_{ID} Power Enable Output	PWR_EN [1:0]	OD12	This active high output enables an external power control device (e.g. FET) to provide enumeration power to the device. When negated, the enumeration power is disabled. This output reflects the state of the PWR_CTL bit in the BCERx.
23,22	Device Removal Request Input	nREMREQ [1:0]	I	A low (0) level on this pin indicates that a request to remove the device in the associated device bay [0 or 1] has been made. This input is de-bounced since its assertion will cause an interrupt to be generated. An external pull-up resistor is required on this pin.
25,24	Security Lock Status Input	nSL_STAT [1:0]	I	A low (0) level on this pin indicates that a physical security lock is present and active on the associated device bay [0 or 1]. A high level (1) indicates that the physical security is either not present or is disengaged. An external pull-up resistor is required on this pin.
SMBus/HOST INTERFACE				
14	Serial Clock Input	SCLK	IOD12	This is the SMBus clock input. Maximum operation is 100kHz.
15	Serial Data Input/Output	SDAT	IOD12	This is the SMBus data input/output. Maximum operation is 100kHz.

SOIC PIN #	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
6	Host Interrupt Output	nINT	O12	This active low output signals a status change or removal request in one of the device bays (see the BCERx register). It is normally connected to one of the Interrupt inputs of the host controller. The interrupt is cleared by writing a "1" to the appropriate BSTRx register bit.
CONFIGURATION OPTIONS				
10,7	Address Select	SMB_A[1:0]	I	These inputs form the last LSB of the SMBus slave address of the controller (eg. 1001_0xx). This allows up to 4 controllers to be used to provide up to 8 device bays in the system.
28	Lock Default State	LOCK_DEF	I	This pin determines the default value of the LOCK CTL bit when the LOCK_MODE pin is low (0). On reset (POR or RST high) the LOCK_DEF pin is sampled and qualified with the value of the LOCK_MODE pin. If LOCK_MODE is high (1), the LOCK_DEF pin has no effect, in which case the LOCK_CTL bit defaults to 0. If LOCK_MODE is low, and the LOCK_DEF pin is low, then the LOCK_CTL bit defaults to 0. If LOCK_MODE is low and the LOCK_DEF pin is high, then the LOCK_CTL bit defaults to 1.
21	Lock Mode	LOCK_MODE	I	A low (0) level on this pin indicates that the LOCK_EN output tracks the state of the LOCK_CTL bit in the BCERx. A high (1) level indicates that the LOCK_EN output is pulsed when the LOCK_CTL bit transitions from 1 to 0.
POWER AND TEST INTERFACE				
1	Reset Input	RST	I	An active high (1) on this pin resets the controllers internal registers to their default states. Reset Input is deglitched by CLKIN; that is, an active high on this pin for 2 pulses of CLKIN will reset the controller's internal registers to their default states.
9	Clock Input	CLKIN	I	A 14.318 MHz clock signal should be applied to this pin.
20	Power	VDD	-	5 or 3.3 Volts should be applied to this pin.
17	Ground	VSS	-	Ground reference

Buffer Type Summary

Table 2 below describes the buffer types shown in Table 1. All values are specified at VDD = +5.0v, ±10%

Table 2 - BUFFER TYPE SUMMARY

BUFFER TYPE	DESCRIPTION
I	Input; TTL level compatible.
O12	Output. 12ma sink; 6ma source.
IO12	Input/Output. 12mA sink; 6mA source.
OD12	Open Drain Output. 12ma sink.
IOD12	Input/Open Drain Output. 12mA sink.
O24	Output. 24ma source/sink.

Output Drivers

Active output drivers in the DBC98C51 will always achieve the minimum specified DC Electrical Characteristics as shown in Table 8.

Operating Voltage

The DBC98C51 operates at either 3.3 Volts or 5 Volts. At 3.3 Volts, the part is 5 Volt tolerant; that is, the input voltage is 5.5V max, and the I/O pads are backdrive protected.

BLOCK DIAGRAM

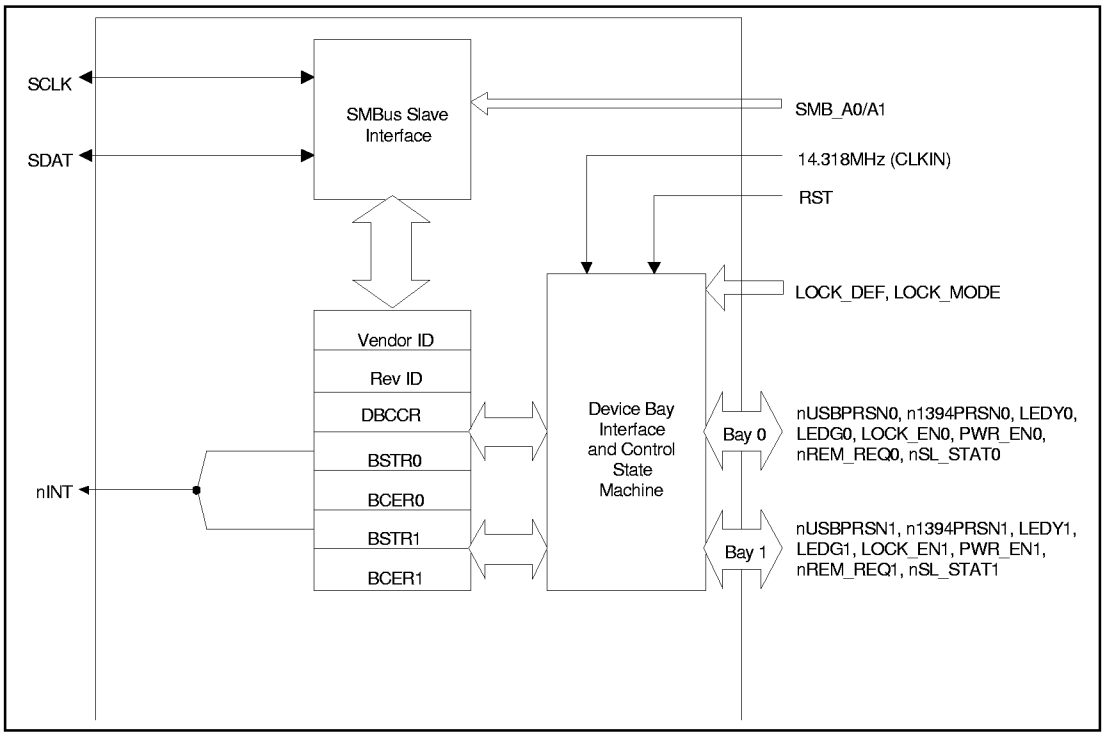


FIGURE 2 – DBC98C51 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

SMBus Slave Interface

The DBC98C51 SMBus implementation is a subset of the SMBus interface to the host. The DBC98C51 is a *slave-only* SMBus device. SMBus (System Management Bus) is a two wire interface protocol that uses the Philips I^2C bus physical layer as its backbone. The implementation in the DBC98C51 is a subset of SMBus since it only supports two commands.

The Read Byte and Write Byte commands are the only valid SMBus command protocols for the DBC98C51. The part responds to other command protocols as described in the Invalid Command Protocol Section. Reference the System Management Bus Specification, Rev 1.0.

The SMBus interface is used to read and write the registers in the Device Bay Controller. The only valid registers for a read or write command are the Device Bay registers shown in the Register Set Section.

Commands

Typical Write Byte and Read Byte commands are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the DBC98C51 driving data on the SDAT line; otherwise host data is on the SDAT line.

The slave address is a unique address for the DBC98C51 that identifies it on SMBus. The register address field is the Device Bay register address to be accessed. The register data field is the data that the host is attempting to write to the Device Bay register or the contents of the Device Bay register that the host is attempting to read.

Data bytes are transferred MSB first.

Write Byte

The Write Byte command is used to write data to the Device Bay registers. The data will only be written if the command protocol shown in Table 3 is performed correctly. Only one byte is transferred at time for a Write Byte command.

Table 3 - SMBus Write Byte Command Protocol

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Reg. Data	Ack	Stop
Bits:	1	7	1	1	8	1	8	1	1

Read Byte

The Read Byte command is used to read data to the Device Bay registers. The data will only be read if the command protocol shown in Table 4 is performed correctly. Only one byte is transferred at time for a Read Byte command.

Table 4 - SMBus Read Byte Command Protocol

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1	7	1	1	8	1	1

Slave Address

The slave address is the unique address for the DBC98C51 that identifies the device on SMBus.

The DBC98C51's slave address is determined by the levels on the SMB_A0 and SMB_A1 pins. The level on these pins forms the LSB of the 7-bit address 1001_0xx. These pins may be used to cascade multiple (up to 4) controllers in a given system.

The upper 5 bits of the DBC98C51's slave address are hardwired in the DBC98C51.

General Call Address Response

The DBC98C51 will not respond to a general call address of 0000_000.

Invalid Command Protocol Response Behavior

The Device Bay Registers that are accessed with an invalid command protocol will not be updated. A register will only be updated following a valid command protocol. The only valid commands are the read byte and write byte commands described above. Note: The 16-bit vendor ID register is accessed through two single byte transfers. The first byte is accessed at address 00 and the second at address 01.

The only valid slave address is determined by the levels on the SMB_A0 and SMB_A1 pins as the LSB of the address 1001_0xx.

The only valid registers for a read or write command are the Device Bay registers shown in the Register Set Section. Reserved registers are not considered valid registers.

The following subsections describe the response by the DBC98C51 to invalid attempts to communicate with it over SMBus.

Invalid Slave Address

If the host sends an invalid slave address, the SMB Slave Interface in the DBC98C51 will not respond and the SMBus Slave Interface will return to the idle state.

Invalid Register Address

If the SMBus Slave Interface receives an invalid Register Address after acknowledging a valid slave address and a write field bit, it will follow through with the command protocol (if the command protocol from the master is correct). It will latch the register address and ACK. In the case of a read byte command, it will ACK the second START, slave address and read field, but return zero data. In the case of a write byte command, it will ACK the register data but it will have no effect. If the command protocol from the master is not correct, it will respond as described below.

Slave Receives Multiple Byte Read Command Protocol

This condition pertains to an attempt by the host to transfer two or more bytes in a read command. If the SMBus Slave Interface receives an ACK after the first register data byte it will stop responding and return to idle. Note: This pertains to an attempted autoincrement read as in I^2C. The DBC98C51 does not support the SMBus block read command.

Slave Receives Multiple Byte Write Command Protocol

This condition pertains to an attempt by the host to transfer two or more bytes in a write command. If the SMBus Slave Interface receives a second data byte following the register data byte ACK, it will stop responding (NACK) and return to the idle state. Note: This pertains to an attempted autoincrement write as in I^2C. The DBC98C51 does not support the SMBus block write command and if a byte count is given in the data byte field, it will be interpreted as data.

Improper Field Within Command Protocol

If the SMBus slave interface receives an improper field, it will stop responding and return to the idle state. Several cases follow. Note that by not responding, a NACK will be produced in the ACK/NACK field that follows the improper field.

Stop Flag Received During Command/Data Expectation

If the SMBus Slave Interface receives a STOP where it is not expected, it will not respond and return to idle.

Start Sequence Received in Middle of Transaction

If the SMBus Slave Interface receives a correct start sequence (start bit, valid slave address and write bit) in the middle of a transaction (not a read byte transaction) it will stop responding and return to idle.

Read Field Received Following the First Slave Address

If the SMBus Slave Interface receives a read bit following the first slave address (excluding the bit field following the second slave address of a read command), it will not respond and then return to idle.

Write Field Received Following the Second Slave Address of a Read Command

If the SMBus Slave Interface receives a write bit following the second slave address of a read command, it will not respond and then return to idle.

Slave Device Time-Out

The device will always time-out when SCLK is held low longer than $T_{TIME\text{-}OUT}$ Max = 35ms. The SMBus Slave Interface resets and returns to idle if SCLK is held low for longer than $T_{TIME\text{-}OUT}$ Max.

Stretching the SCLK Signal

The DBC98C51 supports stretching of the SCLK low time between byte transfers (byte+ACK). The DBC98C51 will not hold the SCLK low longer than ten CLKIN pulses.

SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing Specification in the System Management Bus Specification, Rev 1.0.

Bus Reset Sequence

The SMBus Slave Interface will reset and return to the idle state upon a START field followed immediately by a STOP field.

Interrupt to Host

The DBC98C51 notifies the host system when specific hardware events have occurred. This is done using an interrupt signal, nINT, to the system's ACPI interrupt logic.

REGISTER SET

The DBC98C51 contains three general configuration/status registers and 2 additional registers for each of the two device bays it supports. The registers all reside in the DBC98C51's internal SMBus address space.

Table 5 - Device Bay Registers

REGISTER	ADDRESS	WIDTH[2]	DESCRIPTION
GENERAL REGISTERS			
Vendor ID	00h	16 bits[3]	DBC98C51 Vendor ID
Revision ID	04h	8 bits	DBC98C51 Revision ID
DBCCR	0Ch	8 bits	Device Bay Controller Capabilities Register
DEVICE BAY 0 REGISTERS			
BSTR0	10h	8 bits	Bay 0 Status Register
BCER0	14h	8 bits	Bay 0 Control and Enable Register
DEVICE BAY 1 REGISTERS			
BSTR1 [1]	18h	8 bits	Bay 1 Status Register
BCER1 [1]	1Ch	8 bits	Bay 1 Control and Enable Register
RESERVED			
Reserved	20h	8 bits	RESERVED
•	•	•	•
•	•	•	•
Reserved	39h	8 bits	RESERVED
LETR	40h	8 bits	Lock Enable Timing Register
Reserved	41h	8 bits	RESERVED
•	•	•	•
•	•	•	•
Reserved	FEh	8 bits	RESERVED
SMSC Test Mode	FFh	8 bits	Test Mode Register

Note 1: If only one bay is implemented (BAYCNT[3:0] = xx01b in the DBCCR) then read accesses to these registers return all zeroes and writes have no effect.

Note 2: All registers are in little endian form; that is, bit 0 is the least significant bit.

Note 3: The 16 bit vendor ID register is accessed through two single byte transfers. The least significant byte is accessed at address 00h and the most significant byte at address 01h.

Vendor ID Register

Address: 00h
Attribute: Read-only
Size: 16 bits
Default: 0x1055

The contents of this register identify the manufacturer of the device. The value used is the same as the one allocated by the PCI SIG. The value of this register is 0x1055.

Revision ID Register

Address: 04h
Attribute: Read-only
Size: 8 bits
Default: Revision Number

The contents of this register specify the revision number of the device.

Device Bay Controller Capabilities Register (DBCCR)

Address: 0Ch
Attribute: Read Only after first write to this register following reset (POR or RST high)
Size: 8 bits
Default Value: 0000_0000b

BIT	NAME	ACCESS	DESCRIPTION
7-5	Reserved	R/O	Reserved for future use. Read as 000b.
4	SECLOCK	R/O Note 1	Security Lock Support. • If set (1), at least one bay controlled by this DBC98C51 contains a physical security lock (such as a key lock) that is not necessarily controllable by software. In addition, the current state of the security mechanism (that is, engaged or disengaged) is available in the Bay x Status Register (BSTRx). • If cleared (0), then there are no physical security locks in this Device Bay subsystem.
3,2	BAYCNT[3:2]	R/O	Read only. Returns 00b.
1-0	BAYCNT[1:0]	R/O Note 1	Represents the number of bays implemented with this DBC98C51. It does not indicate how many bays are populated. The value in this field is a binary encoding of the number of bays (for example, 10b indicates that two bays are implemented).

Note 1: These bits may be written once after reset (POR or RST high). They then become read only. These bits MUST be written prior to loading the operating system, even if the default values are to be used, to prevent unauthorized or accidental modifications.

Bay *x* Status Register (BSTR*x*) (One per Bay)

Address: 10h (BSTR0), 18h (BSTR1)
Attribute: Read-Only, Bits 2,3 Read/Write Clear
Size: 8 bits
Default Value: x000_00xxb

BIT	NAME	ACCESS	DESCRIPTION
7	SL_STS	R/O	Indicates the state of the optional bay-mounted physical security lock. • When read as a "1" the physical security lock is engaged for this bay. • When read as a "0" the physical security lock is disengaged for this bay. The value of this bit represents the logical inverse of the state of the nSL_STAT pin.
6-4	BAY_ST[2:0]	R/O	This field represents the actual state of the bay. The states are decoded as follows: **BAY_ST[2:0]** **Meaning** 000 Bay Empty 001 Device Inserted 010 Device Enabled 011 Removal Requested: 100 Device Removal Allowed 101 Reserved 110 Reserved 111 Reserved The value read from this register does NOT necessarily represent the last state written to the Bay *x* Control and Enable Register. The DBC98C51's bay state machine has the ability to override values previously written to the BCER*x* register when an appropriate hardware event (e.g. user removes the device) occurs. Only hardware events can cause transitions from any state to the "Bay Empty" state. Refer to the state diagram that follows. Note that following reset (POR or RST high), if the USBPRSN_STS or 1394PRSN_STS (bits 0 or 1 of the BSTRx register) are a "1", the DEVSTSCHG bit will be set AND if the DEVSTSGHG_EN bit is set, then the controller will transition to the "Device Inserted" state

BIT	NAME	ACCESS	DESCRIPTION
3	REMREQ_STS	R/WC	Indicates the removal request button for this bay has been pressed. • This is a "sticky" bit which is set to "1" when the button is pressed (a high to low transition on the nREMREQ*x* signal) AND a device is present in the bay (see bits 1 & 0 of this register). The low to high transition on the nREMREQ signal is ignored. • This bit along with its corresponding enable bit in the Bay *x* Control and Enable Register can cause the nINT pin to be active. • This bit can only be cleared by writing a "1" to it. If the removal request feature is not used in the system, the corresponding nREMREQx should be tied high externally.
2	DEVSTSCHG	R/WC	Indicates device status has changed in this bay. • This is a "sticky" bit which is set to "1" when the state of either of 1394PRSN_STS or USBPRSN_STS bits in this register changes state. • A high on this bit along with the corresponding enable bit in the Bay *x* Control and Enable Register can cause the nINT pin to be active. • After power on reset this bit can only be cleared by writing a "1" to it. If a device is present upon reset (POR or RST high) this bit will be set.
1	1394PRSN_STS	R/O	Indicates 1394 device presence for this bay. If a 1394 device is present then the bit will be "1"; if no 1394 device is present then the bit will be "0." The value of this bit represents the logical inverse of the state of the 1394 presence (n1394PRSN*x*) pin.
0	USBPRSN_STS	R/O	Indicates USB device presence for this bay. If a USB device is present then the bit will be "1"; if no USB device is present then the bit will be "0." The value of this bit represents the logical inverse of the state of the USB presence (nUSBPRSN*x*) pin.

Bay *x* Control and Enable Register (BCER*x*) (One per Bay)

Address: 14h (BCER0), 1Ch (BCER1)
Attribute: Read/Write
Size: 8 bits
Default Value: 0000_0000b (Note 0)

BIT	NAME	ACCESS	DESCRIPTION
7	LOCK_CTL	R/W	Engages/disengages the software controlled external interlock mechanism for this bay. The LOCK_EN pins are controlled by this bit in one of two modes as selected by the LOCK_MODE pin. LOCK_MODE=0: • When set to "1" the LOCK_EN pin floats and the lock mechanism will be engaged (i.e. the device is physically locked into the bay). • When cleared to "0" the LOCK_EN pin is low and the software interlock mechanism will be disengaged (i.e. the device can be physically removed). LOCK_MODE=1: • The LOCK_EN pin is pulsed low (0) when this bit transitions from 1 to 0. The pulse duration is programmable to either 120msec, 500msec, 1sec or 2sec in via the Lock Enable Timing Register. See the LOCK_ENx pins for additional information on the operation of this bit.

BIT	NAME	ACCESS	DESCRIPTION
6-4	BAY_STREQ[2:0]	R/W	This field represents the state of this bay as **requested** by the DBC98C51 driver, but does NOT necessarily represent the actual state of the bay. The states are decoded as follows: **BAY_STREQ[2:0] Meaning** 000 No change to bay state requested 001 Request to change bay state to Device Inserted 010 Request to change bay state to Device Enabled 011 Request to change bay state to Removal Requested 100 Request to change bay state to Device Removal Allowed 101 Reserved. No effect to bay state 110 Reserved. No effect to bay state 111 Reserved. No effect to bay state If 000b is written then no change of state is requested AND any previous non-zero value of these bits is retained. This allows software to modify other bits in this register without inadvertently causing a bay state change. Any legal, non-zero value written to this field indicates a requested change of bay state. A bay state transition will occur at the time of the write to this field with a device present; there is no queueing of state transition requests. If no device is present at the time a write of a non-zero value occurs then no state transition will ever take effect for that write event; however, this field is updated with that non-zero value. The DBC98C51 resets this field to 000b when the device is removed from the bay (i.e., n1394PRSNx AND nUSBPRSNx pins are both high).
3	REMREQ_EN	R/W	Enables/disables the DBC98C51 to generate an interrupt via the nINT pin due to a removal request. This bit is ANDed with the REMREQ_STS bit in the Bay *x* Status Register to create an interrupt. • When set to "1" the interrupt is enabled. • When cleared to "0" no interrupts will be generated for the corresponding removal request.
2	DEVSTSCHG_EN	R/W	Enables/disables the DBC98C51 to generate an interrupt via the nINT pin due to a device status change event. This bit is ANDed with the DEVSTSCHG bit in the Bay *x* Status Register to create an interrupt. • When set to "1" the interrupt is enabled. • When cleared to "0" no interrupts will be generated for the corresponding device status change event.

BIT	NAME	ACCESS	DESCRIPTION
1	REMEVTWAK_EN	R/W	Enables/disables the interrupt generated due to a device removal event (n1394PRSNx OR nUSBPRSNx pin goes from low to high). This bit gates the device removal event in the DEVSTSCHGx logic (BSTR*x*, bit 2). This bit conditionally allows device removal as an interrupt event. When the bay is not in state 100b (Device Removal Allowed), a device removal event will always cause DEVSTSCHGx to be set. • When set to "1," a device removal event will be cause DEVSTSCHGx to be set when the bay is in state 100b. A corresponding interrupt will be generated provided DEVSTSCHG_ENx (see bit 2) is set. When cleared to "0," device removal events when the bay is in state 100b will not cause DEVSTSCHG to be set.
0	PWR_CTL	R/W	Enables/disables the power for this bay via the PWR_ENx pin. • When set to "1" V_{id} power is enabled, and the PWR_ENx pin floats. This bit can only be written to a "1" if either of the BSTR*x*, bits 1 & 0 are a "1" AND BCERx bit 7 is a "1". • When cleared to "0" V_{id} power is disabled and the PWR_ENx is low. If BCERx bit 7 is a "0", then this bit is cleared. Furthermore, this bit must be cleared automatically by the DBC whenever a device is removed.

Note: The LOCK_DEF pin determines the default value of the LOCK_CTL bit when the LOCK_MODE pin is low (0). On reset (POR or RST high) the LOCK_DEF pin is sampled and qualified with the value of the LOCK_MODE pin. If LOCK_MODE is high (1), the LOCK_DEF pin has no effect, in which case the LOCK_CTL bit defaults to 0. If LOCK_MODE is low, and the LOCK_DEF pin is low, then the LOCK_CTL bit defaults to 0. If LOCK_MODE is low and the LOCK_DEF pin is high, then the LOCK_CTL bit defaults to 1.

Test Mode Register

Address: FFh
Attribute: Read/Write
Size: 8 bits
Default: 0x00

This register is an SMSC test mode register. It is used to enable SMSC test modes only and is not to be accessed under normal operation.

Lock Enable Timing Register
Address: 40h
Attribute: Read/Write
Size: 8 bits
Default: 0x00h

This register is used to select the pulse width of the lock enable pin when lock mode is '1'. This register is defined below.

BIT	NAME	ACCESS	DESCRIPTION
7-2	Reserved	R/O	Reserved for future use. Read as 000000b.
1-0	Pulse Width	R/W	The pulse width of LOCK_ENx when LOCK_MODE=1. The value of the pulse width is programmable one of the following values: 120msec, 500msec, 1sec or 2sec. Bits[1:0]: the value of these bits correspond to the pulse width of LOCK_ENx as follows: 11 = 2sec min to 2.02sec max 10 = 1sec min to 1.02sec max 01 = 500msec min to 520msec max 00 = 120msec min to 140msec max

BAY STATE MACHINE

Status Indicators

This DBC98C51 supports a bay-mounted LEDs that provide user-feedback during the various bay events.

LED STATE	LED COLOR	MEANING(S)
Dark	N/A	1. No device present 2. Safe to remove device 3. Device cannot be configured; O.K. to remove
1/2 Hz Flashing	Green	Insertion event acknowledged by DBC98C51 or OS-directed insertion event.
1/2 Hz Flashing	Yellow	Removal request event acknowledged by DBC98C51 or OS-directed removal request.
On	Green	Device is enabled.

Bay State Transitions

- The state of each bay can change due to hardware events (for example, device insertion) or software actions (for example, enabling the device). The following state diagrams and tables describe the bay states and transitions. Although the diagrams and tables are divided into "hardware" and "software" for the sake of clarity, in reality there is only one state machine per bay.

The behavior of the bay state machine due to hardware events is depicted in the following diagram. In the diagram:

- PRSN=0 indicates that no device is present in the bay (neither USBPRSN_STS nor 1394PRSN_STS in BSTRx are set). The state transitions to the Bay Empty state are independent of the state of DEVSTSCHG_EN.
- PRSN=1 indicates that a device is present in the bay (either USBPRSN_STS and/or 1394PRSN_STS are set). The transition from the Bay Empty state to the Device Inserted state can only be made if DEVSTSCHG_EN in the BCER*x* is set.
- It is assumed that a hardware removal request button is present. If no button is present, then the transitions in and out of the "Removal Requested" state would never be made by hardware events. REMREQ=0 indicates that either REMREQ_STS in the BSTR*x* is not set or REMREQ_EN in the BCER*x* is not set, while REMREQ=1 indicates that REMREQ_STS is set and REMREQ_EN is set.
- The two arcs labeled "PRSN = 0 *" are specified as hardware fail-safe transitions. In the event that the user forcibly overrides the software controlled interlock mechanism, the DBC will return the bay state machine to the correct state. These transitions are independent of the state of DEVSTSCHG_EN.

Note that some states are only accessible through a software transition.

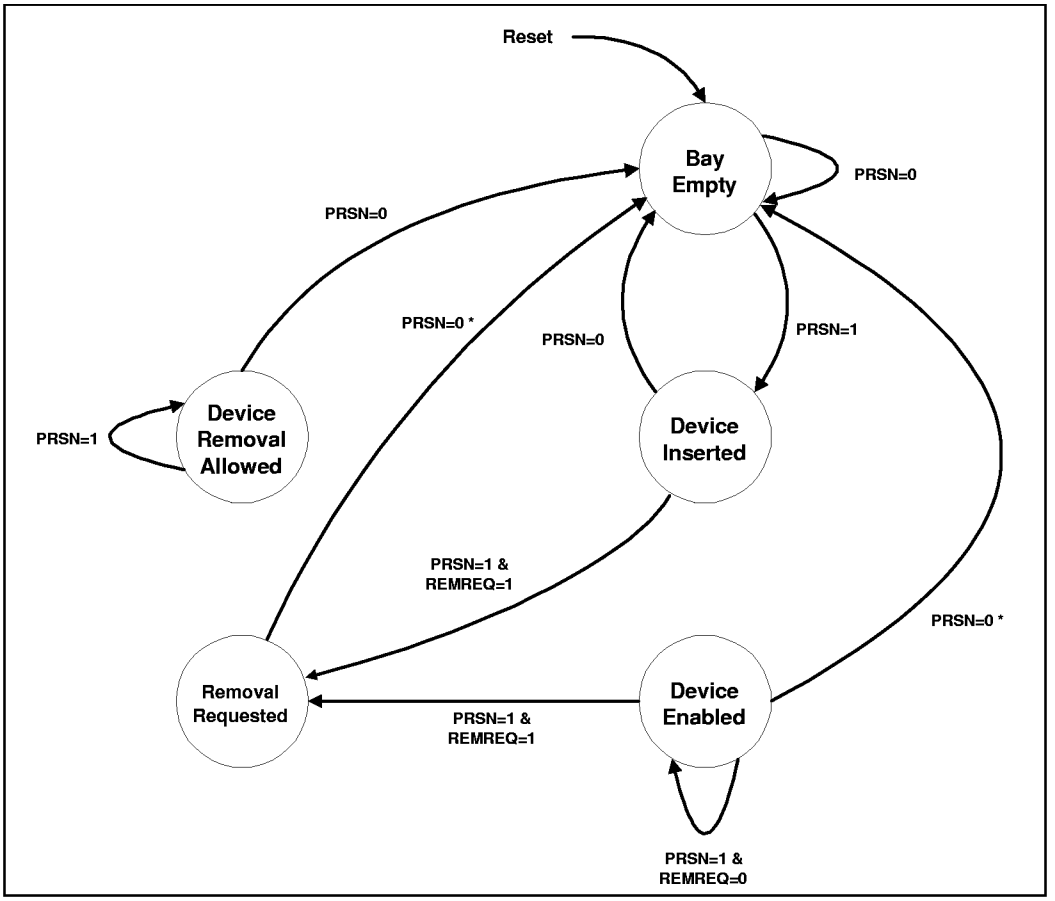


FIGURE 3 - BAY STATE DIAGRAM / HARDWARE TRANSITIONS

These transitions are described in more detail in the following table.

Table 6 - Hardware Event Bay State Transition

CURRENT STATE	NEXT STATE	HARDWARE EVENT	CONDITIONS	NOTES
- - -	Bay Empty (no device present)	Power on reset		Establish initial state.
- - -	Bay Empty (device present)	Power on reset		A device occupying a bay at power-on time will cause DEVSTSCHG to be set. Since DEVSTSCHG_EN defaults to "0" no bay state transition will result.
Bay Empty	Device Inserted	Device present on power on reset OR device inserted into the bay with DEVSTSCHG _EN cleared (0).	Either or both presence bits in the BSTRx are set (1) AND DEVSTSCHG_EN in the BCERx transitions from 0→1.	A device occupying a bay at power-on time will cause DEVSTSCHG to be set. DEVSTSCHG_EN defaults to "0"; writing DEVSTSCHG_EN to "1" will then cause the transition to the Device Inserted state. Also, if either or both presence bits transition from 0 → 1 with DEVSTSCHG_EN=0, then writing DEVSTSCHG_EN to "1" will cause the transition to the Device Inserted state.
Bay Empty	Device Inserted	Device inserted into the bay.	Either or both presence bits in the BSTRx transition from 0 → 1 AND DEVSTSCHG_EN in the BCERx is set.	
Device Inserted	Bay Empty	Device removed from the bay.	Presence bit(s) have transitioned from 1 → 0 independent of the state of DEVSTSCHG_EN.	Unexpected user behavior. The device was removed prior to being properly enabled by the OS. In this case the software controlled interlock mechanism may have been overridden.
Device Inserted	Removal Requested	User pressed the hardware removal request button, if present.	REMREQ_STS is set and REMREQ_EN is set.	User requested device removal before the device was enabled by the OS.

CURRENT STATE	NEXT STATE	HARDWARE EVENT	CONDITIONS	NOTES
Device Enabled	Bay Empty	Device was removed from the bay.	Presence bit(s) have transitioned from 1 → 0 independent of the state of DEVSTSCHG_EN.	Unexpected user behavior. The device was removed from the bay without going through the proper removal request sequence. In this case the software controlled interlock must have been overridden.
Device Enabled	Removal Requested	User pressed the hardware removal request button, if present.	REMREQ_STS is set and REMREQ_EN is set.	User requested device removal through the hardware removal request button.
Removal Requested	Bay Empty	Device removed from the bay.	Presence bit(s) have transitioned from 1 → 0 independent of the state of DEVSTSCHG_EN.	Unexpected user behavior. The device was removed prior to completion of the proper removal request sequence. In this case the software controlled interlock mechanism may have been overridden.
Device Removal Allowed	Bay Empty	Device was removed from the bay.	Presence bit(s) have transitioned from 1 → 0 independent of the state of DEVSTSCHG_EN	Completion of normal device removal sequence.

The behavior of the bay state machine due to software actions is depicted in the following diagram. The OS, using the BAY_STREQ field in the BCER*x*, can transition the state machine from one state to any other state with the following restrictions:

- A device must be present in the bay. The DBC hardware must ignore any software state transition requests when the bay is empty.
- Transitions from any state to the Bay Empty state must be done by DBC hardware only

For the sake of clarity in the state diagram those transitions which are a result of "unexpected OS behavior" are shown with an (*). They are also described in the corresponding table below. All state transitions in the diagram are denoted as a write to the BAY_STREQ field of the BCER*x* (bits [6:4]). The write to the BCER*x* causes the state transition as opposed to a static value in the BCER*x*. For example, the notation 010b → BAY_STREQ indicates that the state transition occurred when 010b was written to bits [6:4] of the BCER*x* at the time the bay was occupied.

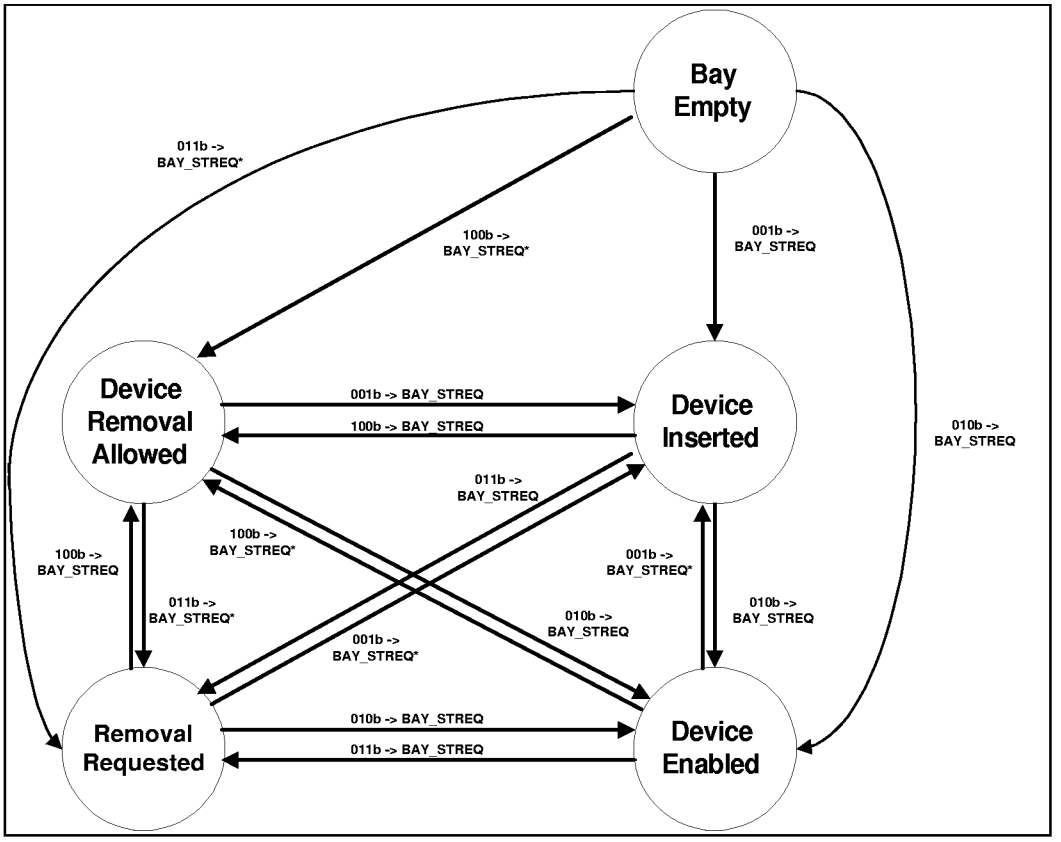


FIGURE 4 - BAY STATE DIAGRAM – SOFTWARE TRANSITIONS

These state transitions are described in more detail in the table on the following page. In this table, the term “Bay Empty” actually means that although a device is present (it must be in order to cause any software initiated state transitions) the DBC hardware could not transition out of the Bay Empty state.

Table 7 - Software Action Bay State Transition Table

CURRENT STATE	NEXT STATE	SOFTWARE ACTION	NOTES
Bay Empty (device is present)	Device Inserted	001b → BAY_STREQ	This transition request could be the result of a device currently in the bay with DEVSTSCHG_EN cleared (as such the DBC hardware could not transition the bay state).
Bay Empty (device is present)	Device Enabled	010b → BAY_STREQ	This transition request is a result of a device that has been properly enumerated and enabled on its native bus(es). In all likelihood the DEVSTSCHG_EN bit was cleared so DBC hardware could not first transition the bay state to Device Inserted.
Bay Empty (device is present)	Removal Requested	011b → BAY_STREQ	Unexpected OS behavior.
Bay Empty (device is present)	Device Removal Allowed	100b → BAY_STREQ	Unexpected OS behavior.
Device Inserted	Device Enabled	010b → BAY_STREQ	Device properly enumerated and enabled on its native bus(es).
Device Inserted	Removal Requested	011b → BAY_STREQ	Unexpected user behavior. User request device removal through the UI before the device was enabled.
Device Inserted	Device Removal Allowed	100b → BAY_STREQ	OS could not enable the device. This could be a result of the OS's failure to properly enumerate the device, lack of sufficient operational power, etc.
Device Enabled	Device Inserted	001b → BAY_STREQ	Unexpected OS behavior.
Device Enabled	Removal Requested	011b → BAY_STREQ	User request device removal through the UI.
Device Enabled	Device Removal Allowed	100b → BAY_STREQ	Unexpected OS behavior.
Removal Requested	Device Inserted	001b → BAY_STREQ	Unexpected OS behavior.
Removal Requested	Device Enabled	010b → BAY_STREQ	OS decided that device removal was not allowed. This could be the result of an active application disallowing the removal. Alternatively, the user could have cancelled the removal request through the UI.
Removal Requested	Device Removal Allowed	100b → BAY_STREQ	OS has completed the device removal sequence.

CURRENT STATE	NEXT STATE	SOFTWARE ACTION	NOTES
Device Removal Allowed	Device Inserted	001b → BAY_STREQ	User has requested to "re-use" the device through the UI. This state transition eliminates the need for the user to remove the device and then immediately re-insert it. This could be especially useful in the presence of an engaged physical security lock. This bay state transition might be used in order to provide user feedback (via the bay status indicator) while the OS is performing the steps necessary to re-enable the device.
Device Removal Allowed	Device Enabled	010b → BAY_STREQ	User has requested to "re-use" the device through the UI. This state transition eliminates the need for the user to remove the device and then immediately re-insert it. This could be especially useful in the presence of an engaged physical security lock. This state transition indicates that the device has been properly re-enumerated and re-enabled on its native bus(es).
Device Removal Allowed	Removal Requested	011b → BAY_STREQ	Unexpected OS behavior.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range.....-55° to +150°C
Lead Temperature Range (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to Ground.....Vcc+0.3V
Negative Voltage on any pin, with respect to Ground..... -0.3V
Maximum V_{CC}..... +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0°C - 70°C, VDD = 5.0V or 3.3 V ± 10%, unless otherwise noted)

TABLE 8 - DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I and IO12 Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Input Leakage (All I and IO12 buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = VDD
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA, VDD=5.0V I_{OL} = 6mA, VDD= 3.3V
High Output Level	V_{OH}	VDD-1.0V			V	I_{OH} = -6mA, VDD=5.0V I_{OH} = -3mA, VDD=3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to VDD (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24mA, VDD=5.0V I_{OL} = 12mA,VDD= 3.3V
High Output Level	V_{OH}	VDD-1.0V			V	I_{OH} = -24mA, VDD=5.0V I_{OH} = -12mA, VDD=3.3V
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA, VDD=5.0V I_{OL} = 6mA ,VDD= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to VDD
Supply Current Active	I_{CC}			5	mA	All outputs open.

Note 1: Output leakage is measured with the pin in high impedance state.

CAPACITANCE T_A = 25°C;fc = 1MHz; V_{CC} = 3.3V

Table 9 - Clock Pin Loading

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	CLKIN			20	pF	All pins except pin under test tied to AC ground
Inputs				10	pF	

AC TIMING

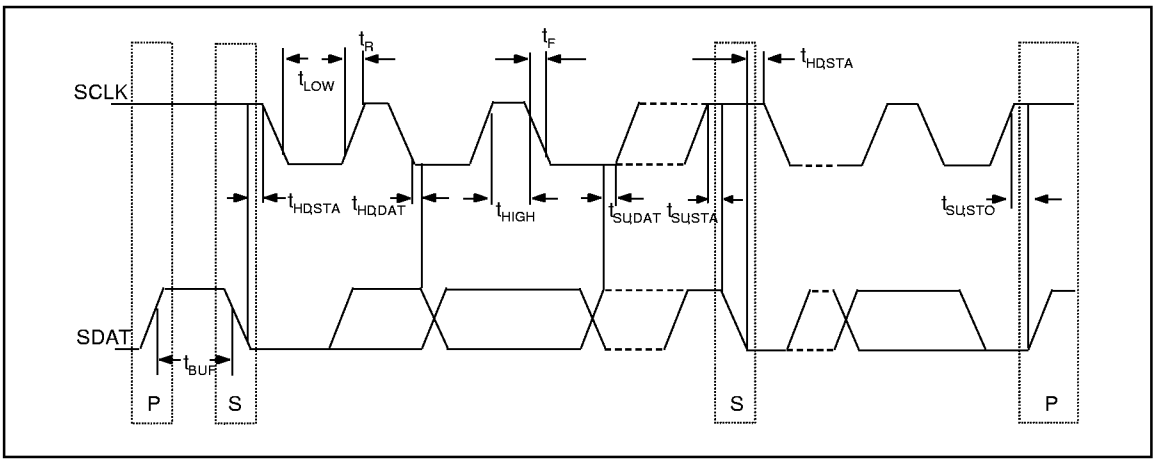


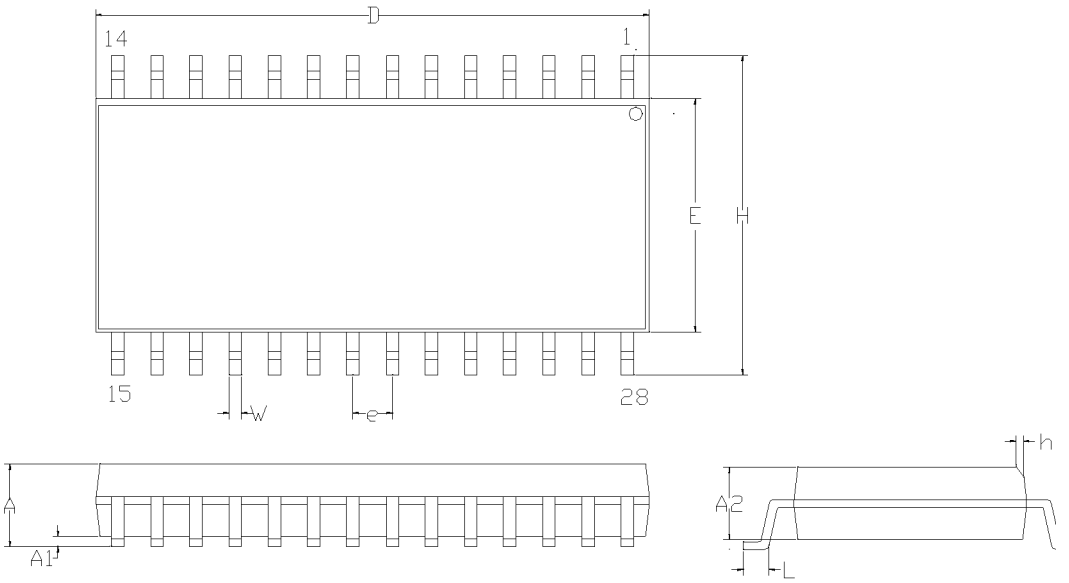
FIGURE 5 – SMBUS TIMING

AC timing is with 100pF capacitive loading.

Table 10 - SMBUS TIMING

SYMBOL	PARAMETER	LIMITS		UNITS	COMMENTS
		MIN	MAX		
FSMB	SMB Operating Frequency	10	100	kHz	
TBUF	Bus free time between Stop and Start Condition	4.7		µs	
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	4.0		µs	
TSU:STA	Repeated Start Condition setup time	4.7		µs	
TSU:STO	Stop Condition setup time	4.0		µs	
THD:DAT	Data hold time	300		ns	
TSU:DAT	Data setup time	250		ns	
TTIMEOUT	Device Timeout	25	35	ms	See Note 1
TLOW	Clock low period	4.7		µs	
THIGH	Clock high period	4.0	50	µs	See Note 2
TLOW: SEXT	Cumulative clock low extend time (slave device)		25	ms	See Note 3
TF	Clock/Data Fall Time		300	ns	
TR	Clock/Data Rise Time		1000	ns	

Note 1: A device will timeout when any clock low exceeds this value.
Note 2: THIGH Max provides a simple guaranteed method for devices to detect bus idle conditions.
Note 3: TLOW:SEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.



	MIN	NOMINAL	MAX	REMARK
A	2.35	~	2.65	Overall Package Height
A1	0.10	~	0.30	Standoff
A2	2.29	2.34	2.39	Body Thickness
D	17.70	~	18.10	X Body Size
E	7.40	~	7.60	Y Body Size
H	10.00	~	10.65	Y Span
L	0.40	~	1.27	Lead Foot Length from Centerline
C	0.23	~	0.32	Lead Thickness
h	0.25	~	0.75	Chamber
e	1.27 BSC.			Lead Pitch
	0°	~	8°	Lead Foot Angle
W	0.33	~	0.51	Lead Width
Ccc	~	~	0.09	Coplanarity *(Assemblers)*
Ccc	~	~	0.10	Coplanarity *(Test House)*

Notes:

[1] Controlling Unit: millimeter

[2] Tolerance on the position of the leads is ± 0.125 mm maximum

[3] Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm

FIGURE 6 – 28 PIN SOIC PACKAGE OUTLINE