

rev 0.4

2.5V or 3.3V, 200MHz, 14 Output Zero Delay Buffer

General Features

- Output frequency range: 8.3MHz to 200MHz
- Input frequency range: 4.2MHz to 125MHz
- 2.5V or 3.3V operation
- Split 2.5V/3.3V outputs
- 14 Clock outputs: Drive up to 28 clock lines
- 1 Feedback clock output
- 2 LVCMOS reference clock inputs
- 150pS max output-output skew
- PLL bypass mode
- 'SpreadTrak'
- Output enable/disable
- Industrial temperature range: -40°C to +85°C
- 52 Pin 1.0 mm TQFP Package
- RoHS Compliance

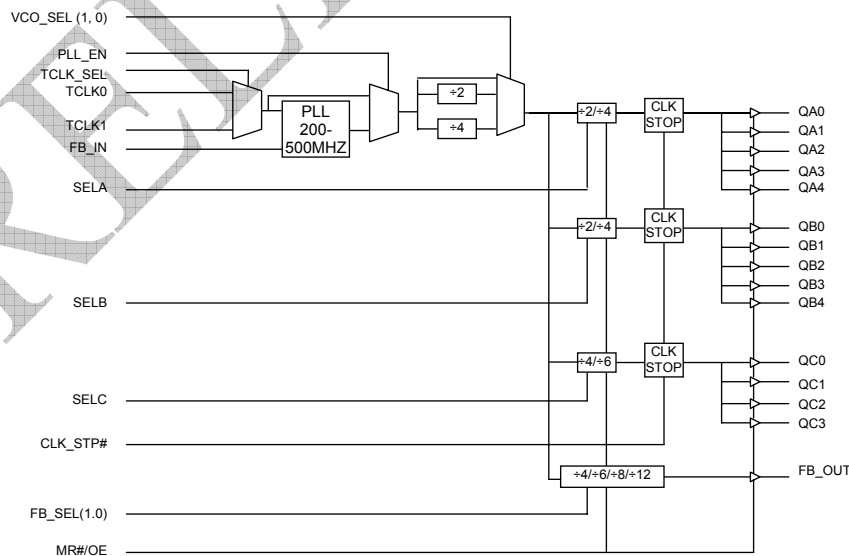
Functional Description

The PCS519775 is a low-voltage high-performance 200MHz PLL-based zero delay buffer designed for high-speed clock distribution applications. The PCS519775 features two reference clock inputs and

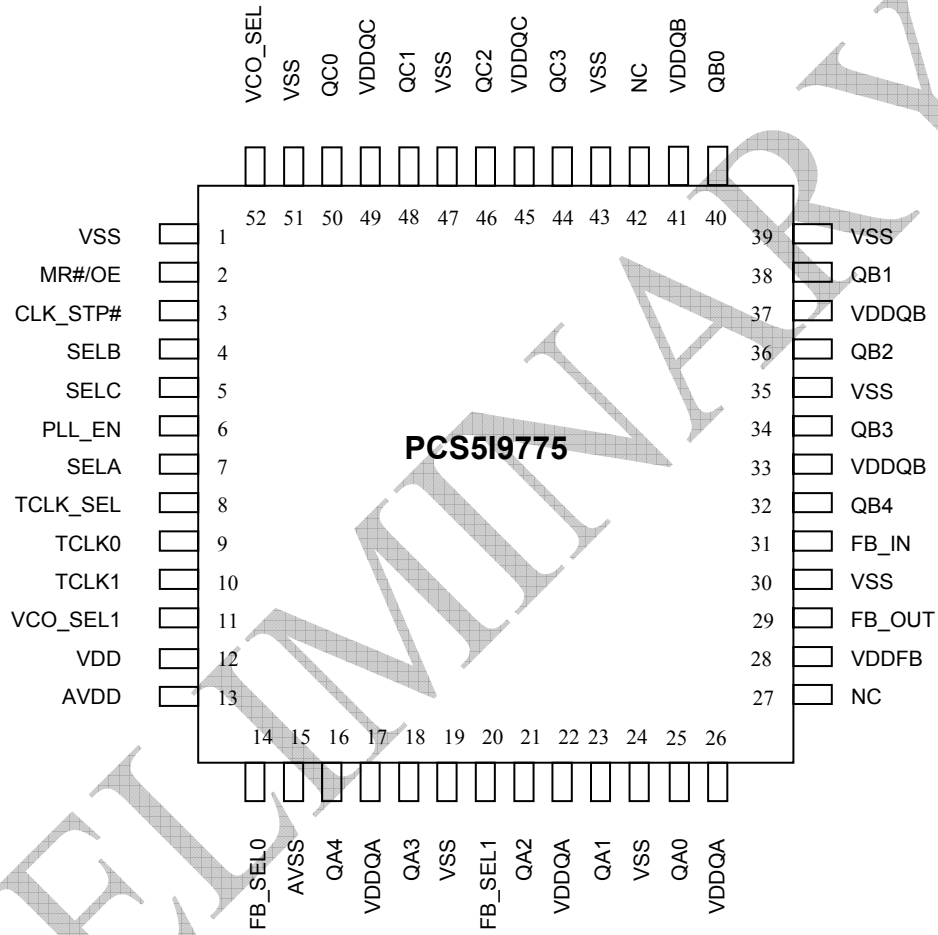
provides 14 outputs partitioned in 3 banks of 5, 5, and 4 outputs. Bank A and Bank B divide the VCO output by 4 or 8 while Bank C divides by 8 or 12 per SEL(A:C) settings, see *Functional Table*. These dividers allow output to input ratios of 6:1, 4:1, 3:1, 2:1, 3:2, 4:3, 1:1, and 2:3. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:28.

The PLL is ensured stable, given that the VCO is configured to run between 200MHz and 500MHz. This allows a wide range of output frequencies from 8.3MHz to 200MHz. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see *Frequency Table*. When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Block Diagram



Pin Configuration



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Pin Description¹

Pin	Name	I/O	Type	Description
9	TCLK0	I, PD	LVC MOS	LVC MOS/LVTTL reference clock input
10	TCLK1	I, PU	LVC MOS	LVC MOS/LVTTL reference clock input
16, 18, 21, 23, 25	QA(4:0)	O	LVC MOS	Clock output bank A
32, 34, 36, 38, 40	QB(4:0)	O	LVC MOS	Clock output bank B
44, 46, 48, 50	QC(3:0)	O	LVC MOS	Clock output bank C
29	FB_OUT	O	LVC MOS	Feedback clock output. Connect to FB_IN for normal operation.
31	FB_IN	I, PU	LVC MOS	Feedback clock input. Connect to FB_OUT for normal operation. This input should be at the same voltage rail as input reference clock. See Table 1.
2	MR#/OE	I, PU	LVC MOS	Output enable/disable input. See Table 2.
3	CLK_STP#	I, PU	LVC MOS	Clock stop enable/disable input. See Table 2.
6	PLL_EN	I, PU	LVC MOS	PLL enable/disable input. See Table 2.
8	TCLK_SEL	I, PD	LVC MOS	Reference select input. See Table 2.
11, 52	VCO_SEL(1,0)	I, PD	LVC MOS	VCO divider select input. See Tables 2, 3 and 4.
7, 4, 5	SEL(A:C)	I, PD	LVC MOS	Frequency select input, Bank (A:C). See Table 3.
20, 14	FB_SEL(1,0)	I, PD	LVC MOS	Feedback dividers select inputs. See Table 4.
17, 22, 26	VDDQA	Supply	VDD	2.5V or 3.3V Power supply for bank A output clocks ^{2,3}
33, 37, 41	VDDQB	Supply	VDD	2.5V or 3.3V Power supply for bank B output clocks ^{2,3}
45, 49	VDDQC	Supply	VDD	2.5V or 3.3V Power supply for bank C output clocks ^{2,3}
28	VDDFB	Supply	VDD	2.5V or 3.3V Power supply for feedback output clock ^{2,3}
13	AVDD	Supply	VDD	2.5V or 3.3V Power supply for PLL ^{2,3}
12	VDD	Supply	VDD	2.5V or 3.3V Power supply for core and inputs ^{2,3}
15	AVSS	Supply	Ground	Analog Ground
1, 19, 24, 30, 35, 39, 43, 47, 51	VSS	Supply	Ground	Common Ground
27, 42	NC			No Connection

Notes:

1. PU = Internal pull-up, PD = Internal pull-down
2. A 0.1µF bypass capacitor should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQA, VDDQB, VDDQC, and VDDFB power supply pins.

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‘SpreadTrak’

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. PCS5I9975A is designed so as not to filter off the Spread Spectrum feature of the Reference Input, assuming it exists.

When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

Table 1. Frequency Table

Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
÷8	Input Clock * 8	25MHz to 62.5MHz	25MHz to 50MHz
÷12	Input Clock * 12	16.6MHz to 41.6MHz	16.6MHz to 33.3MHz
÷16	Input Clock * 16	12.5MHz to 31.25MHz	12.5MHz to 25MHz
÷24	Input Clock * 24	8.3MHz to 20.8MHz	8.3MHz to 16.6MHz
÷32	Input Clock * 32	6.25MHz to 15.625MHz	6.25MHz to 12.5MHz
÷48	Input Clock * 48	4.2MHz to 10.4MHz	4.2 MHz to 8.3MHz
÷4	Input Clock * 4	50MHz to 125MHz	50MHz to 100MHz
÷6	Input Clock * 6	33.3MHz to 83.3MHz	33.3MHz to 66.6MHz
÷8	Input Clock * 8	25MHz to 62.5MHz	25MHz to 50MHz
÷12	Input Clock * 12	16.6MHz to 41.6MHz	16.6MHz to 33.3MHz

Table 2. Function Table (Configuration controls)

Control	Default	0	1
TCLK_SEL	0	TCLK0	TCLK1
VCO_SEL0	0	VCO÷2 (mid input frequency range)	VCO÷4 (low input frequency range)
VCO_SEL1	0	Gated by VCO_SEL0	VCO (high input frequency range)
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
$\overline{\text{MR/OE}}$	1	Outputs disabled (three-state) and reset of the device. During reset/output disable the PLL feedback loop is open and the VCO running at its minimum frequency. The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled
$\overline{\text{CLK_STP}}$	1	QA, QB, and QC outputs disabled in LOW state. FB_OUT is not affected by CLK_STP.	Outputs enabled

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Table 3. Function Table (Bank A, B, and C)

VCO_SEL1	VCO_SEL0	SELA	QA(4:0)	SELB	QB(4:0)	SELC	QC(3:0)
0	0	0	÷4	0	÷4	0	÷8
0	0	1	÷8	1	÷8	1	÷12
0	1	0	÷8	0	÷8	0	÷16
0	1	1	÷16	1	÷16	1	÷24
1	x	0	÷2	0	÷2	0	÷4
1	x	1	÷4	1	÷4	1	÷6

Table 4. Function Table (FB_OUT)

VCO_SEL1	VCO_SEL0	FB_SEL1	FB_SEL0	FB_OUT
0	0	0	0	÷8
0	0	0	1	÷16
0	0	1	0	÷12
0	0	1	1	÷24
0	1	0	0	÷16
0	1	0	1	÷32
0	1	1	0	÷24
0	1	1	1	÷48
1	x	0	0	÷4
1	x	0	1	÷8
1	x	1	0	÷6
1	x	1	1	÷12

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
VDD	DC Supply Voltage		-0.3	5.5	V
VDD	DC Operating Voltage	Functional	2.375	3.465	V
V _{IN}	DC Input Voltage	Relative to VSS	-0.3	VDD + 0.3	V
V _{OUT}	DC Output Voltage	Relative to VSS	-0.3	VDD + 0.3	V
V _{TT}	Output termination Voltage			VDD ÷ 2	V
LU	Latch Up Immunity	Functional	200		mA
R _{PS}	Power Supply Ripple	Ripple Frequency < 100kHz		150	mVp-p
T _S	Temperature, Storage	Non Functional	-65	+150	°C
T _A	Temperature, Operating Ambient	Functional	-40	+85	°C
T _J	Temperature, Junction	Functional		150	°C
Ø _{JC}	Dissipation, Junction to Case	Functional		23	°C/W
Ø _{JA}	Dissipation, Junction to Ambient	Functional		55	°C/W
ESD _H	ESD Protection (Human Body Model)		2000		Volts
FIT	Failure in Time	Manufacturing test		10	ppm

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DC Electrical Specifications (VDD= 3.3V ± 5%, T_A = -40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V _{IL}	Input Voltage, Low	LVC MOS			0.8	V
V _{IH}	Input Voltage, High	LVC MOS	2.0		VDD+0.3	V
V _{OL}	Output Voltage, Low ⁴	I _{OL} = 24 mA			0.55	V
		I _{OL} = 12 mA			0.30	
V _{OH}	Output Voltage, High ⁴	I _{OH} = -24 mA	2.4		-	V
I _{IL}	Input Current, Low ⁵	V _{IL} = VSS			-100	μA
I _{IH}	Input Current, High ⁵	V _{IL} = VDD			100	μA
I _{DDA}	PLL Supply Current	AVDD only		5	10	mA
I _{DDQ}	Quiescent Supply Current	All VDD pins except AVDD			1	mA
I _{DD}	Dynamic Supply Current	Outputs loaded @ 100MHz		225		mA
		Outputs loaded @ 200MHz		290		
C _{IN}	Input Pin Capacitance			4		pF
Z _{OUT}	Output Impedance		12	15	18	Ω

DC Electrical Specifications (VDD= 2.5V ± 5%, T_A = -40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max	Unit
V _{IL}	Input Voltage, Low	LVC MOS			0.7	V
V _{IH}	Input Voltage, High	LVC MOS	1.7		VDD+0.3	V
V _{OL}	Output Voltage, Low ⁴	I _{OL} = 15 mA	-		0.6	V
V _{OH}	Output Voltage, High ⁴	I _{OH} = -15 mA	1.8		-	V
I _{IL}	Input Current, Low ⁵	V _{IL} = VSS			-100	μA
I _{IH}	Input Current, High ⁵	V _{IL} = VDD			100	μA
I _{DDA}	PLL Supply Current	AVDD only		5	10	mA
I _{DDQ}	Quiescent Supply Current	All VDD pins except AVDD			1	mA
I _{DD}	Dynamic Supply Current	Outputs loaded @ 100MHz		135		mA
		Outputs loaded @ 200MHz		160		
C _{IN}	Input Pin Capacitance			4		pF
Z _{OUT}	Output Impedance		14	18	22	Ω

Notes:

- 4. Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50Ω series terminated transmission lines.
- 5. Inputs have pull-up or pull-down resistors that affect the input current.

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AC Electrical Specifications⁶ (VDD= 2.5V ± 5%, T_A = -40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
f _{VCO}	VCO Frequency		200		400	MHz
f _{in}	Input Frequency	÷4 Feedback	50		100	MHz
		÷6 Feedback	33.3		66.6	
		÷8 Feedback	25		50	
		÷12 Feedback	16.7		33.3	
		÷16 Feedback	12.5		25	
		÷24 Feedback	8.3		16.7	
		÷32 Feedback	6.3		12.5	
		÷48 Feedback	4.2		8.3	
		Bypass mode (PLL_EN = 0)	0		200	
f _{refDC}	Input Duty Cycle		25		75	%
t _r , t _f	TCLK Input Rise/Fall Time	0.7V to 1.7V	-		1.0	nS
f _{MAX}	Maximum Output Frequency	÷2 Output	100		200	MHz
		÷4 Output	50		100	
		÷6 Output	33.3		66.6	
		÷8 Output	25		50	
		÷12 Output	16.7		33.3	
		÷16 Output	12.5		25	
		÷24 Output	8.3		16.7	
DC	Output Duty Cycle		45		55	%
t _r , t _f	Output Rise/Fall times	0.7V to 1.8V	0.1		1.0	nS
t _(φ)	Propagation Delay (static phase offset)	TCLK to FB_IN, does not include jitter	-100		100	pS
t _{sk(O)}	Output-to-Output Skew	Skew within Bank			150	pS
t _{sk(B)}	Bank-to-Bank Skew	Banks at same frequency			150	pS
		Banks at different frequency			225	
t _{PLZ, HZ}	Output Disable Time				10	nS
t _{PZL, ZH}	Output Enable Time				10	nS
BW	PLL Closed Loop Bandwidth (-3 dB)	VCO_SEL = 0		0.5 - 1.0		MHz
		VCO_SEL = 1		1.0 - 2.0		
t _{JIT(CC)}	Cycle-to-Cycle Jitter	Same frequency			150	pS
		Multiple frequencies			300	
t _{JIT(PER)}	Period Jitter				100	pS
t _{JIT(φ)}	I/O Phase Jitter				150	pS
t _{LOCK}	Maximum PLL Lock Time				1	mS

Note:

6. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Parameters are guaranteed by characterization and are not 100% tested.

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AC Electrical Specifications⁶ (VDD= 3.3V ± 5%, TA = -40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
f _{VCO}	VCO Frequency		200		500	MHz
f _{in}	Input Frequency	÷4 Feedback	50		125	MHz
		÷6 Feedback	33.3		83.3	
		÷8 Feedback	25		62.5	
		÷12 Feedback	16.7		41.6	
		÷16 Feedback	12.5		31.3	
		÷24 Feedback	8.3		20.8	
		÷32 Feedback	6.3		15.6	
		÷48 Feedback	4.2		10.4	
	Bypass mode (PLL_EN = 0)	0		200		
f _{refDC}	Input Duty Cycle		25		75	%
t _r , t _f	TCLK Input Rise/Fall Time	0.8V to 2.0V	-		1.0	nS
f _{MAX}	Maximum Output Frequency	÷2 Output	100		200	MHz
		÷4 Output	50		125	
		÷6 Output	33.3		83.3	
		÷8 Output	25		62.5	
		÷12 Output	16.7		41.6	
		÷16 Output	12.5		31.3	
		÷24 Output	8.3		20.8	
DC	Output Duty Cycle		45		55	%
t _r , t _f	Output Rise/Fall times	0.8V to 2.4V	0.1		1.0	nS
t _(φ)	Propagation Delay (static phase offset)	TCLK to FB_IN, same VDD, does not include jitter	-100		100	pS
t _{sk(O)}	Output-to-Output Skew	Skew within Bank			150	pS
t _{sk(B)}	Bank-to-Bank Skew	Banks at same voltage, same frequency			150	pS
		Banks at same voltage, different frequency			225	
		Banks at different voltage			250	
t _{PLZ, HZ}	Output Disable Time				10	nS
t _{PZL, ZH}	Output Enable Time				10	nS
BW	PLL Closed Loop Bandwidth (-3dB)	VCO_SEL = 0		0.5 - 1.0		MHz
		VCO_SEL = 1		1.0 - 2.0		
t _{JIT(CC)}	Cycle-to-Cycle Jitter	Same frequency			150	pS
		Multiple frequencies			300	
t _{JIT(PER)}	Period Jitter				100	pS
t _{JIT(φ)}	I/O Phase Jitter	I/O at same VDD			150	pS
t _{LOCK}	Maximum PLL Lock Time				1	mS

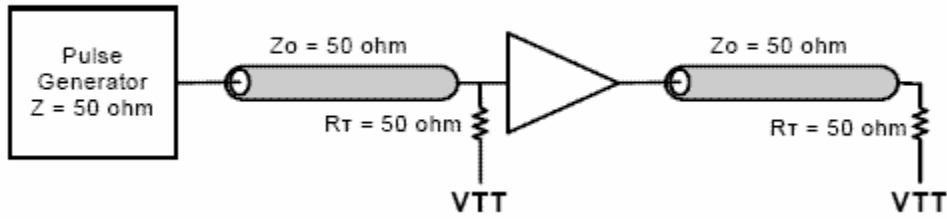


Figure 1. AC Test Reference for VDD = 3.3V / 2.5V

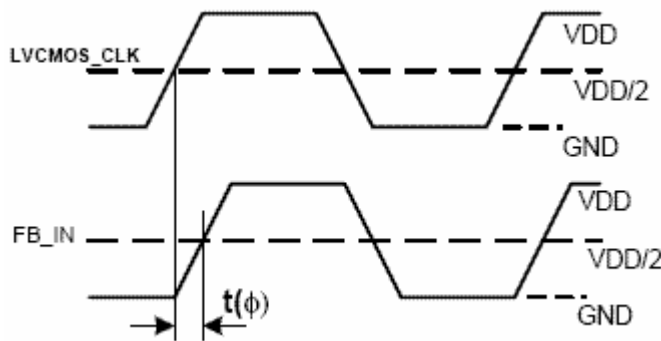


Figure 2. Propagation Delay $t(\phi)$, Static Phase Offset

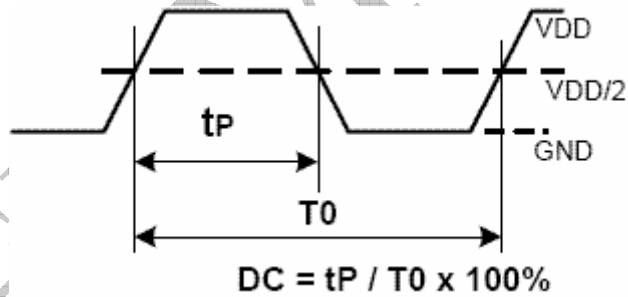


Figure 3. Output Duty Cycle (DC)

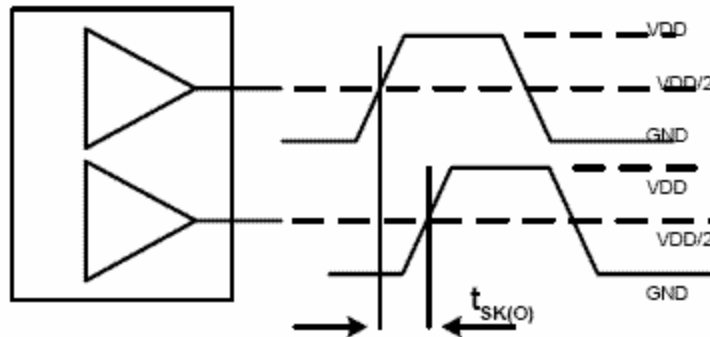
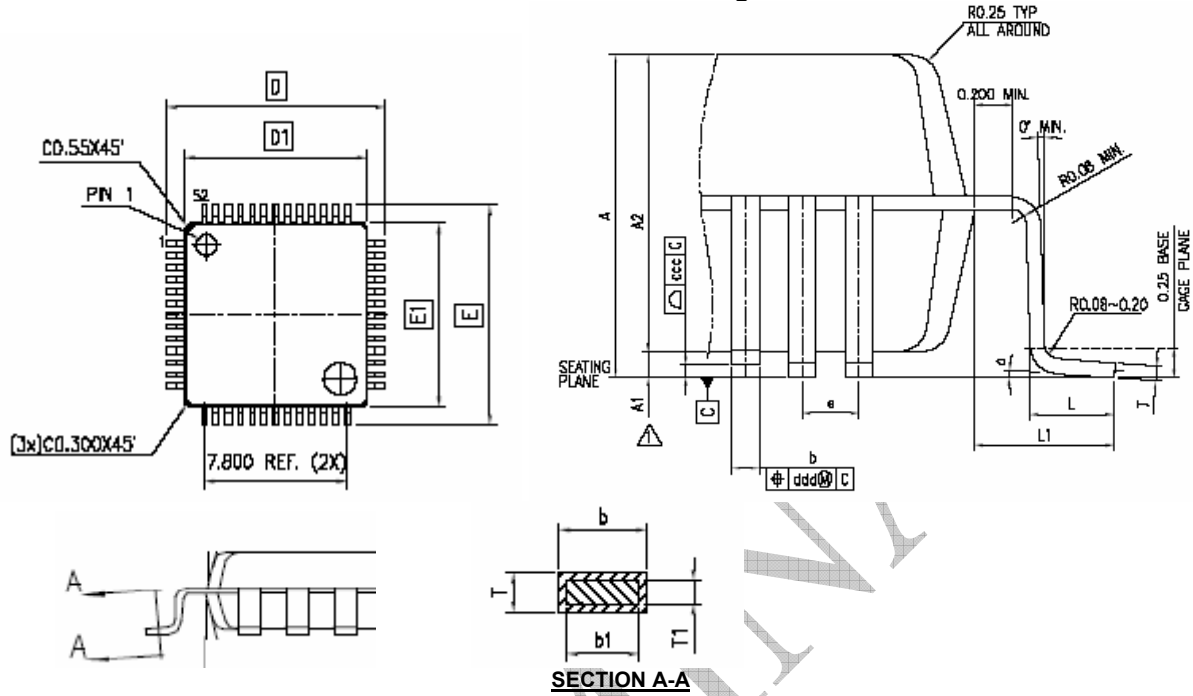


Figure 4. Output-to-Output Skew, $t_{sk(O)}$

52-lead TQFP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0472	...	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.4646	0.4803	11.8	12.2
D1	0.3898	0.3976	9.9	10.1
E	0.4646	0.4803	11.8	12.2
E1	0.3898	0.3976	9.9	10.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0102	0.0150	0.26	0.38
b1	0.0106	0.0130	0.27	0.33
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.0256 BASE		0.65 BASE	

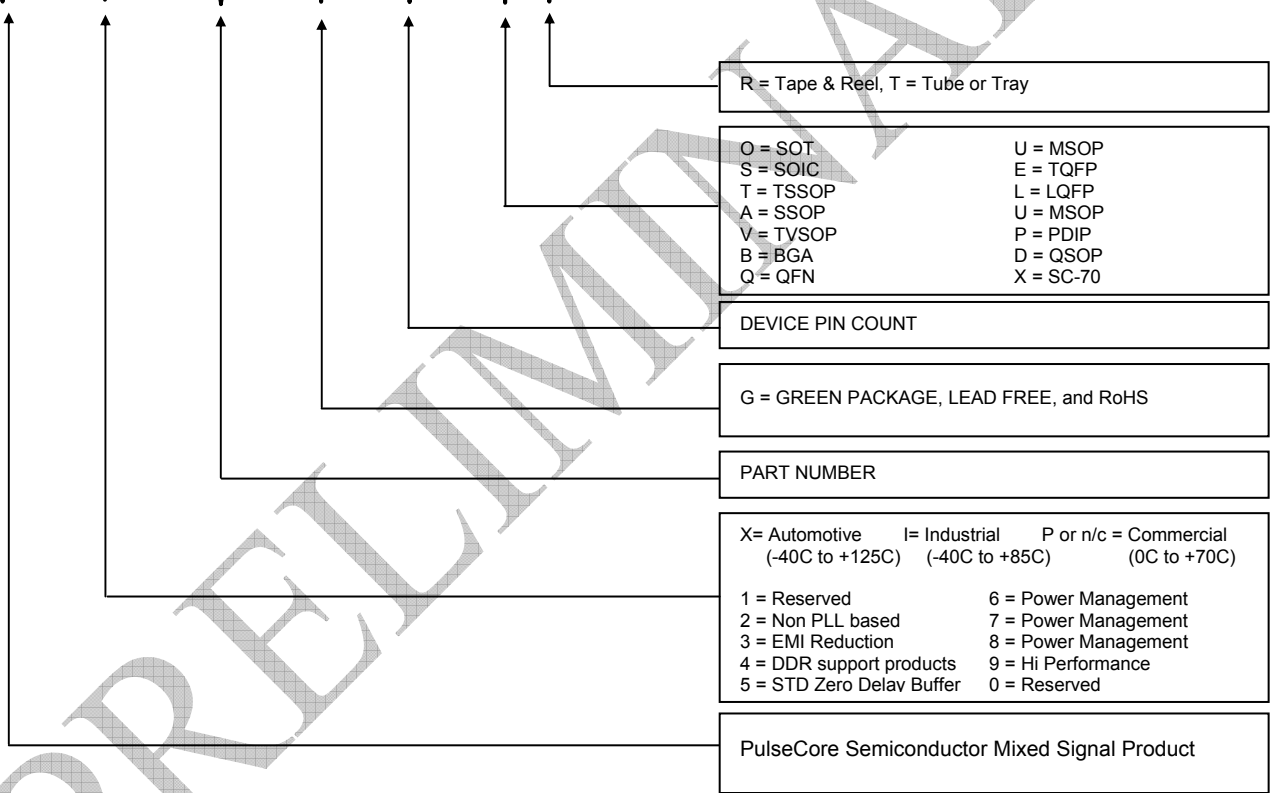
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Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS5P9775G-52-ET	PCS5P9775G	52-pin TQFP, Tray, Green	Commercial
PCS5P9775G-52-ER	PCS5P9775G	52-pin TQFP – Tape and Reel, Green	Commercial
PCS5I9775G-52-ET	PCS5I9775G	52-pin TQFP, Tray, Green	Industrial
PCS5I9775G-52-ER	PCS5I9775G	52-pin TQFP – Tape and Reel, Green	Industrial

Device Ordering Information

PCS5I9775G-52-ET



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Preliminary Information
Part Number: PCS5I9775
Document Version: 0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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