Ordering number : EN8321A

SANYO Semiconductors
DATA SHEET

Monolithic Digital IC

LB11600JV — Brushless Motor Predriver IC for Automotive Applications

Overview

The LB11600JV is a direct PWM drive predriver IC appropriate for 3-phase power brushless motors in automotive applications. This IC can implement either high side PWM drive or low side PWM drive motor driver circuits depending on the configuration of the output circuits, which use discrete transistors such as MOSFETs or bipolar transistors. In addition to a full complement of protection functions, including overcurrent, thermal, motor constraint, and undervoltage protection, the LB11600JV also provides an integrated speed control function. Thus the LB11600JV can implement high reliability/high functionality drive circuits.

Functions

- Three-phase bipolar drive (UH, VH, and WH pins, PWM control)
- Forward/reverse switching circuit
- Overcurrent protection circuit
- Undervoltage protection circuit
- Motor constraint protection circuit
- Thermal protection circuit
- Speed control circuit

Applications

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Rated value	Unit
Supply voltage	V_{CC} max	V_{CC} Pin	14.5	V
Output Circuit current	I_O max	UL, VL, WL, UH, VH, and WH pins	40	mA
Allowable power dissipation	Pd max	Independent IC	0.5	W
Operating temperature	Topr		-40 to 100	°C
Storage temperature	Tstg		-55 to 150	°C

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Rated value	Unit
V_{CC} voltage supply voltage range	V_{CC}	V_{CC} Pin	4.5 to 14	V
Output current	V_{CC} op	UL, VL, WL, UH, VH, and WH pins	30	mA
RF pin voltage	VRF		0 to 3	V
HP pin voltage	VHP		0 to 14	V
HP pin voltage	IHP		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Rated value			Unit
			Min.	Typ.	Max.	
Current drain 1	$I_{CC}1$	S/S = 0V	13	20	27	mA
Current drain 2	$I_{CC}2$	Stop mode, S/S = 5V	1.5	2.5	3.5	mA
Output Block						
Output voltage 1-1	$V_{OUT}1$-1	Low level, IO = 400μA		0.1	0.3	V
Output voltage 1-2	$V_{OUT}1$-2	Low level, IO = 10mA		0.8	1.1	V
Output voltage 2	$V_{OUT}2$	High level, IO = -20mA	V_{CC}-1.1	V_{CC}-0.9		V
Hall Amplifier Block						
Input bias current	IHB (HA)		-2	-0.5		μA
Common-mode input voltage range 1	VICM1	When a Hall effect element is used	0.5		V_{CC}-2.0	V
Common-mode input voltage range 2	VICM2	When a single-sided input bias is used (Hall IC applications)	0		V_{CC}	V
Hall input sensitivity			80			mV_{P-P}
Hysteresis	ΔVIN (HA)		15	24	40	mV
Input voltage (low → high)	VSLH (HA)		5	12	20	mV
Input voltage (high → low)	VSHL (HA)		-20	-12	-5	mV
TOC Pin						
Input voltage 1	VTOC1	Output duty: 100%	2.72	3.0	3.30	V
Input voltage 2	VTOC2	Output duty: 0%	1.15	1.35	1.55	V
Input voltage 1L	VTOC1L	When V_{CC} = 4.7V Output duty: 100%	2.5	2.80	3.1	V
Input voltage 2L	VTOC2L	When V_{CC} = 4.7V, Output duty: 0%	1.05	1.24	1.43	V
Input voltage 1H	VTOC1H	When V_{CC} = 5.3V, Output duty: 100%	2.88	3.20	3.52	V
Input voltage 2H	VTOC2H	When V_{CC} = 5.3V, Output duty: 0%	1.17	1.38	1.59	V
CTL Pin						
Input offset voltage	V_{IO} (CONT)		-10		10	mV
Input bias current	IB (CONT)		-1		1	μA
Common-mode input voltage range	VICM		0		V_{CC}-1.7	V
High-level output voltage	V_{OH} (CONT)	ITOC = -0.2mA	V_{CC}-1.1	V_{CC}-0.8		V
Low-level output voltage	V_{OL} (CONT)	ITOC = 0.2mA		0.8	1.1	V
PWM Oscillator (PWM pin)						
High-level output voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Low-level output voltage	V_{OL} (PWM)		1.2	1.35	1.5	V
External capacitor charge current	1CHG	PWM = 2.1V	-60	-45	-30	μA
Oscillator frequency	F (PWM)	C = 1000pF	20	25	30	kHz
Amplitude	Vp-p (PWM)		1.25	1.65	2.05	V_{P-P}
HP Pin						
Output saturation voltage	VHPL	I_O = 7mA		0.15	0.5	V
Output leakage current	IHPleak	V_O = 13.5V			10	μA

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Parameter	Symbol	Conditions	Rated value			Unit
			Min.	Typ.	Max.	
Motor Constraint Protection Circuit Block (CSD and CSET pins)						
CSD saturation voltage	VSCSD	I_0 = -0.5mA, V_{CC}-VCSD		0.1	0.3	V
CSD off voltage	VCSDOF		0.55	0.6	0.65	V
CSD voltage	VCSD	CSET = 4.9V	4.7	4.9		V
CSET pin current	ICSET	CSET = 4.8V	35	50	65	μA
CSET pin on voltage	VCSETON	V_{CC} - CSET pin		0.1	0.3	V
CSET pin off voltage	VCSETOFF	V_{CC} - CSET pin	0.6	0.7	0.85	V
Current Limiter Circuit (RF pin)						
Limiter voltage	VRF		0.216	0.24	0.264	V
RFGND pin current	IRFGND	RFGND = 0V	-60	-40	-20	μA
Undervoltage Protection Circuit						
Operating voltage	VSDL		3.6	3.8	4.0	V
Release voltage	VSDH		4.1	4.3	4.5	V
Hysteresis	ΔVSD		0.35	0.5	0.65	V
Thermal Shutdown Circuit (thermal protection circuit)						
Thermal shutdown temperature	TSD	Design target value (junction temperature)*	150	170		°C
Hysteresis	ΔTSD	Design target value (junction temperature)*		25		°C
CEG Pin						
CEG pin current	ICEG	CEG = 4.8V	35	50	65	μA
CEG pin on voltage	VCEGON	V_{CC} - CSET pin		0.1	0.3	V
CEG pin off voltage	VCEGOFF	V_{CC} - CSET pin	0.6	0.7	0.85	V
CR Pin						
High-level output voltage	V_{OH} (CR)		3.12	3.4	3.68	V
Low-level output voltage	V_{OL} (CR)		0.67	0.75	0.83	V
Clamp voltage	VCLP (CR)		1.3	1.45	1.6	V
FV Pin						
Charge current	ICHG1	FV = 2.5V	-420	-300	-230	μA
Discharge current	ICHG2	FV = 1V	1.3	2.5	5.0	mA
FV pin high-level voltage	VOFVH	I_O = -200μA	4.7	4.9		V
FV pin low-level voltage	VOFVL	I_O = 200μA		0.15	0.3	V
S/S Pin						
High-level input voltage	V_{IH}(SS)		2.0			V
Low-level input voltage	V_{IL}(SS)				1.0	V
Input open voltage	V_{IO}(SS)		V_{CC}-0.5		V_{CC}	V
Hysteresis	V_{IS}(SS)		0.2	0.3	0.4	V
High-level input current	I_{IH}(SS)	S/S = 5V	-10	0	10	μA
Low-level input current	I_{IL}(SS)	S/S = 0V	-130	-96		μA
F/R Pin						
High-level input voltage	V_{IH} (FR)		2.0			V
Low-level input voltage	V_{IL} (FR)				1.0	V
Input open voltage	V_{IO} (FR)		V_{CC}-0.5		V_{CC}	V
Hysteresis	V_{IS} (FR)		0.2	0.3	0.4	V
High-level input current	I_{IH} (FR)	F/R = 5V	-10	0	10	μA
Low-level input current	I_{IL} (FR)	F/R = 0V	-130	-96		μA

*: These are design target value and are not tested.

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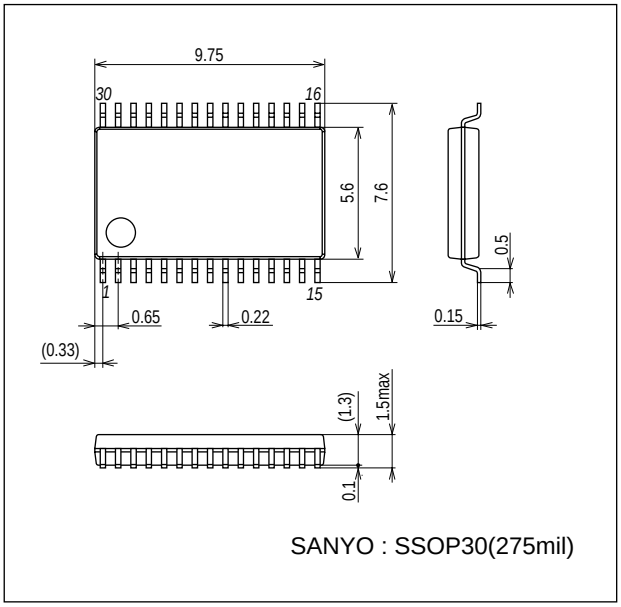
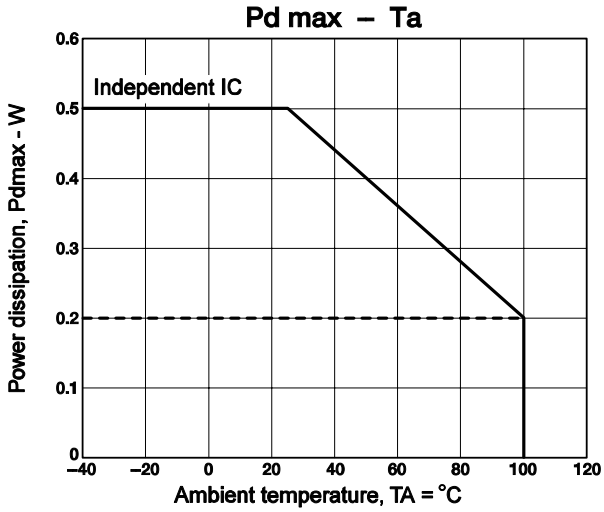
Parameter	Symbol	Conditions	Rated value			Unit
			Min.	Typ.	Max.	
PWMIN Pin						
High-level input voltage	V_{IH} (PWMIN)		2.0			V
Low-level input voltage	V_{IL} (PWMIN)				1.0	V
Input open voltage	V_{IO} (PWMIN)		V_{CC}-0.5		V_{CC}	V
Hysteresis	V_{IS} (PWMIN)		0.2	0.3	0.4	V
High-level input current	I_{IH} (PWMIN)	PWMIN = 5V	-10	0	10	μA
Low-level input current	I_{IL} (PWMIN)	PWMIN = 0V	-130	-96		μA
Input frequency	F (PWMIN)				50	kHz
PWMRE Pin						
PWMRE pin current	IPWMIRE	PWMRE = 0V	-260	-200	-140	μA
Threshold voltage	PWMRETH		1.12	1.25	1.38	V
Hysteresis	PWMREHYS		0.44	0.7	1.1	V

Package Dimensions

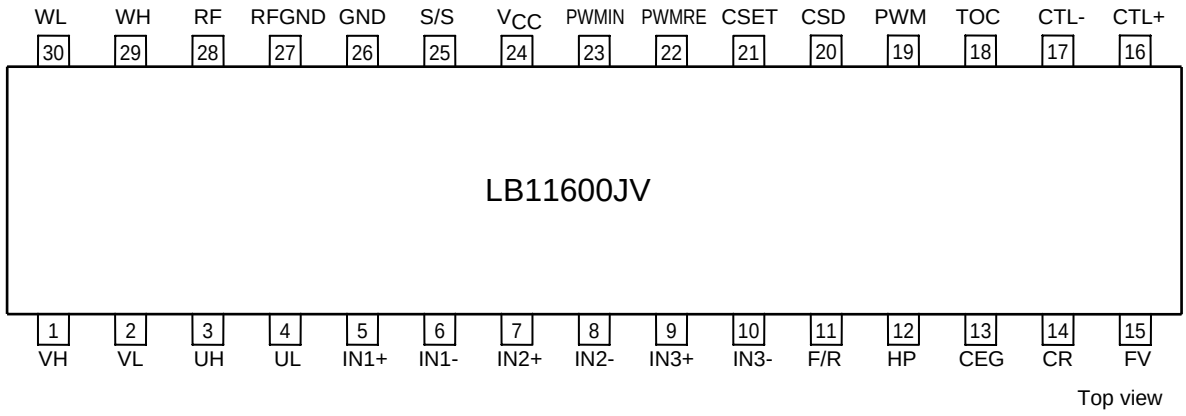
unit : mm (typ)
3191B



SANYO : SSOP30(275mil)



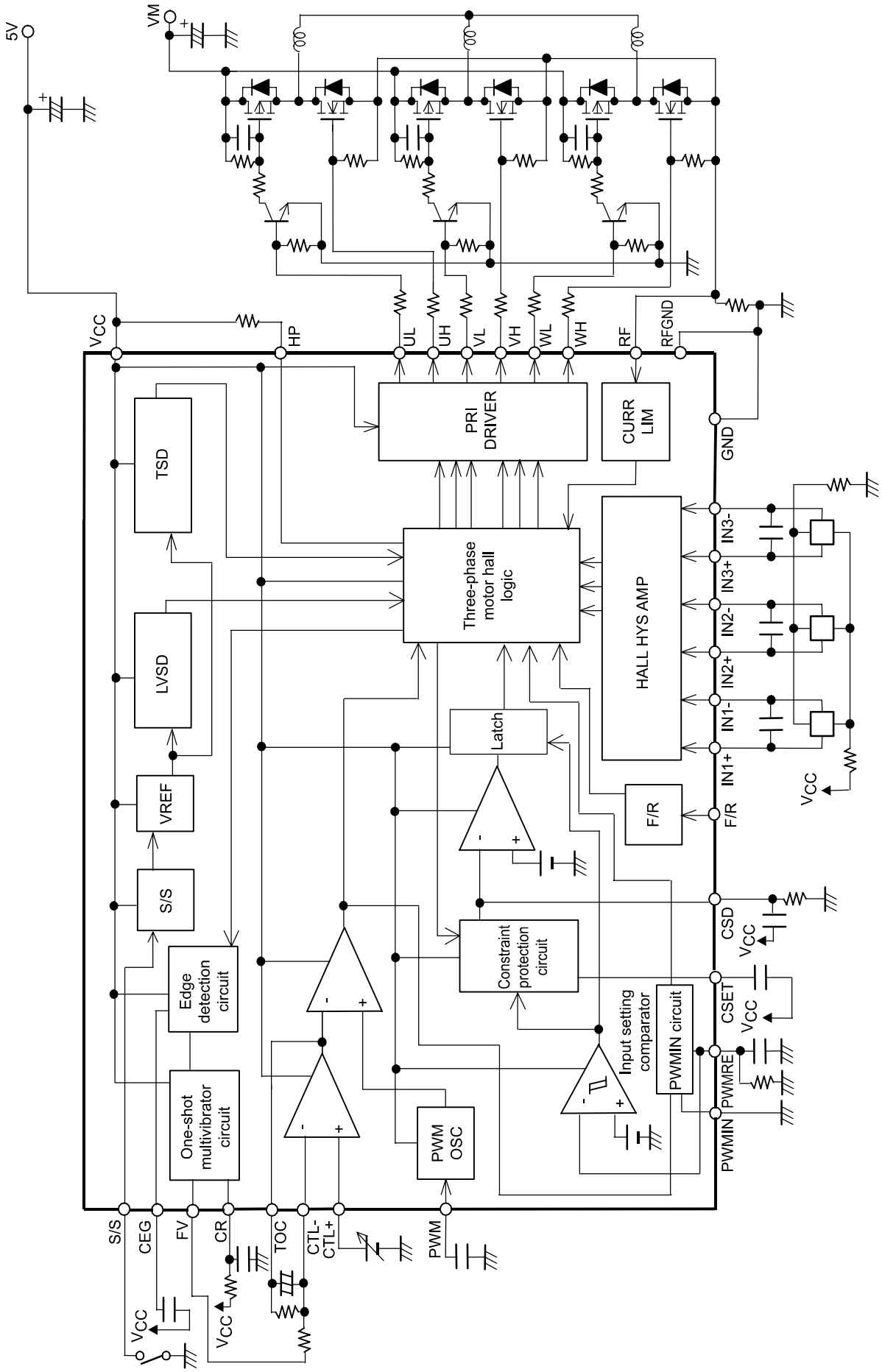
Pin Assignment



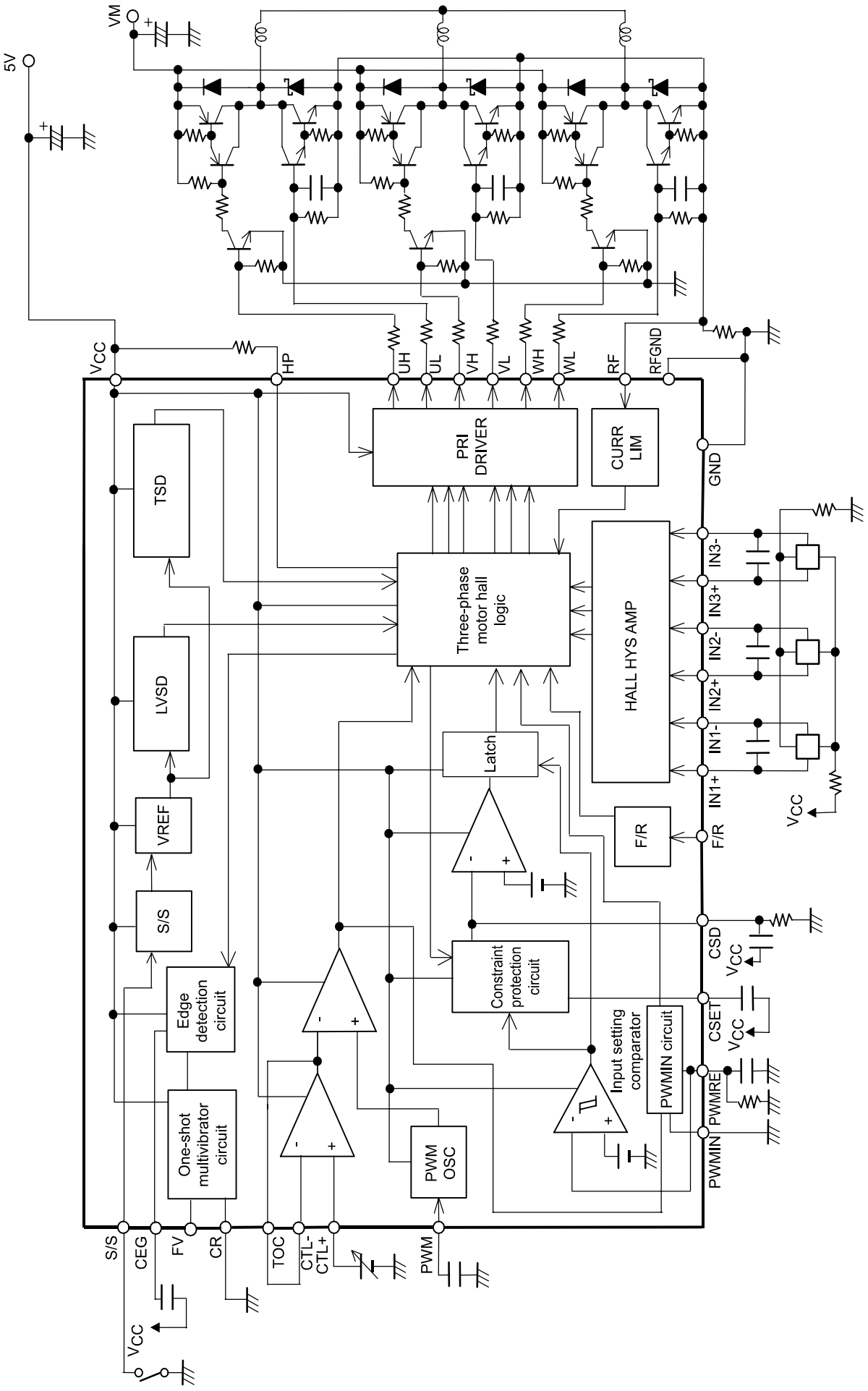
Top view

Block Diagram and Application Circuit 1

: MOS transistor drive (low side PWM), speed control feedback application



Application Circuit 2: Bipolar transistor (high side PWM)



Truth Table

- Three-Phase Logic Truth Table (IN = H means that the input is in the IN+ > IN- state.)

	F/R=[L]			F/R=[H]			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	Fixed
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

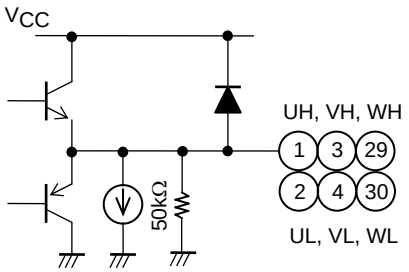
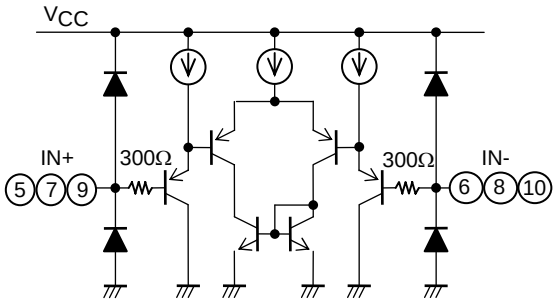
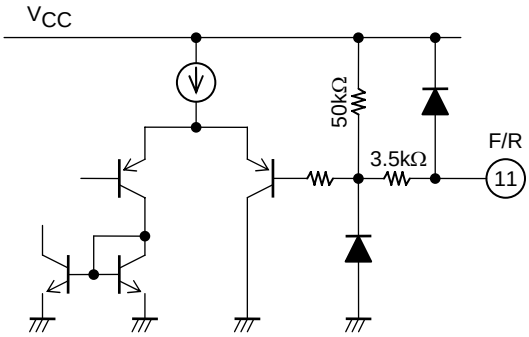
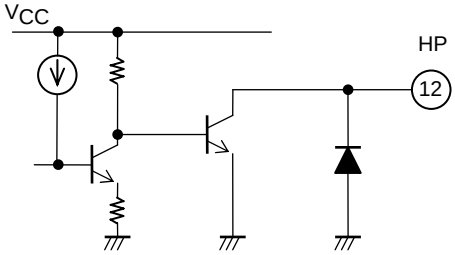
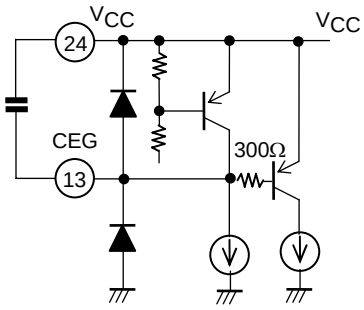
When F/R is low, the IC recognizes the states where the Hall inputs in the above table occur in the order 1 → 6 as forward rotation, and the reverse order as reverse rotation.
When F/R is high, the IC recognizes the states where the Hall inputs in the above table occur in the order 6 → 1 as forward rotation, and the reverse order as reverse rotation.

- S/S Pin

Input state	Operating state
High or open	Stop state
L	Start state

If the S/S pin is not used, the input must be held at the low-level voltage.

Pin Functions

Pin Number	Function	Function	Equivalent circuit
1 2 3 4 29 30	VH VL UH UL WH WL	Outputs. These are push-pull outputs. Duty control is applied to the UH, VH, and WH pins. Internal 50kΩ leakage protection resistors between the outputs and ground are provided to protect against output leakage in standby mode.	
5 6 7 8 9 10	IN1+ IN1- IN2+ IN2- IN3+ IN3-	Hall effect sensor inputs from each motor phase. The logic high state corresponds to the state where IN+ > IN-. If input is provided from a Hall IC, the common mode input range can be expanded by biasing either the + or - input.	
11	F/R	Forward/reverse switching input.	
12	HP	Hall signal single-phase output. (This pin is an open-collector output.) This pin outputs a signal that is inverted from the signal formed from the IN3 input.	
13	CEG	Rotation pulse edge detection input. (This input is used by the one-shot multivibrator circuit.) Insert a capacitor between this pin and V_{CC}.	

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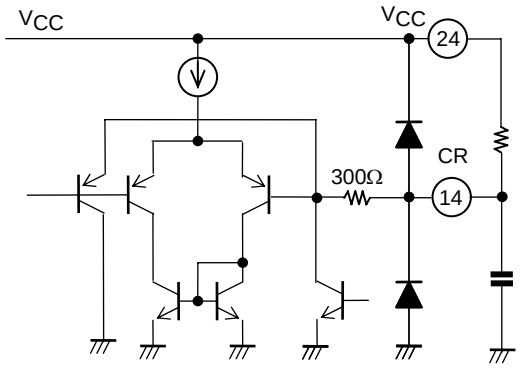
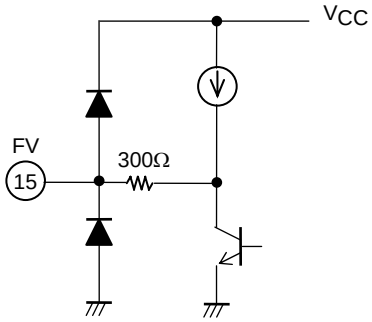
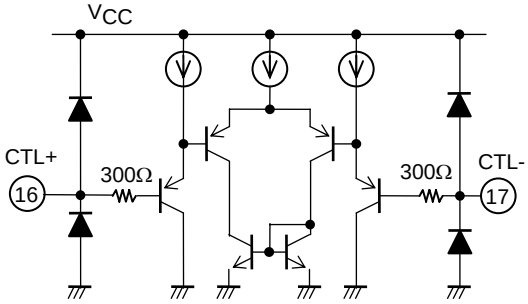
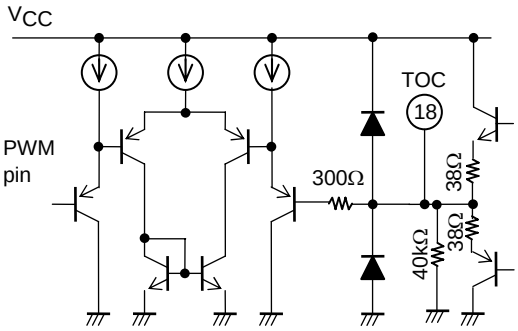
Pin Number	Function	Function	Equivalent circuit
14	CR	One-shot multivibrator pulse width setting. Insert a resistor between this pin and V_{CC} and a capacitor between this pin and ground. If unused: short to ground.	
15	FV	Hall signal one-shot multivibrator output. If unused: leave open.	
16 17	CTL+ CTL-	CTL+: Control voltage input (Integrating amplifier noninverting input) CTL-: Control voltage input (Integrating amplifier inverting input)	
18	TOC	PWM waveform comparator (Integrating amplifier output)	

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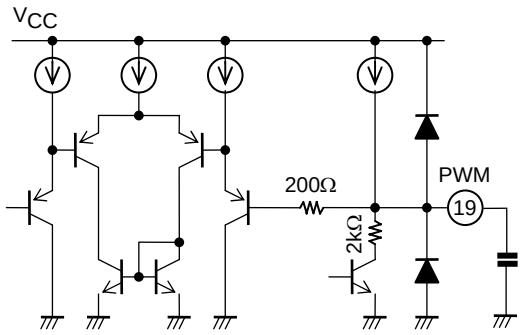
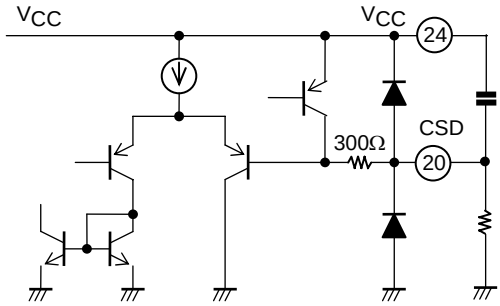
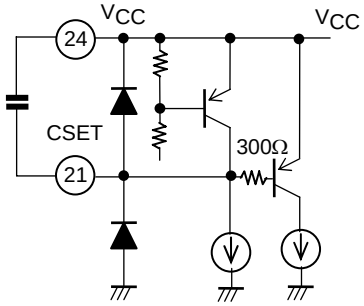
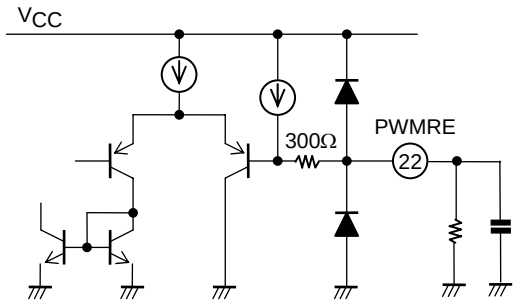
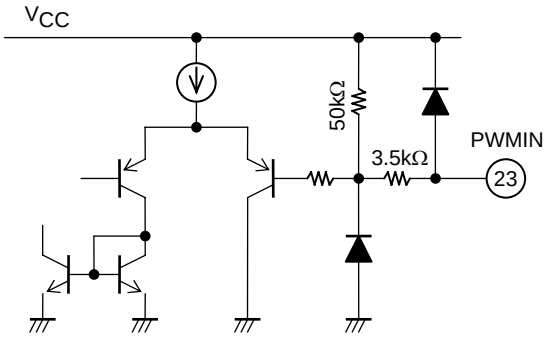
Pin Number	Function	Function	Equivalent circuit
19	PWM	PWM oscillator frequency setting. Insert a capacitor between this pin and ground.	
20	CSD	Motor constraint protection detection sense input. Insert a capacitor between this pin and V_{CC} and a resistor between this pin and ground.	
21	CSET	Motor constraint protection circuit rotation input pulse detection. Insert a capacitor between this pin and V_{CC}.	
22	PWMRE	PWM input reset. Insert a resistor and a capacitor between this pin and ground.	
23	PWMIN	External PWM input. When the input is low, the out put will be in the drive state and when the input is high or open, the output will be off.	

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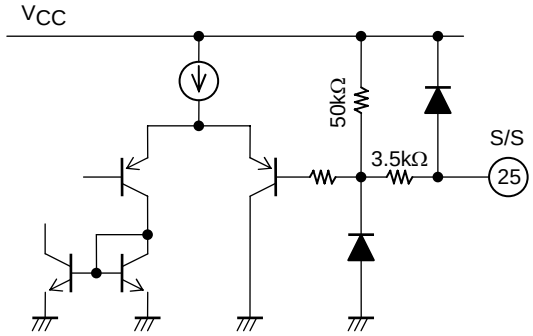
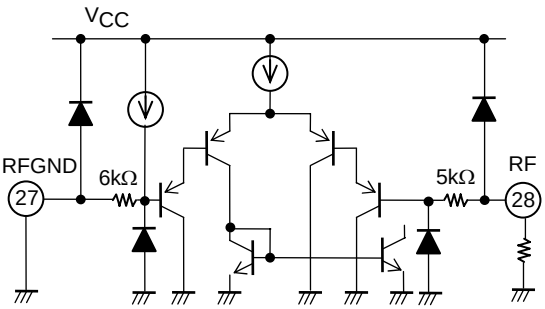
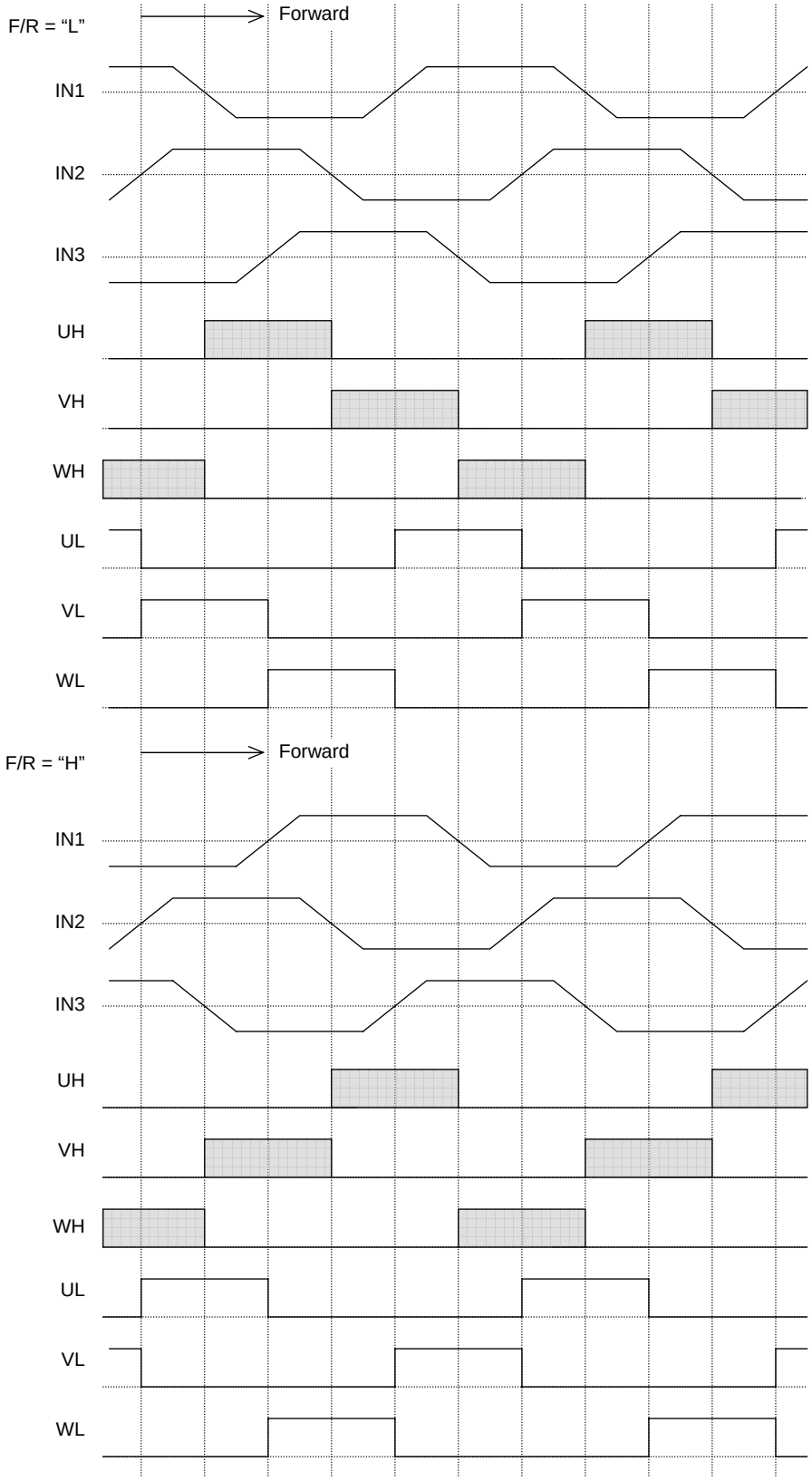
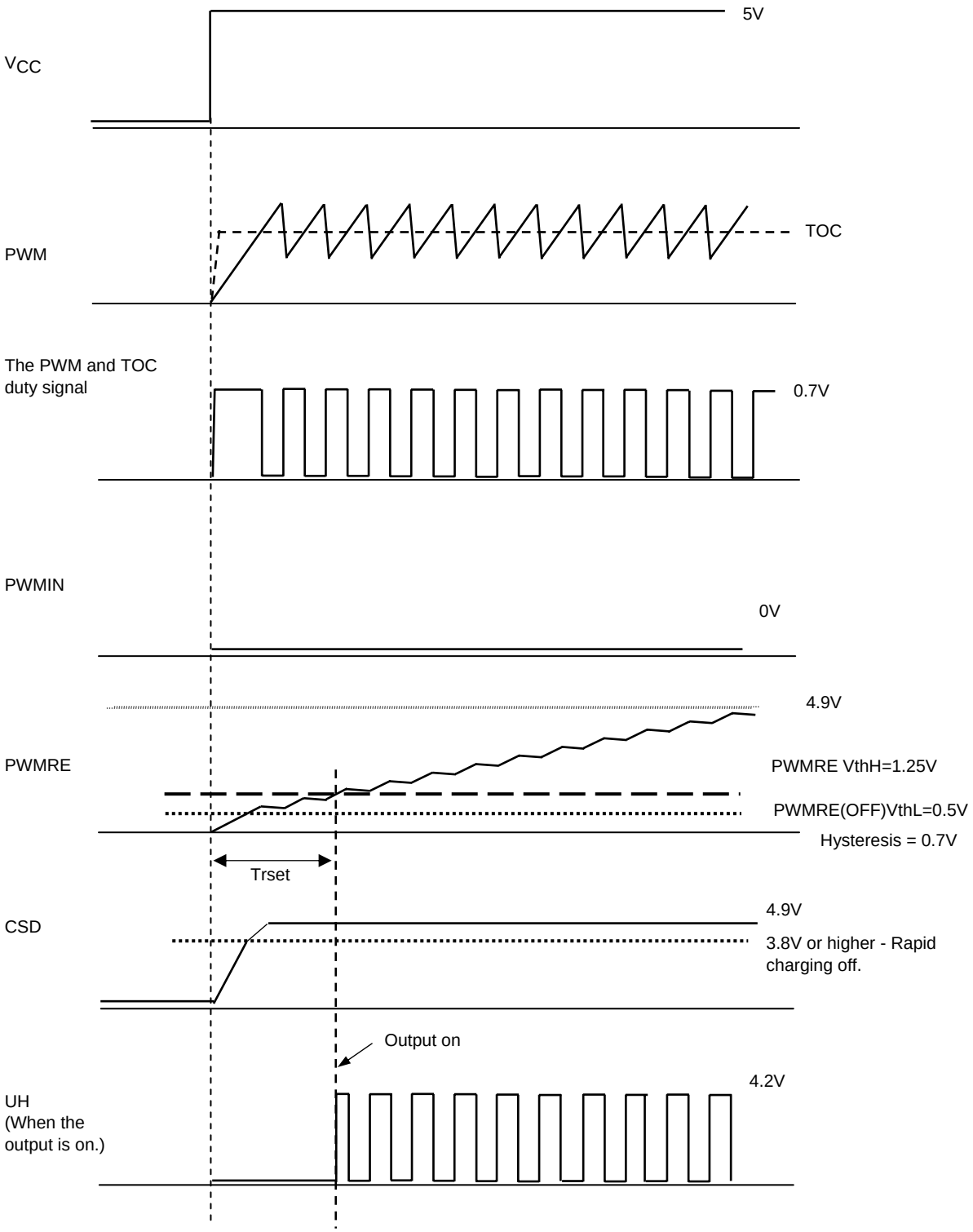
Pin Number	Function	Function	Equivalent circuit
24	V_{CC}	V_{CC} power supply connection.	
25	S/S	Start/stop control. A low level sets the IC to the start state and a high level or open sets it to the stop state.	
26	GND	Ground connection	
27 28	RFGND RF	RFGND: Output current detection circuit comparator reference ground. RF: Output current detection. Insert a resistor with a low resistance between the RF pin and ground. The maximum output current is set to I_{OUT} = 0.24/RF by the resistor RF.	

Timing Charts (Hall input/output, startup, input off state, and constraint protection timing charts)

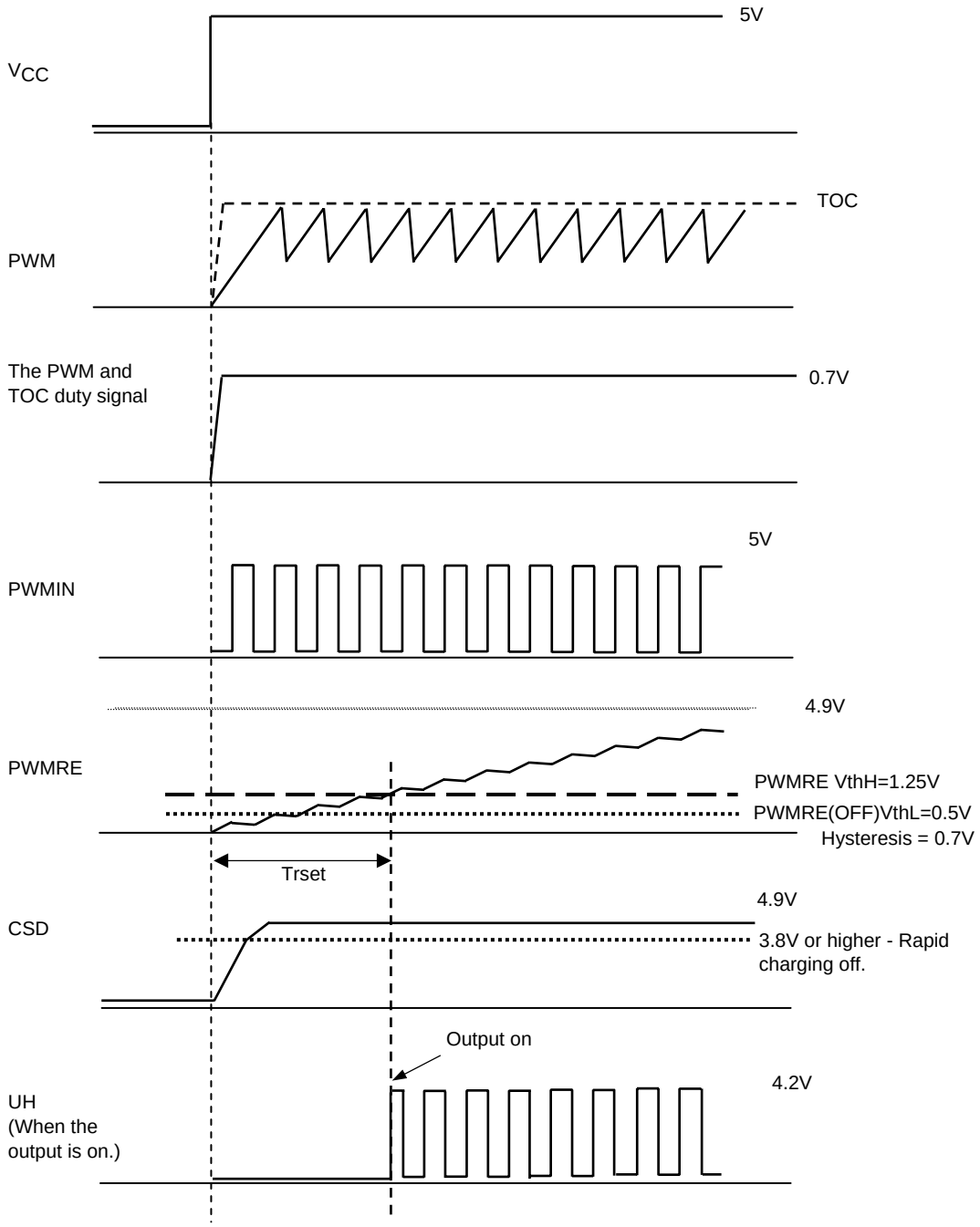


The gray areas indicate PWM output.

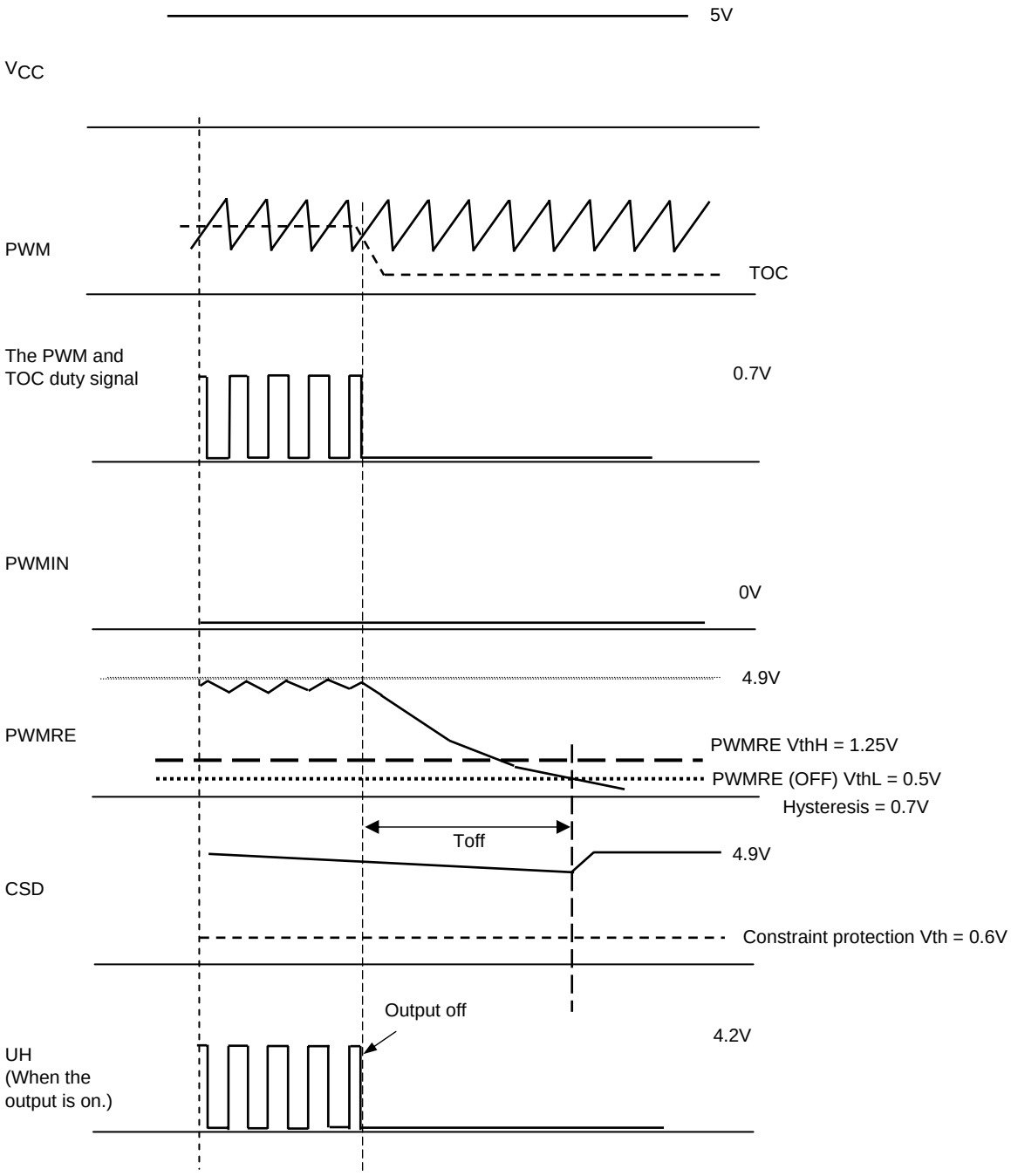
Startup Timing Chart (When a buffered input is provided to CTL+)



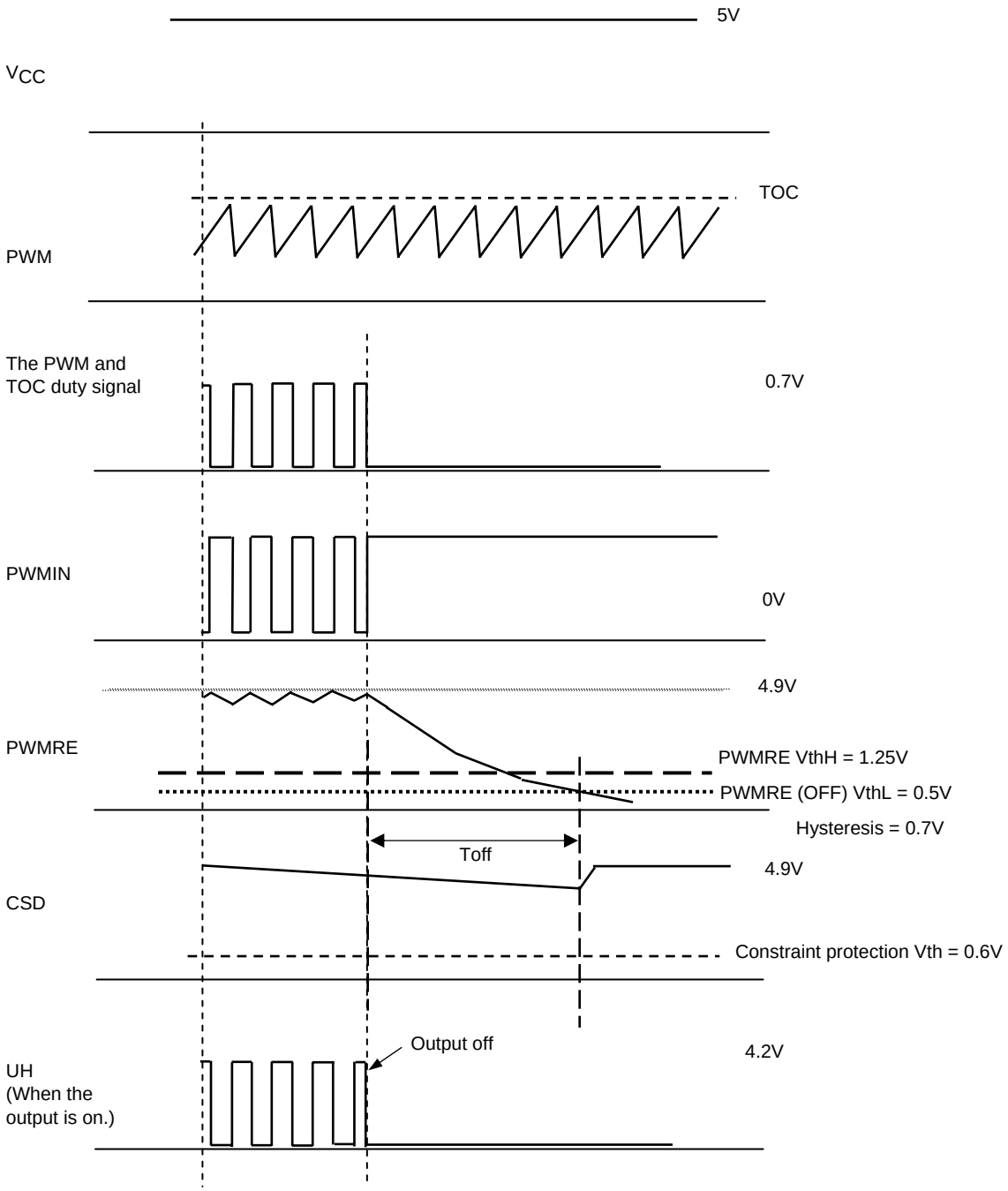
Startup Timing Chart (When the PWMIN input is used)



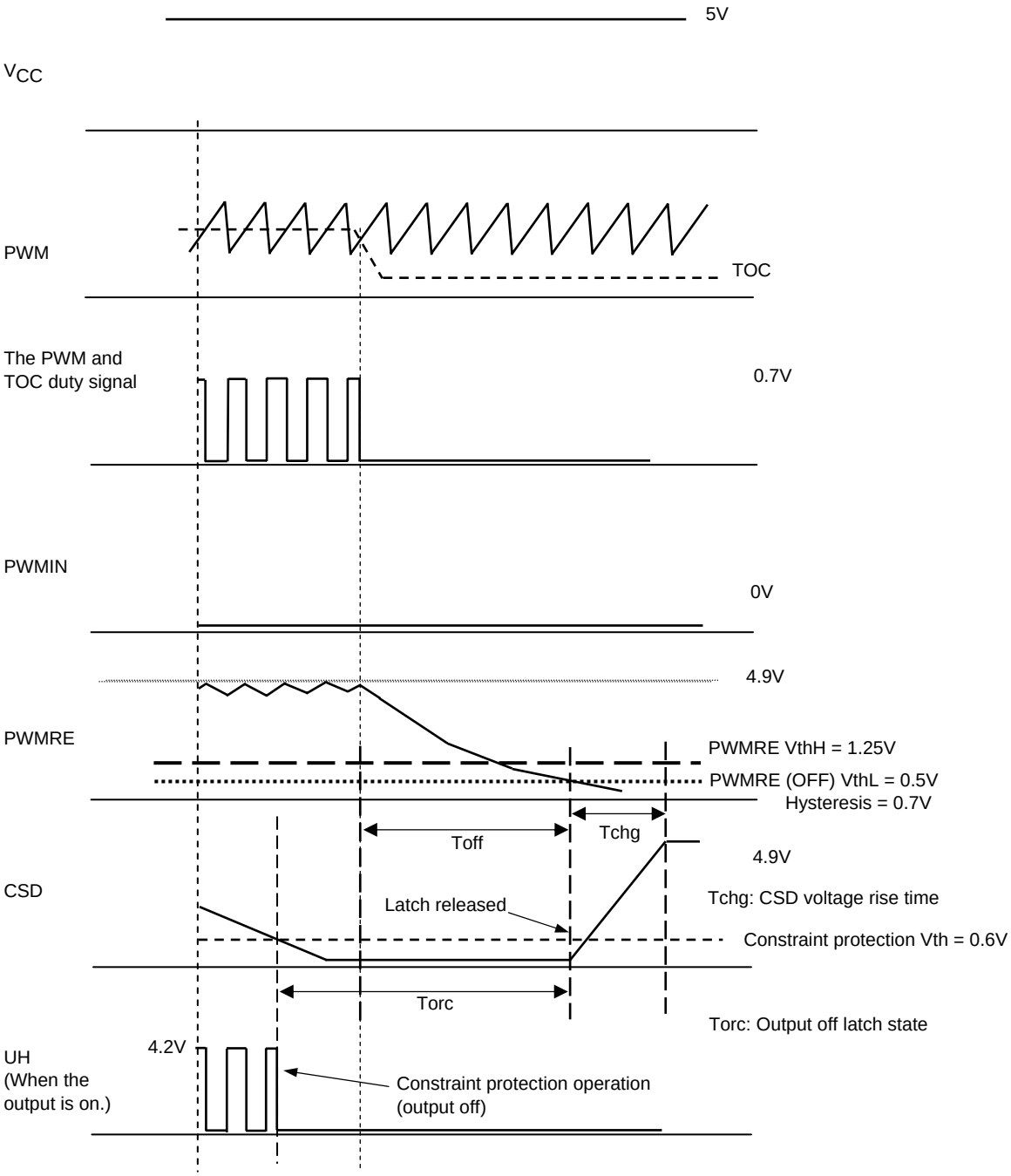
Input Off State (CTL+input) Reset Operation Timing Chart



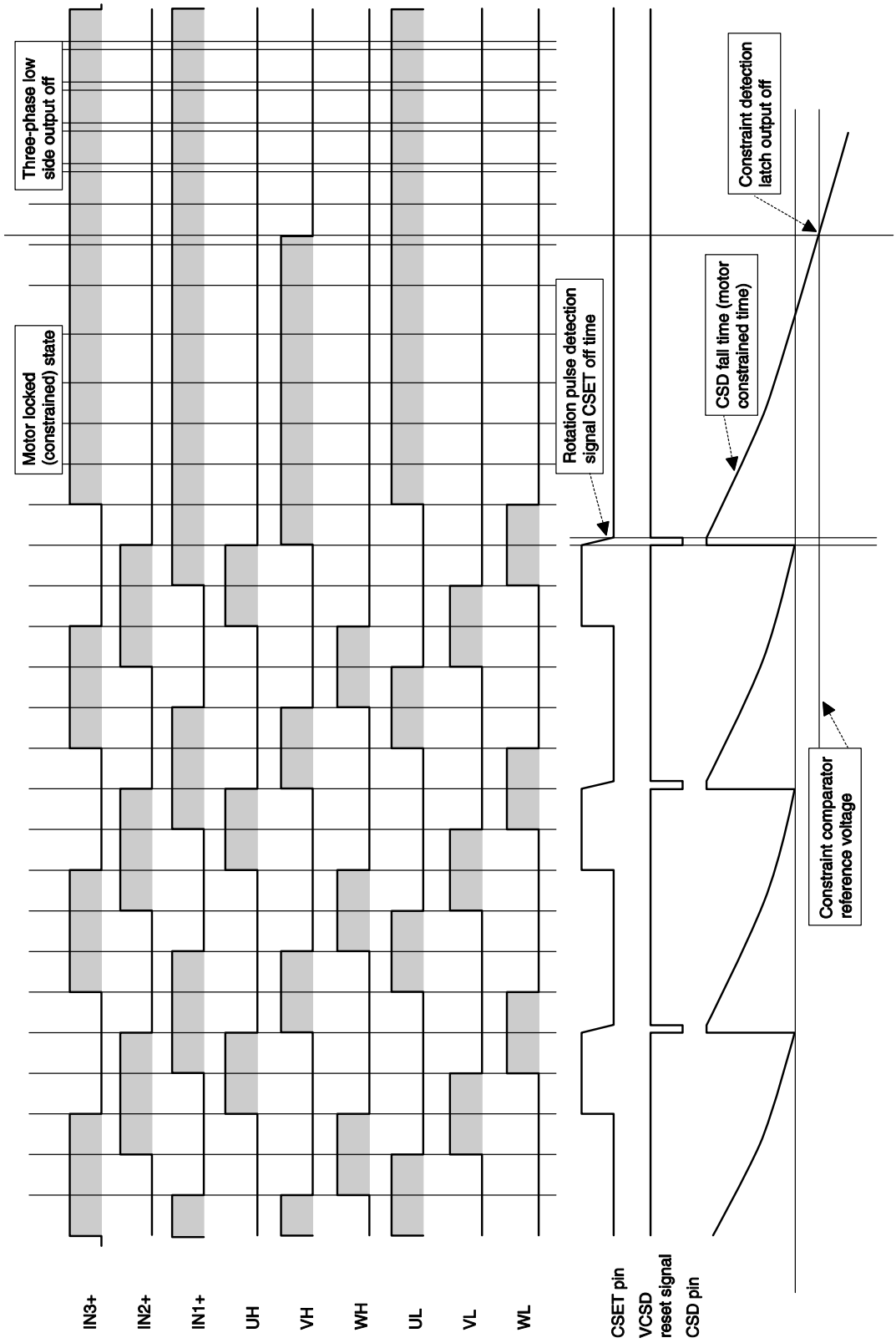
Input Off State (PWMIN input) Reset Operation Timing Chart



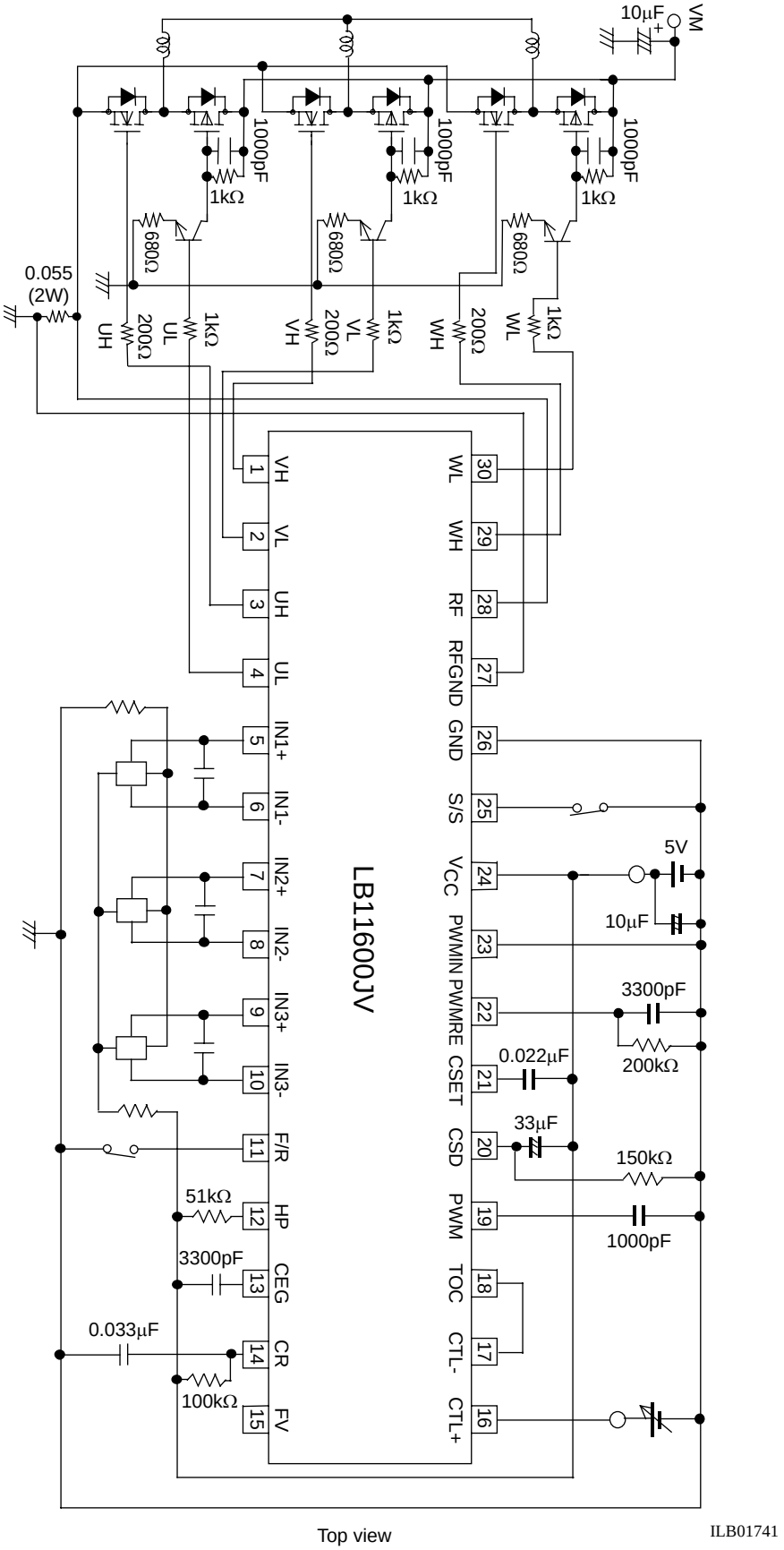
Constraint Protection State Latch Release Timing Chart (CLT+ input)



Constraint Protection Timing Chart



LB11600JV Application Circuit Diagram (FET driver: low side PWM control)



Top view

ILB01741

*: The resistor, capacitor, and transistor values shown are for reference purposes only. The values used in an application will depend on the motor used and the control specifications.

LB11600JV Operation

1. Output Drive Circuit

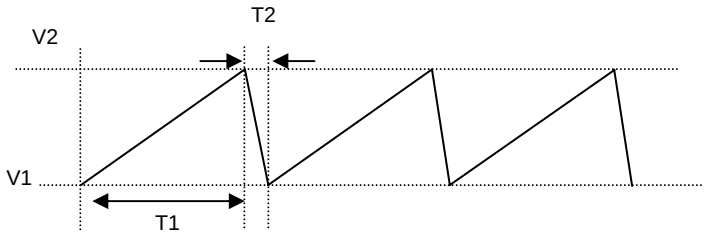
The LB11600JV adopts direct PWM drive to minimize power loss in the output system. The output transistors are always saturated when on and the motor drive power is adjusted by changing the output on duty. Output PWM switching is applied the UH, VH, and WH output side circuits. Since the UL to WL and UH to WH outputs have the same output configuration, either low side PWM or high side PWM drive can be implemented by using appropriate circuit structures with the external output drive transistors. Since the reverse recovery time for the diodes connected to the non-PWM side outputs can be a problem, care is required in selecting these diodes. (If diodes with a short reverse recovery time are not used, through currents will flow at the instant the PWM side transistors are turned on.)
The UL to WL and UH to WH outputs go to the high-impedance state in the stopped state and when the supply voltage is extremely low (i.e. lower than the allowable operating voltage). This means that workarounds (such as pull-down resistors) are required so that leakage currents and other phenomenon do not cause incorrect operation in external circuits.

2. Power Saving Circuit

The LB11600JV goes to a power saving state in which power consumption is reduced when the S/S pin is set to the high level. The power saving state cuts off the bias current from most of the circuits in the IC.

3. Notes on the PWM Frequency

The PWM frequency is set by the capacitance of the capacitor (C) connected to the PWM pin.
The formula for calculating the PWM frequency is shown below.



Formula (When V_{CC} = 5V (typical))

Oscillator period:	T = T1 + T2 (s)
Threshold voltage:	V1 = 0.25 × V_{CC} + 0.0975 = 1.35 (V) V2 = 0.6 × V_{CC} = 3.0V (V)
Charge time:	T1 = C × (V2 - V1)/IC (s)
IC:	Charge current provided by the PWM pin: 45µA
Discharge time:	T2 = - C × Rin × ln (V1/V2) (s)
Rin:	PWM pin internal discharge resistor (2kΩ)
C:	External capacitor
Oscillator frequency:	Fpwm = 1/T (Hz)

If a 1000pF capacitor is used, the oscillator frequency will be about 25kHz. If the PWM frequency is too low, the motor may emit audible switching noise, and if it is too high, power loss in the output circuits will be excessive. We recommend using a frequency in the range 15 to 50kHz. Connect the ground side of the external capacitor as close as possible to the IC GND pin to minimize the influence of output noise and other problems.

4. Notes on PWM Drive Methods

The output duty can be controlled by any of the following methods.

• Control by Comparing the TOC Pin Voltage with the PWM Oscillator Waveform

This method sets the UH, VH, and WH output duty by comparing the TOC pin voltage with the PWM oscillator waveform. When the TOC pin voltage falls below 1.35V (typical), the duty will be 0%, and when it rises above 3.0V (typical), the duty will be 100%. Since the TOC pin is the control amplifier's output pin, it is not possible to directly input a control voltage to the TOC pin. Therefore, the control amplifier is normally used as a buffer amplifier (by connecting the CTL- pin to the TOC pin) and inputting a DC voltage to the CTL+ pin. (This causes the TOC pin voltage to become the same as the CTL+ pin voltage.)

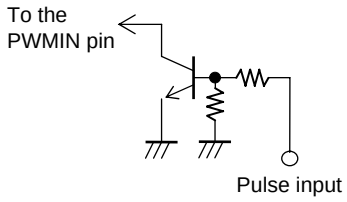
In this case, the output duty will increase as the CTL+ pin voltage becomes higher. Since the motor will be driven if the CTL+ pin is in the open state, a pull-down resistor must be connected to the CTL+ pin if it is not desirable to drive the motor when the input is in the open state.

If the CTL+ pin is used for motor control, set the PWMIN pin to the low level or short it to ground.

• Pulse Control Using the PWMIN Pin

A pulse input can be applied to the PWMIN pin and the duty of that signal used to control the output.

When a low-level input voltage is applied to the PWMIN pin the output will be on, and when a high-level input voltage is applied the output will be off. When the PWMIN pin is open, it goes to the high level and the output will be turned off. If the inverse input logic is required, use an external npn transistor as shown in the figure.



If the PWMIN pin is used for control, connect the CTL- pin to ground and connect the CTL- pin to the TOC pin.

A 1000pF capacitor must be connected to the PWM pin even when the PWMIN pin is used for control.

• PWMRE Pin Input Pulse Reset

To prevent incorrect operation of the constraint protection circuit when the V_{CC} power supply is started or when the motor is stopped (the constraint protection circuit will operate immediately if the CSD pin potential is low), that is to assure that the CSD pin is set to the high-level voltage reliably (by assuring the capacitor charge time), a reset period (outputs off, the rapid charge time for the CSD pin) is set up by a resistor and capacitor connected to the PWMRE pin. When the motor is controlled by either the CTL+ pin or by pulses input to the PWMIN pin, output to the motor is not provided immediately. Rather the output remains in the off state (the reset period) until the charge/discharge potential due to the on/off operation set by the input pulse duty width, the PWMRE pin charge current, and the capacitor and resistor connected to the PWMRE pin rises above 1.25V (typical). The IC enters operating mode when the PWMRE potential is over 1.25V (typical), and the output goes to the off state (reset state) when the PWMRE potential falls below 0.55V (typical) in the input pulse off state.

The IC operates with the outputs on (UH, VH, and WH), when the PWMRE potential is over 1.25V (typical) and the CSD pin potential is over $0.76 \times V_{CC}$ (3.8V typical when V_{CC} = 5V).

See the timing chart for startup and the input off state.

The formula for setting the reset time (Trest) and the timing charts are shown on the following pages.

<Reset time (Trest f) due to the PWMRE pin (PWMIN input mode) when V_{CC} = 5V>

The rise potential (V1) and the fall potential (V2) due to the on/off duty ratio when a PWMIN input is used:

When on:	$V1 = (V0 - Ipwmre \times R) \times e^{-t1/RC} + Ipwmre \times R$
When off:	$V2 = V1 \times e^{-t2/RC} = \Delta V$
Ipwmre:	PWMRE pin charge current: 200µA (typical)
V0:	PWMRE initial potential: 0V
C:	PWMRE pin external capacitor
R:	PWMRE pin external resistor
t1:	PWMIN input duty on time
t2:	PWMIN input duty off time

The time (n times the PWMIN period) required for the potential, which is increased by the V2 potential difference (ΔV) on each input pulse, to exceed the threshold voltage (Vth = 1.25V) is the reset period (Trest).

$V2 + \Delta V + \Delta V \cdots \geq 1.25V$

$Trest \leq TPWMIN \times n$ (s)

<PWMRE Reset Time Setting Example>

V_{CC} = 5V, PWMIN = 25kHz, on duty ratio = 20%

PWMRE: C = 2200pF, R = 180kΩ

PWMIN = 25kHz = 40μs

$t1 = 40\mu s \times 0.2 = 8\mu s$ $t2 = 40\mu s \times 0.8 = 32\mu s$

$V1 = (V0 - Ipwmre \times R) \times e^{-t1/RC} + Ipwmre \times R$

$= (0 - 200\mu A \times 180k\Omega) \times 0.98 + (200\mu A \times 180k\Omega)$

$= -35.28 + 36 = 0.72$ (V)

$V2 = V1 \times e^{-t2/RC}$

$= 0.72 \times 0.922 = 0.664$ (V)

Since ΔV (0.644) is added on each PWMIN input pulse, and

$V2 + \Delta V = 0.664 + 0.664 \geq 1.25V$

the threshold voltage (1.25V) will be exceeded on the second pulse.

From the formula for the on time: $t1' = CR \times \ln((V0 - Ipwmre \times R)/(V1 - Ipwmre \times R))$

Since the potential difference with respect to 1.25V due to the rise potential V2 of the second PWMIN pulse is 1.25 - 0.664 = 0.586V, 1.25V will be exceeded in the on duty state. Therefore,

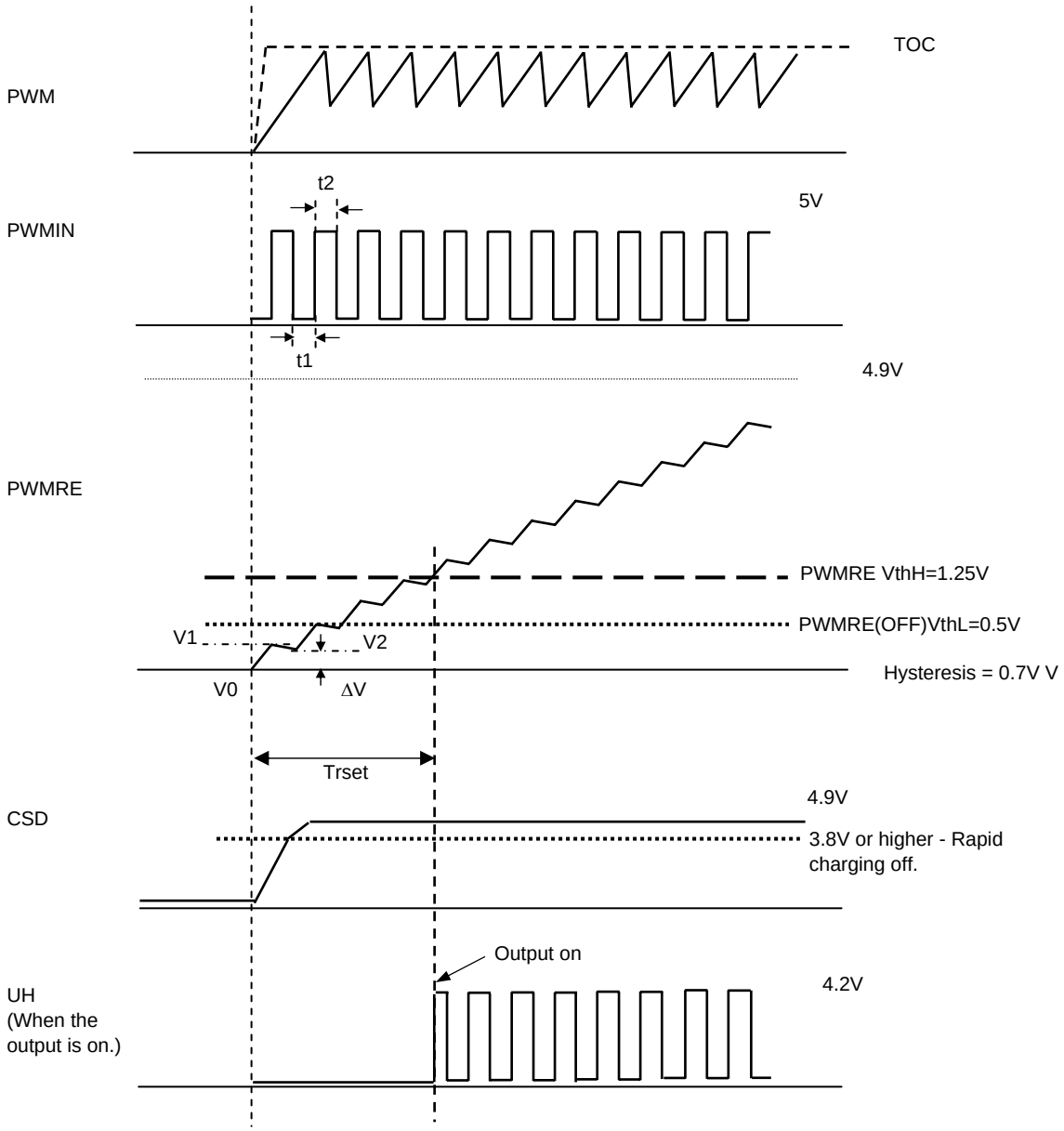
$t1' = 2200pF \times 180k\Omega \times \ln((0.664 - 200\mu A \times 180k\Omega) / (1.25 - 200\mu A \times 180k\Omega))$

$= 396\mu s \times \ln(35.336/34.75) = 6.622\mu s$ (s)

Thus the reset time Trest will be one PWMIN period plus t1'.

$Trest = 40\mu s + 6.622\mu s = 46.622\mu s$ (s)

PWMRE Timing Chart for PWMIN Pin Input



<Reset time (Trest f) due to the PWMRE pin (CTL+ buffer input mode) when V_{CC} = 5V>

1. CTL+ input mode (When the TOC potential is higher than the PWM triangle wave rise)

The rise potential (V1) and fall potential (V2) due to the on/off duty due to the TOC potential and the PWM triangle wave

When on: $V1 = (V0 - Ipwmre \times R) \times e^{-t1/RC} + Ipwmre \times R$

When off: $V2 = V1 \times e^{-t2/RC}$

When the TOC potential rises and the PWM triangle wave rise is slow, the IC will be in the ON duty state at startup. This results in the time Tpwmra, which is the time until the PWM triangle wave low level is reached.

The potential difference due to each input pulse is: $\Delta V = V2 - Vpwmra$.

$Vpwmra = (Ipwm \times Tpwmra) / Cpwm$

Ipwm: PWM pin charge current: 45µA (typical)

Cpwm: Capacitance of the PWM pin external capacitor

Ipwmre: PWMRE pin charge current: 200µA (typical)

V0: PWMRE pin initial potential: 0 V

C: Capacitance of the PWMRE pin external capacitor

R: Resistance of the PWMRE pin external resistor

t1: PWMIN pin input duty on time

t2: PWMIN pin input duty off time

The time (n times the PWMIN period) required for the potential, which is increased by the V2 potential difference (ΩV) on each input pulse, to exceed the threshold voltage (Vth = 1.25V) is the reset period (Trest).

$V2 + \Delta V + \Delta V \cdots \geq 1.25V$

$Trest \leq TPWMIN \times n + Tpwmra$ (s)

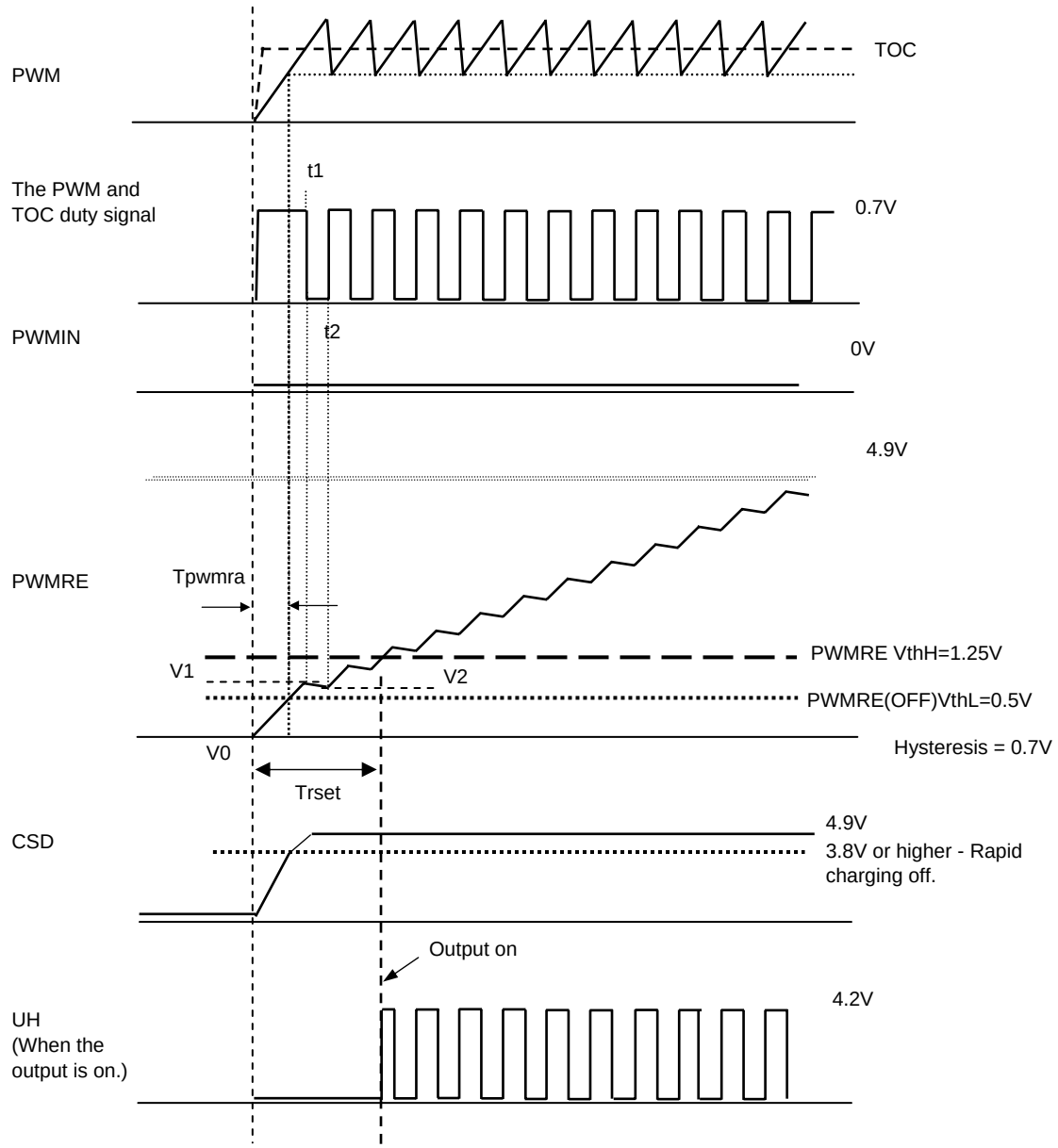
2. CTL+ input mode (When the TOC potential rises after the PWM triangle wave rises)

The time required for the sum of the potentials due to the times set for each on/off duty ratio for the rise time to exceed the threshold voltage (1.25V) becomes the reset time (Trest).

The times t1 and t2 for the rise potential (V1) and fall potential (V2) due to each on duty ratio will differ. Thus these must be calculated individually for each input pulse signal. The formulas for calculating V1 and V2 are the same as for the PWMIN input case.

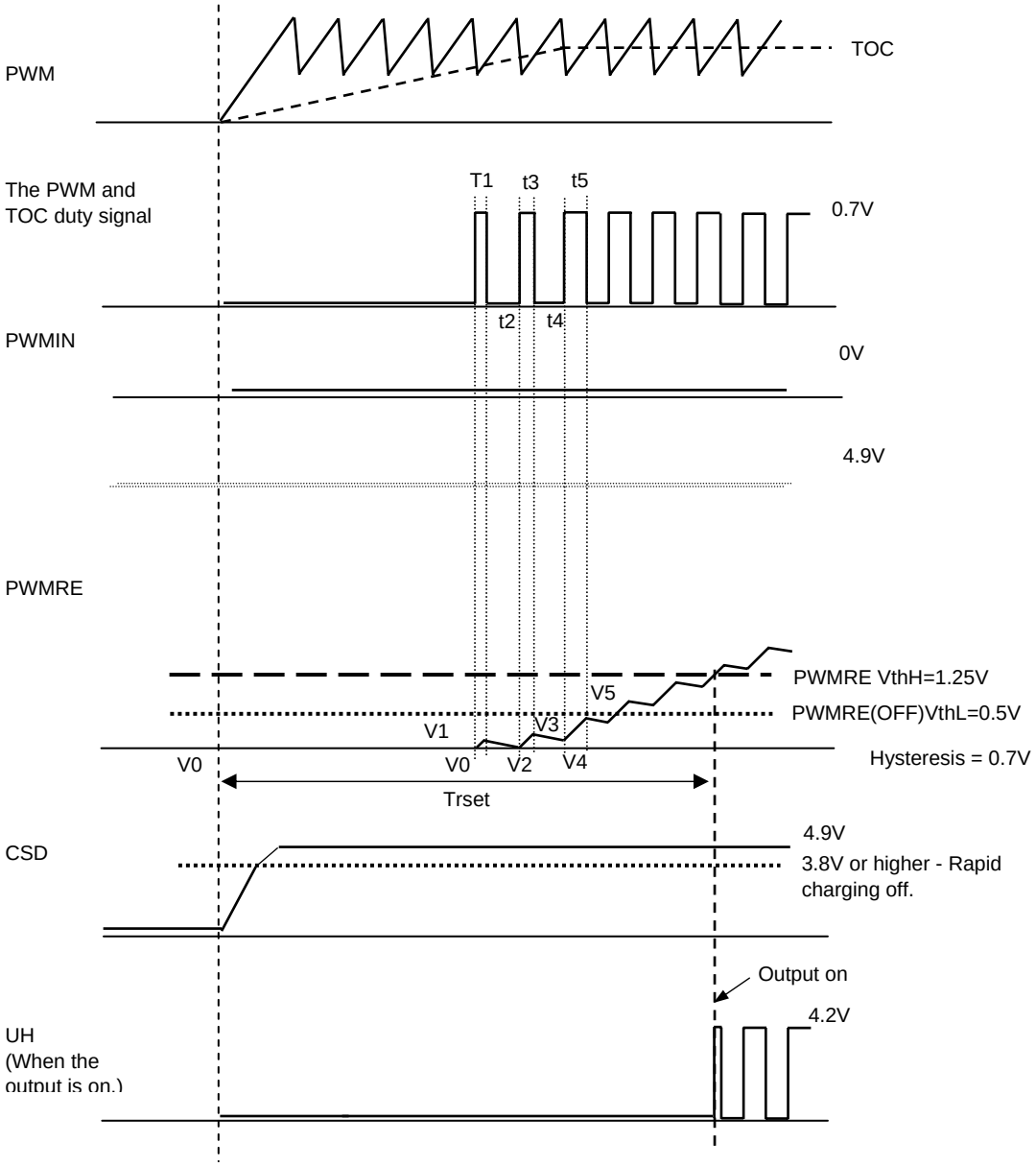
PWMRE Timing Chart for CTL+ Buffered Input

(1) CTL+ input mode (When the TOC potential is high due to the rise of the PWM triangle wave)



PWMRE Timing Chart for CTL+ Buffered Input

(2) CTL+ input mode (When the TOC potential rises after the rise of the PWM triangle wave)



5. Hall Input Signals

The Hall effect sensor inputs require input signals with an amplitude larger than the hysteresis (80mV maximum) and an even larger amplitude is desirable to avoid problems due to noise, phase displacement, and other issues. If disturbances to the output waveforms (at phase switching) or HP output occur due to noise, the disturbances must be prevented by inserting capacitors across the inputs or by other means. The Hall inputs are used as input discrimination signals to the constraint protection circuit and the one-shot multivibrator circuit. Although these circuits are designed to tolerate a certain amount of noise, care is required if these protection circuits are used. If all three phases of the Hall input signals go to the same state, all of the outputs will be turned off (all of the UL, VL, WL, UH, VH, and WH outputs will go to the low level potential).

If the outputs from a Hall IC are used for these inputs, tying one side of the inputs (either the + or - side) to a voltage within the common-mode input range for when Hall sensors are used allows the other side of the input to be used with an input in the 0 to V_{CC} range.

6. Undervoltage Protection Circuit

This IC starts up (output operation turns on) at a V_{CC} voltage of 4.3V (typical) and turns the outputs off (sets the UH, VH, and WH outputs to the low level potential) when the V_{CC} voltage falls to under 3.8V(typical).

7. Constraint Protection Circuit

The LB11600JV includes a constraint protection circuit to protect the motor and the IC itself when the motor is physically prevented from turning. If the Hall input signals do not change for a certain fixed period when the IC is operating in the motor drive state, one side of the output system (the UH, VH, and WH outputs) is turned off. The time is set by the discharge time of the resistor and capacitor connected to the CSD pin. (See the constraint protection circuit timing chart.)

The motor rotation pulse detection signal is detected with the timing of the fall (high to low) of the UH output signal, one of the three output phases. The rotation pulse detection signal time is set by the discharge time for the CSET pin capacitor. During motor rotation, the CSD pin potential will always be high during the rotation pulse detection time. If the motor becomes constrained (stopped), the CSD potential is discharged and the outputs (UH, VH, and WH) are set low when the CSP potential falls under 0.6V.

After the constraint protection circuit operates, the outputs will be latched in the low state. To clear this latched state, set either PWMIN or S/S to the high level.

The latched state is cleared when the PWMRE potential falls below 0.55V (typical) and the IC enters the reset state. (See the latch clear timing chart.)

Note that if the CSD pin resistor Rc is too large, the CSD pin potential may rise due to the bias current from the internal comparator circuit.

Rotation pulse detection signal time: $Tps = Cs \times VBE / Icset$ (s)

- Cs: CSET pin external capacitor (connected between VCC and CSET)
- VBE: VBE for the transistor in the constraint protection circuit: 0.7V (typical)
- Lcset: CSET pin discharge current: 50µA (typical)

Motor constraint time: $Tcsd = \ln (V_{CC} / (0.6 - Ibcd \times Rc) \times Cc \times Rc$ (s)

- Cc: CSD pin external capacitor (connected between V_{CC} and CSD)
- Rc: CSD pin external resistor (connected between the CSD pin and ground)
- Ibcd: CSD pin internal comparator bias current: 1µA (typical)
- CSD pin discharge potential threshold voltage: 0.6V (typical)

Latch release time: $Toff = \ln (V_{CC} / 0.55) \times Cre \times Rre$ (s)

- Cre: PWMRE pin external capacitor (connected between the PWMRE pin and ground)
- Rre: PWMRE pin external resistor (connected between the PWMRE pin and ground)

CSD potential rise time (rapid charging time): $Tchg \approx Cc \times Rc \times \ln ((V1 - Ic \times Rc) / (V2 - Ic \times Rc))$ (s)

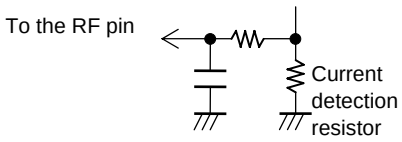
- Cc: CSD pin external capacitor (connected between V_{CC} and CSD)
- Rc: CSD pin external resistor (connected between the CSD pin and ground)
- Ic: CSD pin transistor current (7mA maximum (design target value))
- V1: CSD pin initial voltage
- V2: CSD pin voltage (when the transistor is in the on state): 4.9V (typical)

CSD voltage rise time (during motor rotation): Tchg ≈ Cc × Rc × ln((V1 - Ic × Rc) / (V2 - Ic × Rc)) (s)

- Cc: CSD pin external capacitor (connected between V_{CC} and CSD)
- Rc: CSD pin external resistor (connected between the CSD pin and ground)
- Ic: CSD pin transistor current (3.5mA maximum (design target value))
- V1: CSD pin initial voltage
- V2: CSD pin voltage (when the transistor is in the on state): 4.9V (typical)

<Constraint Time Setting Example>
When V_{CC} = 5V, to set the motor constraint time to 3 seconds:
Use a 10μF capacitor for the CSD pin capacitor Cc and a 130kΩ resistor for Rc.
Motor constraint time: Tcsd = 1n (5 / (0.6 – 130kΩ × 1μA) × 10μF × 130kΩ
= 2.36 × 10μF × 130kΩ = 3.068 (s)
The discharge time for the capacitor specified above will be the motor constraint time.
The pulse signal that detects whether or not the motor is turning is set by the CSET pin capacitor.
If a 0.022 μF capacitor is used as the CSET pin capacitor Cs:
Rotation pulse signal detection time: Tps = 0.022μF × 0.7/50μA = 308μs
Note that care is required in setting these values since the amplitude of the rotation pulse detection signal is influenced by the motor speed, and the CSD capacitance.
If the rotation pulse detection signal time is too short, the IC will not be able to raise the CSD potential to the high level. Also, if the CSD pin capacitor value is too small and the discharge time too short, the rotation detection pulse signal will not be issued for the motor rotation period at the start of motor rotation (when the motor is turning slowly), and the constraint protection circuit may latch. For example, since at speeds under 100rpm the UH output period will be 300ms, the motor constraint time must be set to a time of at least 600ms.

8. Overcurrent Protection Circuit



The overcurrent protection circuit limits the output current to be a maximum of I = VRF/Rf (where VRF = 0.24V typical, and RF is the current detection resistor). The current limiter circuit detects the reverse recovery current in the output diodes due to PWM operation and includes a built-in filter circuit to prevent incorrect operation. While this internal filter circuit is adequate for most applications, if the circuit is observed to operate incorrectly (for example, in cases where the diode reverse recovery current flows for over 3 μs), an external filter circuit (such as a passive low-pass filter circuit) must be added.

9. Thermal Protection Circuit

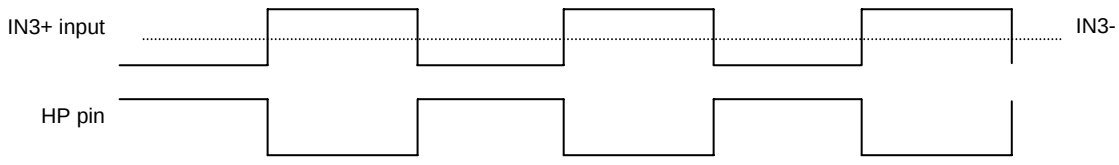
The thermal protection circuit turns off one side of the output (UH, VH, and WH) if the IC junction temperature (Tj) exceeds the stipulated temperature (TSD = 170°C, typical).

10. Direction Reversal

Do not reverse motor direction while the motor is turning. To reverse directions, first stop the motor (set PWMIN high or set the S/S pin high) and then startup again with the desired direction.

11. HP Output

The Hall signal created from the IN3 pin Hall amplifier input signal is inverted and output from the HP pin. Since the HP pin is an open-collector output, a pull-up resistor must be inserted between V_{CC} and the HP pin.
Hall amplifier input conditions: IN3-: fixed potential, HP pin: pulled up to V_{CC}.



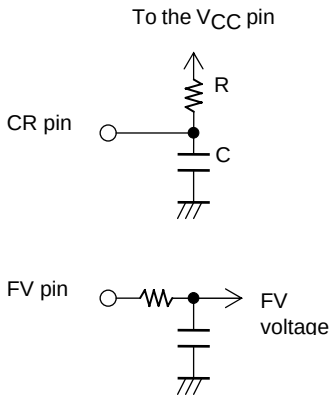
12. One-Shot Multivibrator Circuit Block (CEG, CR, and FV pins)

The LB11600JV includes a built-in one-shot multivibrator circuit to allow it to support speed feedback control. The signal used for speed control is a rotation pulse detection signal that is created in the CEG pin circuit block with the timing of the fall (high to low) of the UH output signal, one of the three output phases. The LB11600JV detects the rotation period from this signal. The rotation pulse detection signal time is set by the discharge time of the capacitor connected to the CEG pin.

Rotation pulse detection signal time: Tps = Ce × VBE/Iceg (s)

Ce:	CEG pin external capacitor (connected between V_{CC} and CEG)
VBE:	VBE for the transistor in the CEG edge detection circuit: 0.7V (typical)
Iceg:	CSET pin discharge current: 50μA (typical)

The CR pin sets the pulse width (high period) generated at the FV pin at each signal from the CEG pin.



The pulse width is set by connecting a resistor and a capacitor between the CR pin and V_{CC} and ground, respectively.
The pulse width TRC can be calculated approximately with the following formula.

$TRC \approx 1.1 \times R \times C$ (s)

Normally, a smoothing circuit consisting of a resistor and capacitor as shown in the figure is connected to the FV pin. A resistor with a value of at least 25kΩ must be selected. The value of the capacitor must be selected so that adequate smoothing of the FV voltage is provided when the motor speed is low.
Normally, this circuit is set up so that the following relationship holds when fUH (Hz) is the UH output frequency at the highest motor speed.

$TRC \leq 1/(2 \times fUH)$ (s)

In this case, the FV voltage will change from 0 to about 5V according to the motor speed.
If the FV output is not used, connect the CR pin to ground and leave the FV pin open.

13. Power Supply Stabilization

Since the LB11600JV adopts a switching-based drive method, the power supply line level is easily disturbed. Therefore it is necessary to connect a capacitor with adequate capacitance to stabilize the power supply between the V_{CC} pin and ground.
If diodes are inserted in the power supply lines to prevent damage if the power supply is inadvertently connected with reverse polarity, the power supply line will be even more sensitive to disruption. Here, an even larger capacitance must be provided.
If the switch and the capacitor are widely separated when the power supply is turned on and off, such as during switching, the supply voltage may swing widely due to the surge current between the line inductance and the capacitor. Voltages that exceed the LB11600JV's voltage handling capacity may occur. In applications such as this, do not use components, such as ceramic capacitors, which have a low capacitor series impedance, but rather use electrolytic capacitors and implement measures to minimize the surge current and prevent voltage increases.

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