

# NUP2114UPXV5

## Transient Voltage Suppressors

### Low Capacitance ESD Protection for High Speed Data

The NUP2114UPXV5 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra-low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 applications.

#### Features

- Low Capacitance 0.8 pF
- Stand Off Voltage: 5 V
- Low Leakage
- Protection for the Following IEC Standards:  
IEC 61000-4-2 Level 4 ESD Protection
- UL Flammability Rating of 94 V-0
- This is a Pb-Free Device

#### Typical Applications

- High Speed Communication Line Protection
- USB 2.0 High Speed Data Line and Power Line Protection
- Monitors and Flat Panel Displays
- MP3
- Gigabit Ethernet
- Notebook Computers
- Digital Video Interface (DVI) and HDMI

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

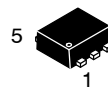
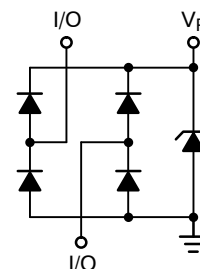
Rating	Symbol	Value	Unit
Operating Junction Temperature Range	$T_J$	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{\text{stg}}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature - Maximum (10 Seconds)	$T_L$	260	$^\circ\text{C}$
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact (ESD)	ESD	16000 400 13000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability. See Application Note AND8308/D for further description of survivability specs.



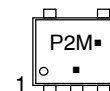
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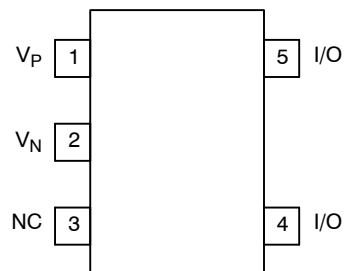
SOT-553  
CASE 463B

#### MARKING DIAGRAM



P2 = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### PIN CONNECTIONS



#### ORDERING INFORMATION

Device	Package	Shipping
NUP2114UPXV5T1G	SOT-553 (Pb-Free)	4000/Tape & Reel

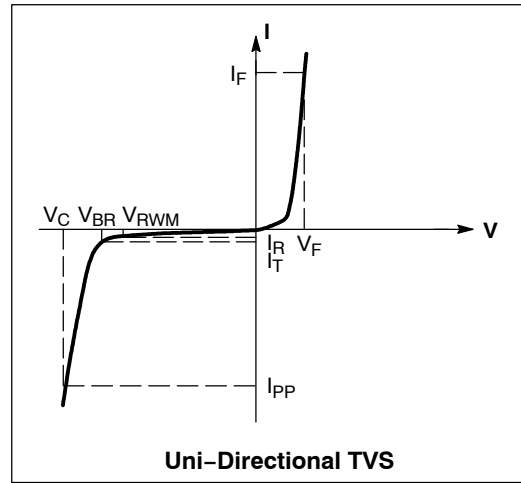
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NUP2114UPXV5

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz

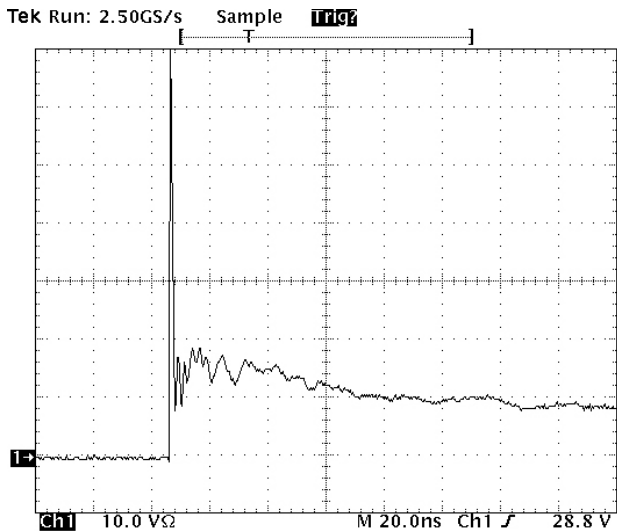


\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

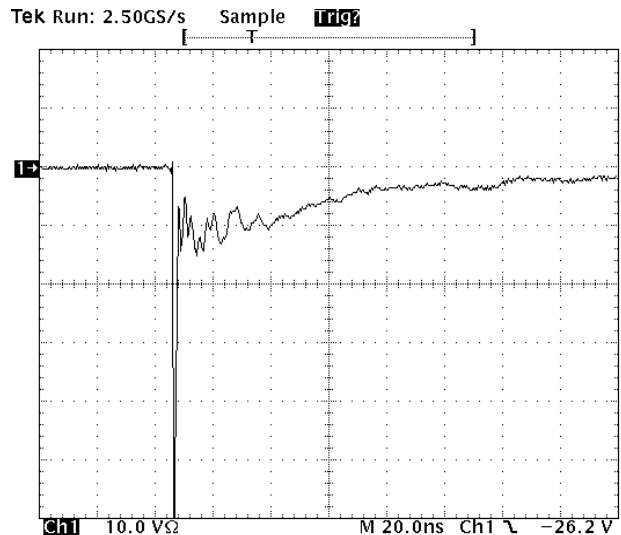
## ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	(Note 1)			5.0	V
Breakdown Voltage	$V_{BR}$	$I_T = 1$ mA, (Note 2)	6.0			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5$ V			1.0	$\mu\text{A}$
Junction Capacitance	$C_J$	$V_R = 0$ V, $f = 1$ MHz between I/O Pins and GND		0.8	1.0	pF
Junction Capacitance	$C_J$	$V_R = 0$ V, $f = 1$ MHz between I/O Pins		0.4	0.5	pF
Clamping Voltage	$V_C$	@ $I_{PP} = 1$ A (Note 3)			9.1	V
Clamping Voltage	$V_C$	Per IEC 61000-4-2 (Note 4)	Figures 1 and 2			V

- TVS devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
- $V_{BR}$  is measured at pulse test current  $I_T$ .
- Surge current waveform per Figure 5.
- Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.



**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2**



**Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2**

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## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

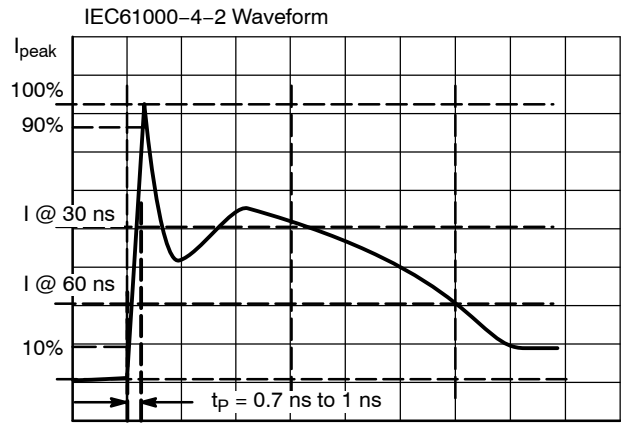


Figure 3. IEC61000-4-2 Spec

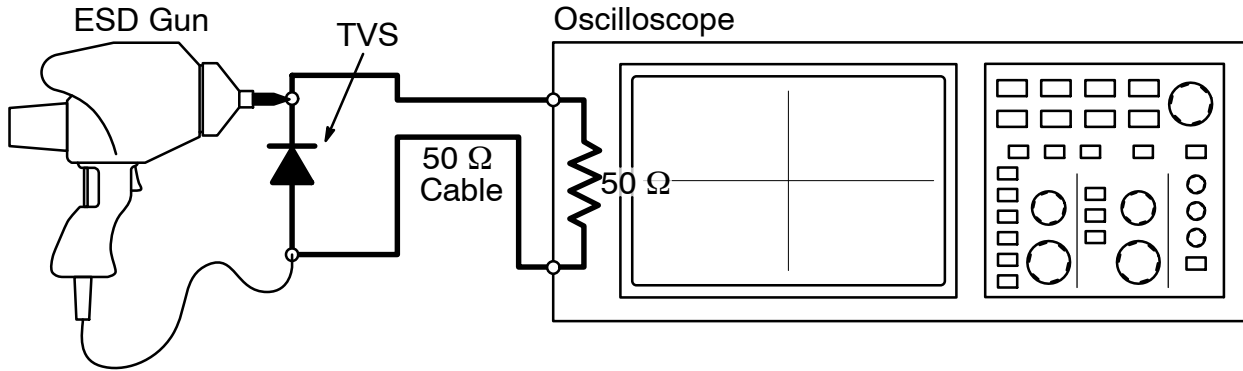


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

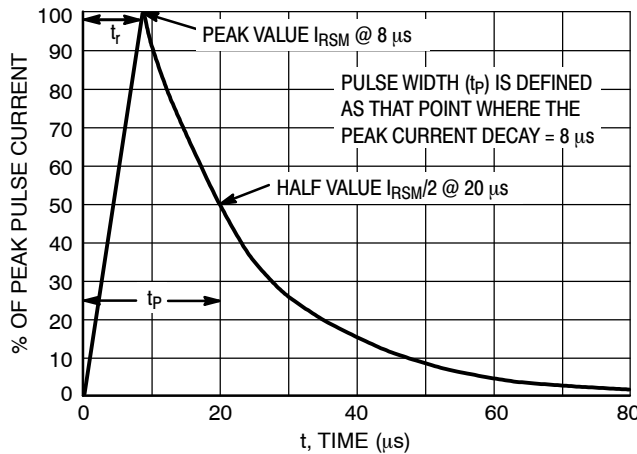
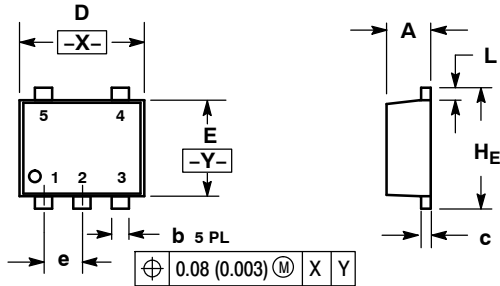


Figure 5. 8 X 20 μs Pulse Waveform

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## PACKAGE DIMENSIONS

### SOT-553, 6 LEAD CASE 463B-01 ISSUE B

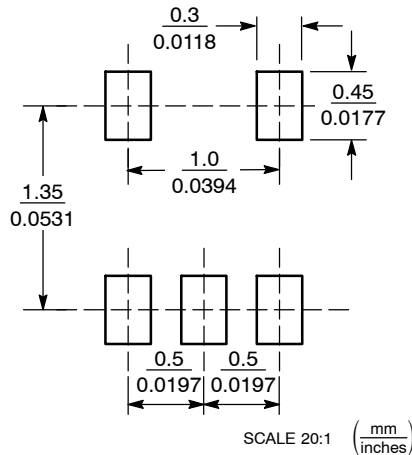


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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