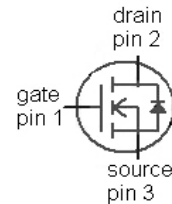


**OptiMOS®3 Power-Transistor**
**Features**

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC<sup>1)</sup> for target applications
- N-channel, logic level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Avalanche rated
- Pb-free plating; RoHS compliant

**Product Summary**

$V_{DS}$	30	V
$R_{DS(on),max}$	3.9	mΩ
$I_D$	50	A



Type	IPF039N03L G	IPU039N03L G
<b>Package</b>	PG-TO252-3-23	PG-TO251-3-21
<b>Marking</b>	039N03L	039N03L

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	50	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	50	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	50	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	50	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	350	
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	50	
Avalanche energy, single pulse	$E_{AS}$	$I_D=50\text{ A}, R_{GS}=25\text{ Ω}$	115	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=50\text{ A}, V_{DS}=24\text{ V}, di/dt=200\text{ A}/\mu\text{s}, T_{j,max}=175\text{ °C}$	6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$		$\pm 20$	V

<sup>1)</sup> J-STD20 and JESD22

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	94	W
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

#### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$		-	-	1.6	K/W
SMD version, device on PCB	$R_{\text{thJA}}$	minimal footprint	-	-	75	
		6 cm <sup>2</sup> cooling area <sup>4)</sup>	-	-	50	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\text{ }\mu\text{A}$	1	-	2.2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance <sup>5)</sup>	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=30\text{ A}$	-	4.2	5.2	$\text{m}\Omega$
		$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=30\text{ A}$	-	3.3	3.9	
Gate resistance	$R_{\text{G}}$		-	1.6	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=30\text{ A}$	48	96	-	S

<sup>2)</sup> See figure 3 for more detailed information

<sup>3)</sup> See figure 13 for more detailed information

<sup>4)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>5)</sup> Measured from drain tab to source pin

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	4000	5300	pF
Output capacitance	$C_{oss}$		-	1400	1900	
Reverse transfer capacitance	$C_{rss}$		-	81	120	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_G=1.6\ \Omega$	-	9	-	ns
Rise time	$t_r$		-	7	-	
Turn-off delay time	$t_{d(off)}$		-	35	-	
Fall time	$t_f$		-	5	-	

**Gate Charge Characteristics<sup>6)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	12	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.3	-	
Gate to drain charge	$Q_{gd}$		-	5.6	-	
Switching charge	$Q_{sw}$		-	11	-	
Gate charge total	$Q_g$		-	25	-	
Gate plateau voltage	$V_{plateau}$		-	2.9	-	
Gate charge total	$Q_g$	$V_{DD}=15\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	51	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	22	-	
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	37	-	

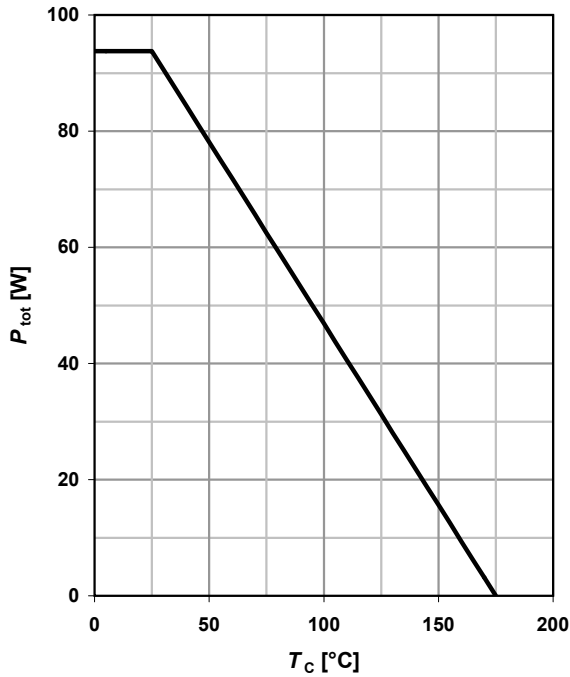
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	350	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.85	1.1	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	20	nC

<sup>6)</sup> See figure 16 for gate charge parameter definition

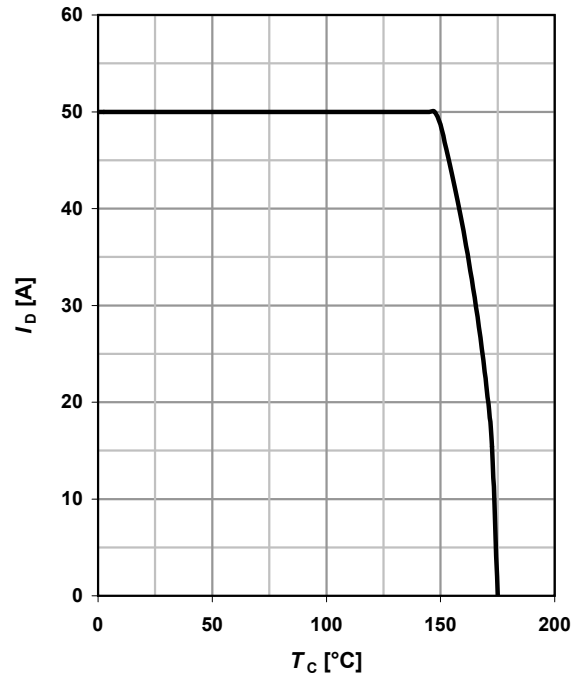
**1 Power dissipation**

$$P_{tot} = f(T_C)$$



**2 Drain current**

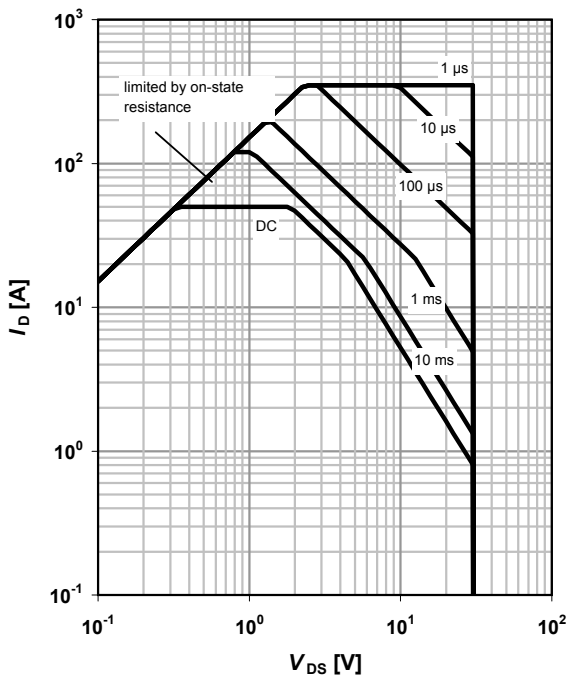
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

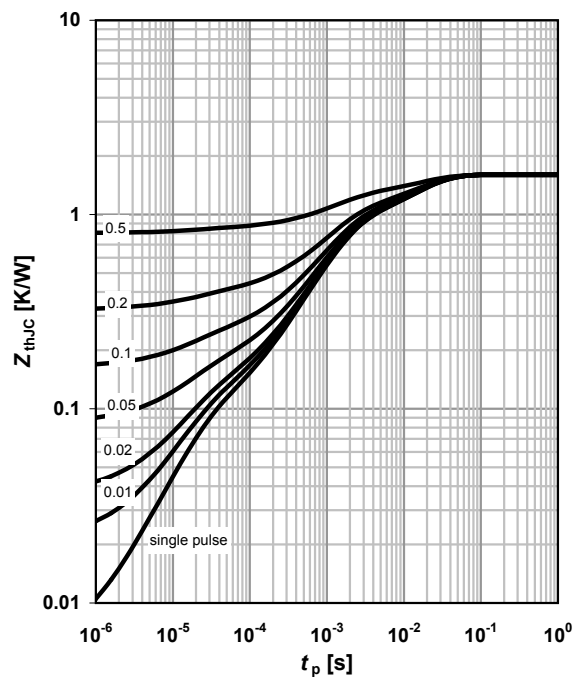
parameter:  $t_p$



**4 Max. transient thermal impedance**

$$Z_{thJC} = f(t_p)$$

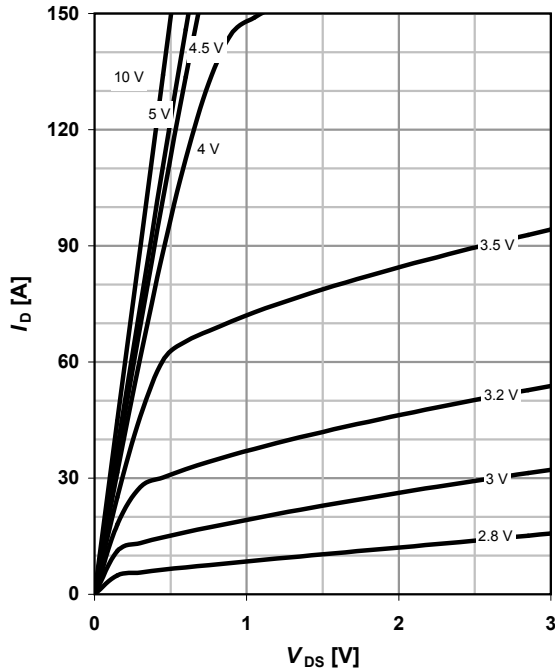
parameter:  $D = t_p / T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

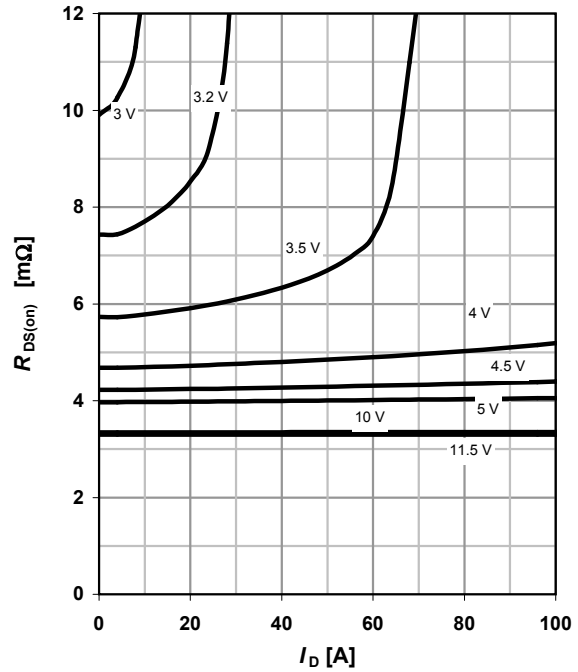
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

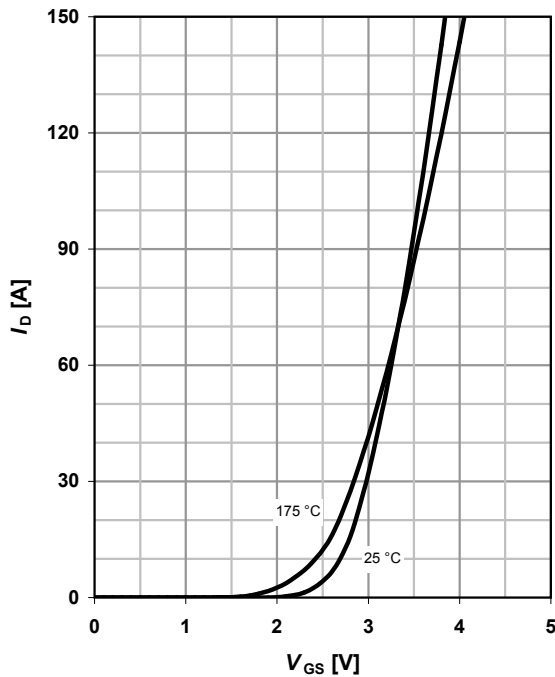
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

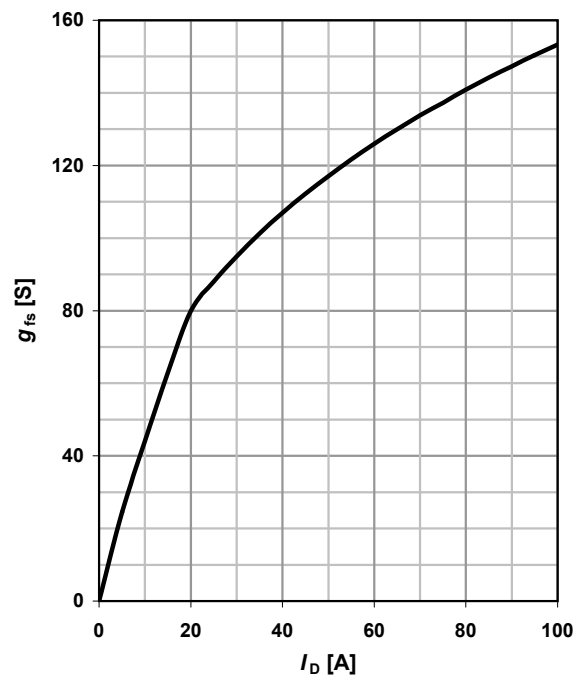
$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$

parameter:  $T_j$



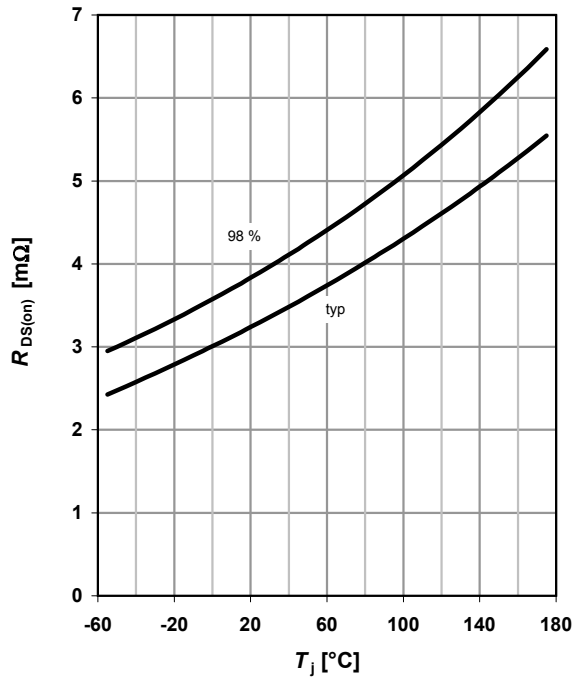
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



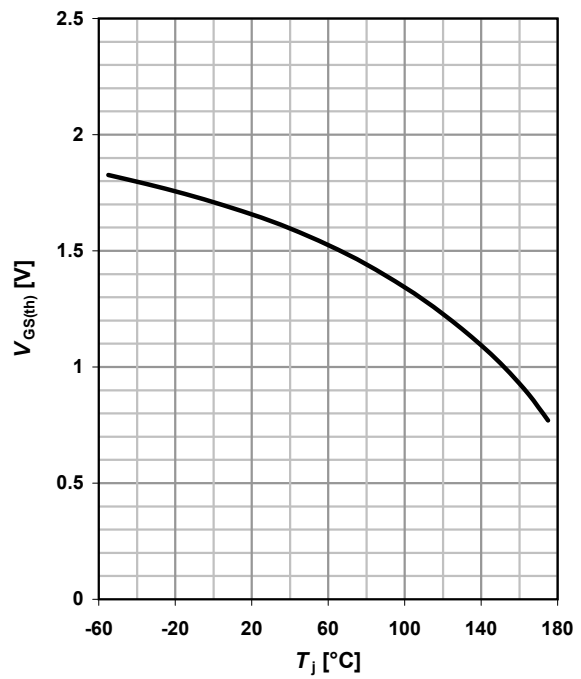
**9 Drain-source on-state resistance**

$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$$



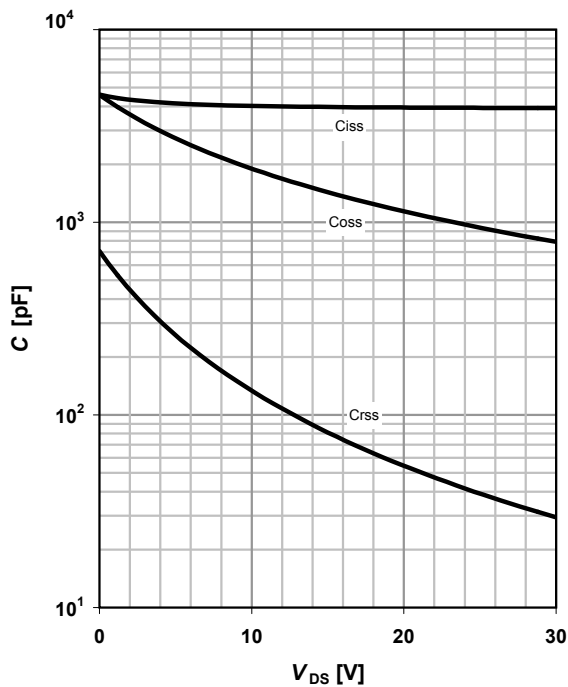
**10 Typ. gate threshold voltage**

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}$$



**11 Typ. capacitances**

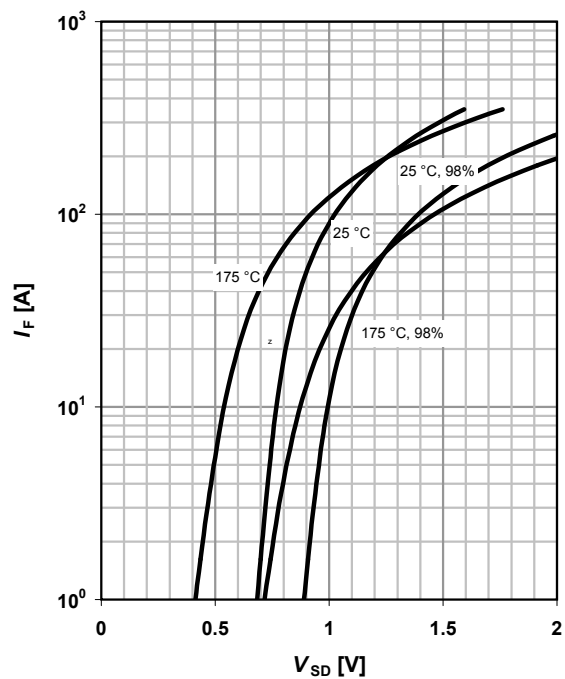
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



**12 Forward characteristics of reverse diode**

$$I_F = f(V_{SD})$$

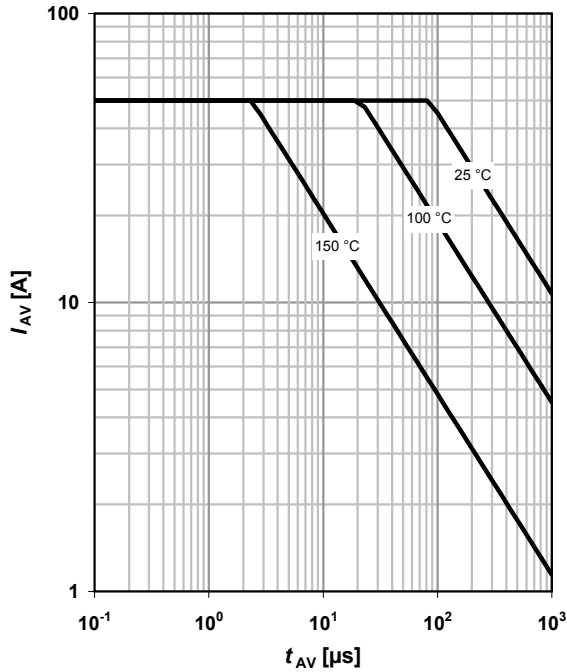
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

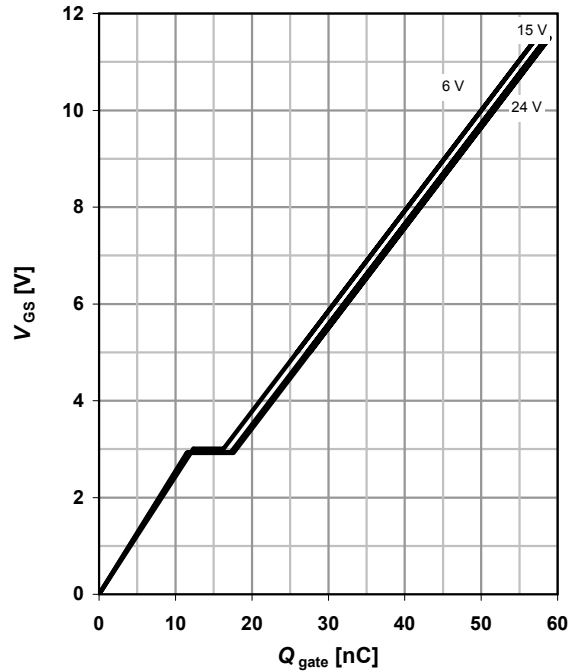
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

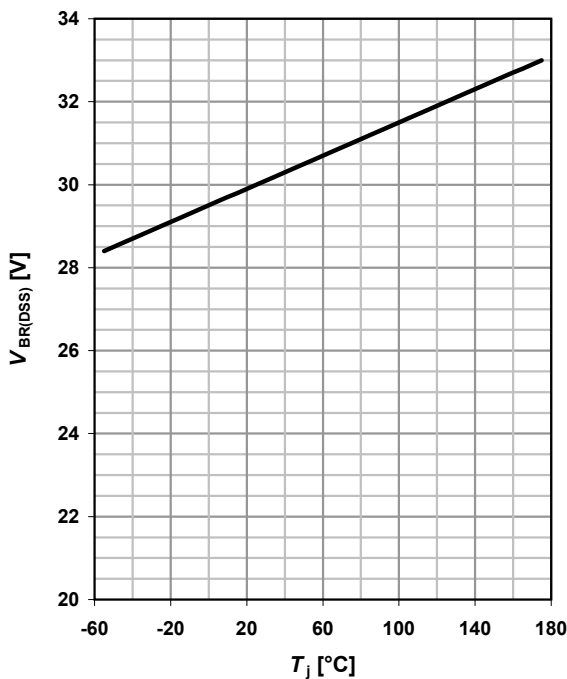
$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$

parameter:  $V_{DD}$

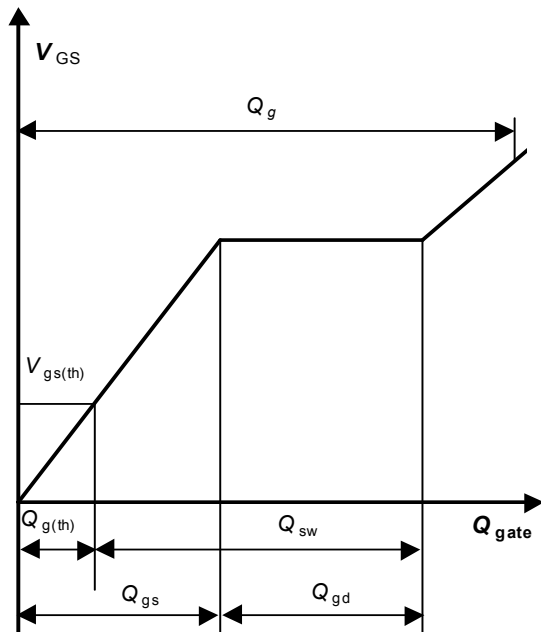


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

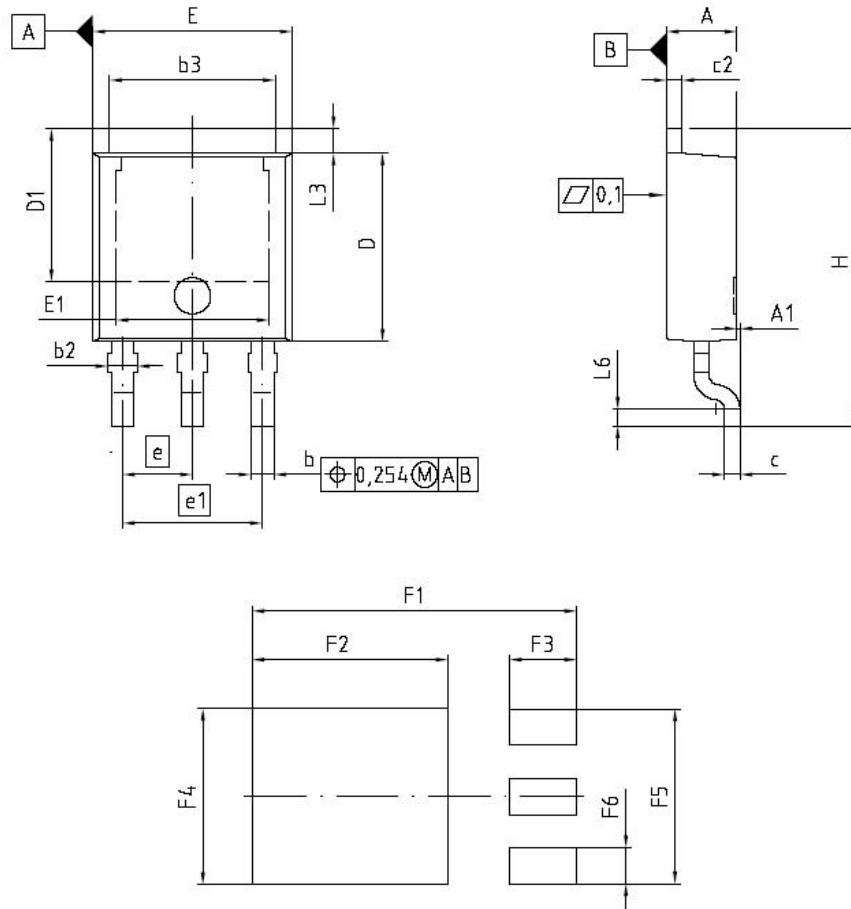


**16 Gate charge waveforms**



Package Outline

PG-TO252-3-23



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.159	2.413	0.085	0.095
A1	0.000	0.150	0.000	0.006
b	0.635	0.889	0.025	0.035
b2	0.650	1.150	0.026	0.045
b3	5.004	5.500	0.197	0.217
c	0.457	0.580	0.018	0.023
c2	0.460	0.980	0.018	0.039
D	5.969	6.223	0.235	0.245
D1	5.020	5.842	0.198	0.230
E	6.400	6.731	0.252	0.265
E1	4.850	5.207	0.191	0.205
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
H	9.400	10.480	0.370	0.413
L3	0.900	1.143	0.035	0.045
L4	0.584	0.950	0.023	0.037
L6	0.510	0.686	0.020	0.027
F1	10.500	10.700	0.413	0.421
F2	6.300	6.500	0.248	0.256
F3	2.100	2.300	0.083	0.091
F4	5.700	5.900	0.224	0.232
F5	5.660	5.860	0.222	0.231
F6	1.100	1.300	0.043	0.051

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-/-

SCALE

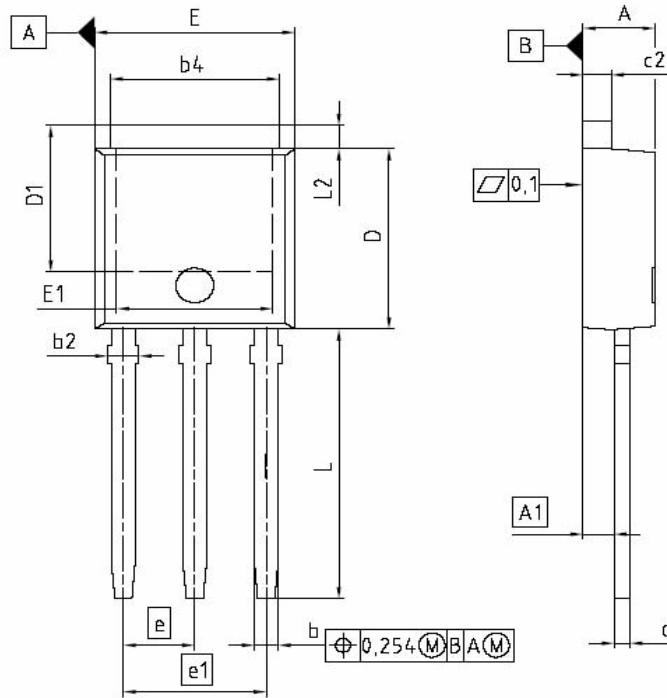
0 2.0 4mm

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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.158	2.413	0.085	0.095
A1	0.900	1.118	0.035	0.044
b	0.650	0.850	0.026	0.033
b2	0.650	1.150	0.026	0.045
b4	5.004	5.500	0.197	0.217
c	0.457	0.580	0.018	0.023
c2	0.737	0.980	0.029	0.039
D	5.969	6.223	0.235	0.245
D1	5.100	6.121	0.201	0.241
E	6.400	6.731	0.252	0.265
E1	4.850	5.207	0.191	0.205
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
L	8.900	9.525	0.350	0.375
L1	0.900	1.143	0.035	0.045

REFERENCE  
JEDEC TO251

SCALE 0 2.0 4mm

EUROPEAN PROJECTION

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