OUALIFICATION REQUIREMENTS REMOVED

MIL-M-38510/201C 24 March 1986 SUPERSEDING MIL-M-38510/2018 9 April 1982

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 512 BIT, BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON BIPOLAR.

I INACTIVE FOR NEW DESIGN AFTER DATE OF THIS REVISION 1

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

- 1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome resistors as the fusible link or programming element. One product assurance class and a choice of case outlines and lead finishes are provided for each type and are reflected in the part number.
- 1.2 Part number. The part number shall be in accordance with MIL-M-38510 except the JAN or "J" certification shall not be used.
 - 1.2.1 Device type. The device type shall be as follows:

| Device type | Circuit |
|-------------|--|
| 01 02 | 64 words/8 bits per word PROM with open collector 64 words/8 bits per word PROM with internal pull-up resistor |

- The device class shall be the product assurance level as 1.2.2 Device class. defined in MIL-M-38510.
 - 1.2.3 Case outline. The case outline shall be designated as follows:

| <u>Letter</u> | Case outline (see MIL-M-38510, appendix C) |
|---------------|---|
| J K | D-3 (24-lead, $1/2$ " x 1-1/4"), dual-in-line package F-6 (24-lead, $3/8$ " x $5/8$ "), flat package F-8 (24-lead, $1/4$ " x $3/8$ "), flat package |

1.3 Absolute maximum ratings.

-0.5 V dc to +7.0 V dc -1.5 V dc at -12 mA to +5.5 V dc -65° to +150°C Supply voltage range - - - - - - - -Input voltage range- - - - - - - - - -Storage temperature range- - -Lead temperature (soldering, 10 seconds) --Thermal resistance, junction-to-case (θეς)<u>1</u>/: See MIL-M-38510, appendix C

1/ Heat sinking is recommended to reduce junction temperature.

Beneficial comments (recommendations, additions, deletions) and any pertinent datal which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end lof this document or by letter.

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1.4 Recommended operating conditions:

Supply voltage - - - - - - - - - - 4.75 V dc minimum to 5.25 V dc maximum
Minimum high level input voltage (VIH) - - 2.0 V dc
Maximum low level input voltage (VIL) - - 0.8 V dc
Normalized fanout (each output) 4/ - - - 6 maximum (10 mA)
Case operating temperature range (TC) - - 55° to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 <u>Specifications and standards</u>. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. An altered item drawing shall be prepared by the contracting activity to specify the required program configuration.
- 3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.
- 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.
 - 2/ Must withstand the added PD due to short circuit test (e.g., I_{OS}).
 - Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.
 - 4/ The device shall fan out in both high and low levels to the specified number of inputs of the same device type as that being tested.

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TABLE I. Electrical performance characteristics.

| Characteristic | Symbol | Conditions | Device type | Lim Min | its Max | Unit |
|--|---------------------|--|----------------------|----------------|-------------------------|--------------------------|
| High level output voltage | Vон | VCC = 4.75 V VIN = 0.8 V IOH = 500 μA | 02 02 | 2.4 | | V |
| Low level output voltage | l V _{OL} | VCC = 4.75 V VIN = 2.0 V IOL = 10 mA | 01 (Ckt A) | | 0.45 | V |
| | | | 01 (Ckt B), 02 | | 0.50 | ! V |
| Input clamp voltage | , AIC | VCC = 4.75 V IIIN = -12 mA ITC = 25 C | 01, 02 | | -1.5 | V |
| Maximum collector cut-off current | I ICEX1 | VCC = 5.25 V VOH = 2.8 V VIN = 0.8 V | 01 | | 100 | μ Α |
| | I CEX2 | VCC = 5.25 V VOH = 5.25 V VIN = 0.8 V | 01 | | 200 | μΑ |
| High level input current | I _{IH1} | VCC = 5.25 V VIN = 2.4 V 1/ | 01, 02 | | 60 | μΑ |
| | I _{IH2} Da | ¥Cce≘t45.125 v v _{IN} = 5.25 v <u>2</u> / | 01, 02 | | 100 | μΑ |
| Low level input current | IIL | VCC = 5.25 V VIN = 0.4 V 2/ | 01, 02 | 1-0.2 | -1.6 | mA |
| Short circuit output current | Ios | VCC = 5.25 V VIN = 0 3/ | 02 | -1.6 | -5.0 | l mA |
| Supply current | Icc | V _{CC} = 5.25 V V _{IN} = 0 | 01, 02 | | 100 | mA |
| Propagation delay time high-to-low level logic | tpHL | V _{CC} = 5.0 V Figure 6 | 01, 02 | 25 | 140 | l ns |
| Propagation delay time l low-to-high level logic | tpLH | | 01, 02 | 25 | 140 | ns |

 $[\]underline{1}$ / When testing one E input, apply GND to the other.

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 $[\]underline{2}$ / When testing one E input, apply 5.25 V to the other.

^{3/} Not more than one output shall be grounded at one time.

3.2.2 Truth table.

- 3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in group A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.
- 3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.
- 3.2.3 Logic diagrams and schematic circuits. The logic diagrams and schematic circuits shall be as specified on figures 3 and 4.
 - 3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.
- 3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).
- 3.4 Electrical performance characteristics. The electrical performance characteristics of table 1 apply over the full recommended case operating temperature range, unless otherwise specified.
- 3.5 Electrical test requirements. The electrical test requirements for class B devices shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (see table III) Class B devices |
|--|---|
| Interim electrical test parameters (method 5004) | 1 |
| Final electrical test parameters (method 5004) for unprogrammed devices | 1*, 2, 3, 1 7*, 8 |
| Final electrical test parameters (method 5004) for programmed devices | 1 1*, 2, 3, 1 7*, 8, 9 |
| Group A test requirements (method 5005) | 1,2,3,7,8, |
| Group C end-point electrical parameters (method 5005) | 1,2,3,7,8 |
| Group D end-point electrical parameters (method 5005) | 1,2,3,7,8 |

NOTES:

- * indicates PDA applies to subgroups 1 and 7 (see 4.2c).
- Any or all subgroups may be combined when using high speed testers. Subgroups 7 and 8 shall consist of verifying the pattern specified.

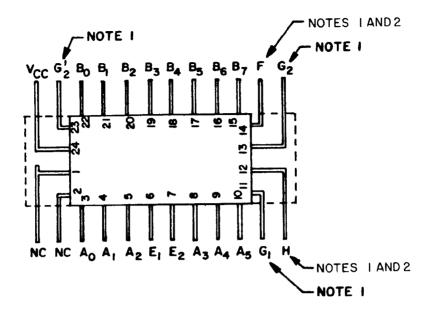
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Device types 01 and 02 (note 4)



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- 1. G_1 , G_2 and G_2 are connected to ground and F and H are left open for normal operation. 2. Terminal F is electrically open in device type 01, circuit A and is connected to an internal inverter (9th bit) for device type 01, circuit B and device type 02.
 - Terminal H is electrically open in device type 01, circuit B and device type 02 and is internally connected to the base of the memory transistor for device type 01, circuit A.
- Pin connections are the same for all case outlines com

FIGURE 1. Terminal connections.

| Word | INPUTS | | | | | | | ΩI | ITPI | UTS | | | | | |
|-------------|-------------|----------------|----------------|----|----------------|----------------|----------------|----|-------|-----|----|----|----|----|------------------|
| No. | <u>E</u> 1/ | A ₅ | A ₄ | A3 | A ₂ | A ₁ | A ₀ | В7 | B_6 | В5 | B4 | Вз | В2 | В1 | \mathbf{B}_{0} |
| <u>x2</u> / | L | х | x | x | x | x | х | Н | Н | Н | Н | Н | Н | Н | H |
| х | Н | х | х | x | x | x | x | L | L | L | L | L | L | L | L |

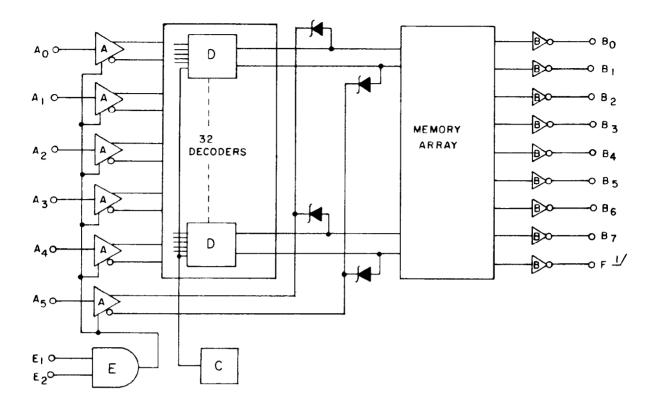
NOTES: $E = E_1 \cdot E_2$ 2/X = Irrelevant

FIGURE 2. Truth table (unprogrammed).

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NOTES: 1/Terminal F provides a 9th bit for test purposes only.

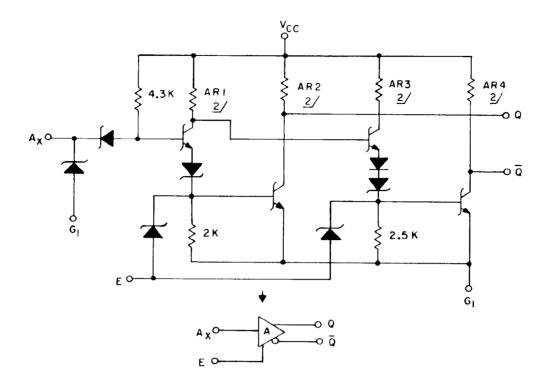
2/ AR1 = $3k\Omega$ and AR2 = AR3 = AR4 = $2.2k\Omega$ except in amplifier-inverter A5 where AR1 = $2.2k\Omega$, AR2 = AR4 = $1.2k\Omega$ and AR3 = $1.8k\Omega$.

3/ The $2k\Omega$ pull-up resistor is used for device type 02 only.

4/All resistance values are nominal.

 $5/G_2$ and G'_2 are internally connected together.

FIGURE 3. Logic diagram and schematic circuit for device type 01, circuit B and device type 02.



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I.IK

8.35 KΩ

G₁

G₂

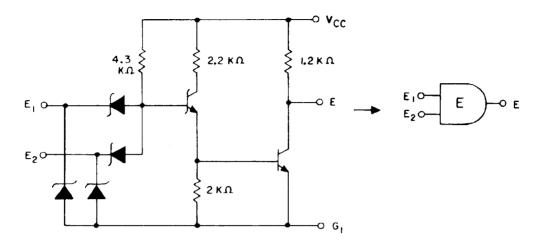
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FIGURE 3. Logic diagram and schematic circuit for device type 01, circuit B and device type 02 - Continued.

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4.7 K Ω

4.7 K Ω

TO AO THRU
A4

TO C

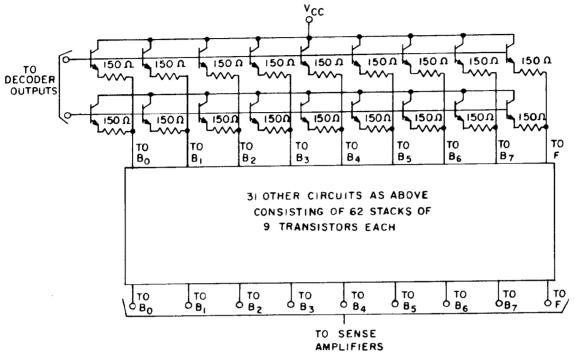
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FIGURE 3. Logic diagram and schematic circuit for device type 01, $\frac{\text{circuit B and device type 02}}{\text{circuit B and device type 02}}$

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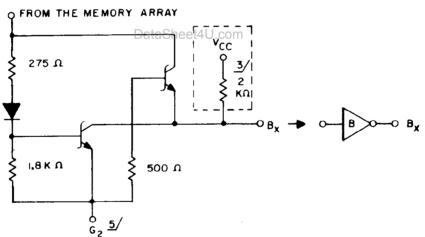


FIGURE 3. Logic diagram and schematic circuit for device type 01, circuit B and device type 02 - Continued.

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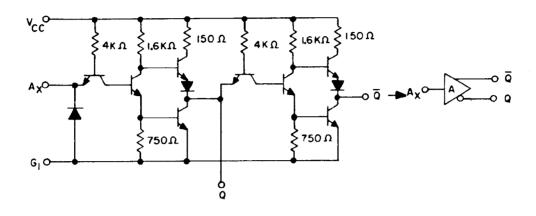
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FIGURE 4. Logic diagram and schematic circuit for device type 01, circuit A.

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VCC^O

4KΩ 1.6KΩ

1.750Ω

1.750Ω

1.750Ω

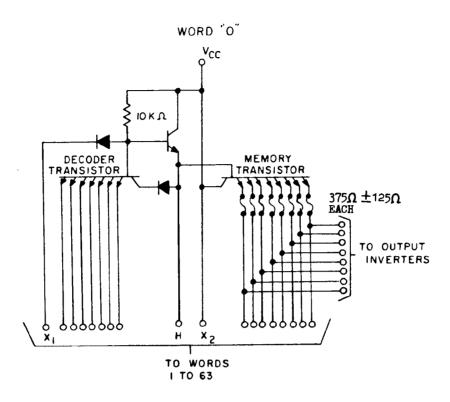
FIGURE 4. Logic diagram and schematic circuit for device type 01, circuit A - Continued.

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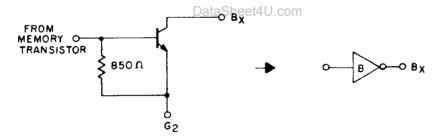
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NOTE: All resistance values are nominal.

FIGURE 4. Logic diagram and schematic circuit for device type Ol, circuit \underline{A} - Continued.

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5.0V (MINIMUM) v_{c c} R 80 Ao R В A_1 Q20-R Q30-A₂ Вз A₃ D. U.T. A4 В4 Q5 O-B₅ A₅ Q60-E, В, E2 Sheet4U.com

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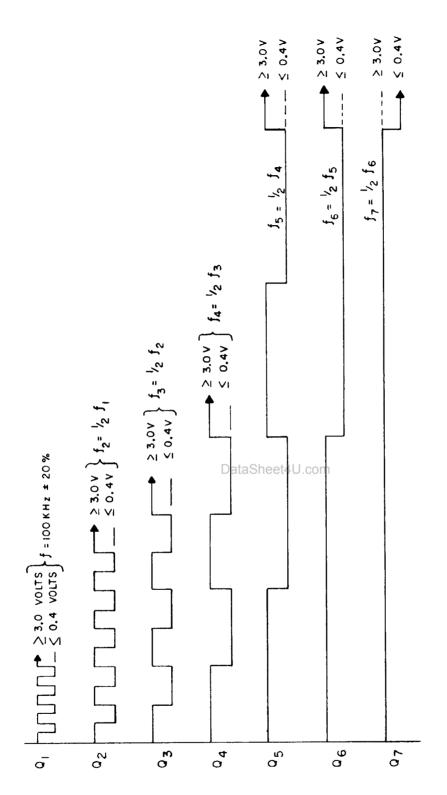
NOTE: $R = 470\Omega \pm 5\%$. All bit outputs shall have separate identical loads.

FIGURE 5. Burn-in and steady state life test circuit for device types 01 and 02.

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INPUT CONDITIONS

Burn-in and steady state life test circuit for device types 01 and 02 - Continued.

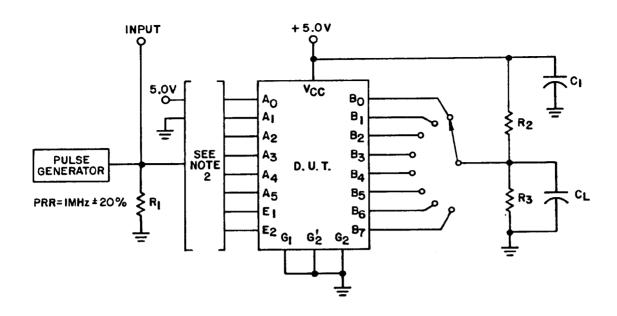
FIGURE 5.

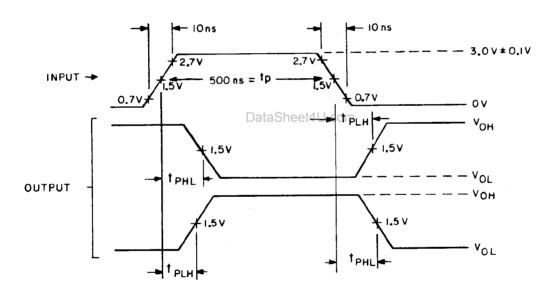
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NOTES:

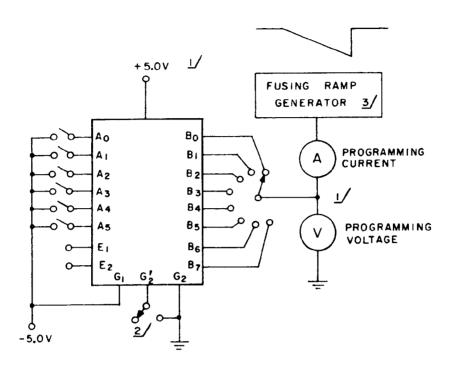
- 1. Pins 12 and 14 shall be left open. 2. Terminal conditions shall be as specified on table III. 3. $C_1 = .05 \mu F \pm 10$ percent; $R_1 = 51\Omega \pm 5$ percent; $R_2 = 470\Omega \pm 5$ percent; $R_3 = 1 k\Omega \pm 5$ percent, $c_{\rm L}^{\rm 2}$ = 30 pF minimum including jig and probe capacitance.

FIGURE 6. Switching time test circuit.

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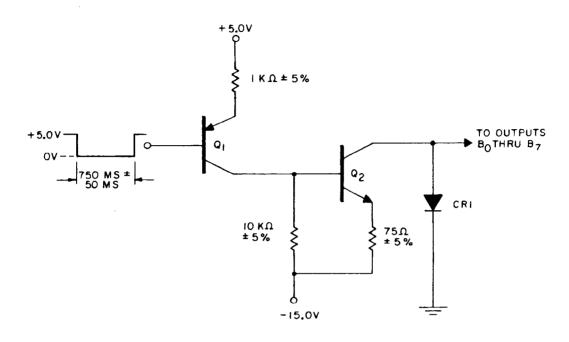
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NOTES: $\frac{1}{\text{Connect }-5.0\text{V}}$ to G1 before applying V_{CC} or programming voltage. $\frac{2}{\text{For device type 01, circuit A, G'_2 shall be open,}}$ For device types 01, circuit B, and 02, G'_2 shall be 0V. $\frac{3}{\text{Cenerator characteristics are defined in 4.6.}}$

FIGURE 7a. Programming circuit.

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NOTES:

- Q₁ = 2N2907 or equivalent.
 Q₂ = 2N1613 or equivalent.
 CR1 = 1N4573 or equivalent.

FIGURE 7b. Alternate high speed programming circuit.

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돨 Unit Test limits Min Max 9 8. V_{CC} 44444411 23 2,8 ¥ 10 11 22 2.8 ¥ 20 83 83 18 2.8 V 17 The conditions to the comparation for device type of the form half conditions to oppose and destinated are open or restrictive coupled to GMD or voltage; inputs not destinated are high $\Sigma_{\rm L}0$ by , low $\zeta_{\rm L}0$ by , or open. 2.8 V 10 m 16 15.25 V 15 4 21 = 5 2.4 1 0.4 v 10 |5.25 V | 1 0.4 V | 0.4 V | 2.4 V 용 6 Š 10.4 V | 5.25 V | GND 2.4 Y -12 mA 2.4 v GND 욹 15.25 V 0.4 V QNS 15.25 V 0.4 V 2.4 V SK G 23222323 333838783 type footnotes at end of device MIL-STD-883-method 3005 300 lcex2 lcex1 Symbol ន 1 IH2 Subgroup T_C = 25°C

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Un 1 Test Himits Measured **₹** 3 23 22 21 13 18 748LE 111. <u>Group A Inspection for device type 01</u> - Continued, Terminal conditions: Outputs not designated are opion oversitistic coupled to GNO or Voltage, Imputs not designated are high 22.0 %, low <u>c.0.3 %, or open.</u> 17 98 15 B7 ¥ + 13 subgroup 1, except $T_C = -55^{\circ}C$ and V_{IC} tests are omitted. Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted. 10 A5 | |Same tests, terminal conditions, and limits as for See footnotes at end of device type 01. MIL-STD-883-method Truth table test Subgroup $r_{\rm C} = \frac{3/4}{25^{\circ}}{\rm C}$ 3 1/ 2 1/

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Test limits Measured 33 23 ы 22 DOT DOT 21 ē DUT ສ OUT 50 19 ij OUT 18 TABLE III. Group A inspection for device type 01 - Continued. Terminal conditions: Outputs not designated are posen oversistive coupled to SMO or voltages inputs not designated are high 2.0° V, low 2.0° V, or open. ΕĪ Ę 17 TI0 OUT 91 DUT 15 Ę 14 Same tests and terminal conditions as for subgroup 9, except T_C = 125°C and the limits are 25 ns minimum and 140 ns maximum. ataSheet4U sheet4U she same tests, terminal conditions, and limits as for subgroup 10, except $T_{C}=-55^{\circ}\mathrm{C}$. Repeat subgroup 7, except TC = +125°C. Repeat subgroup 7, except T_C = -55°C. 122-185 186-249 Symbol |STD-883-|

tori The H

T_C = 25°C

Truth table test

| ' 8 |T_C = 125°C |and -55°C

Subgroup

Output voltages shall be either:

Input voltages shall be: A = 2.0 Y minimum; B = 0.8 V maximum $\underline{2}/~v_{DL}$ = 0.45 Y for circuit A and 0.50 V for circuit B.

a. H = 2.4 V minimum and $L = V_{0L}$ ($V_{0L} = 0.45$ V maximum for circuit B) when using a high speed cheeker double comparator.

b. $H_{2L}0$ V and L < 1.0 V when using a high speed checker single comparator.

Ferminal conditions (800 or 5.0 V) shall be as specified on figure 6 or in the altered item drawing, as applicable, so that all outputs are at a low logic level.

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Unprogrammed device conditions.

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4.

Unit Test limits Min | Max Measured 0-00045-10 24 23 OM5 22 -.5 mA 10 mA GND 21 GMD ଛ S 10 mA 18 ¥ш 5.-S 11 TABLE III. Group A inspection for device type 02. Terminal conditions: Outbuts not designated are open or resistive coupled to 3NO or voltage; inputs not designated are high $\Sigma L0$ V, low $\frac{L}{L0}B$ V, or open. 용 16 SNO 15 14 13 = 5 0.4 V 2.4 V 욹 2.4 V | 2.4 V | 0.4 v 15.25 V 5.25 V GND 6.25 V 0.4 v | 5.25 v GND 7 2.4 SND -12 mA 2.4 ¥ GND 9 0.4 7 Se 15.25 V æ 2.4 / 3 e 2 footnotes at end of device type 02. Cases 13,K,L Test 50 52 53 54 55 55 57 48 88 86 94 4 88 86 94 M1L-STD-883-method 3005 3006 100 <u>:</u> Subgroup T_C = 25°C

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Unit Test limits Measured terminal \$ D 23 22 2 21 8 13 18 TABLE III. Group A inspection for device type 02 - Continued. Terminal conditions of Upputs and designated are posm or resistate coupled to GMD or voltage; inputs not designated are high 2.0° V, for $q_{\rm CM}$ or open. 17 51 8 15 41 2 2 15 = 5 subgroup 1, except T_{C} = 125 $^{\circ}\mathrm{C}$ and V_{IC} tests are omitted. T_C = -55°C and Y_{IC} tests are omitted. 2 subgroup 1, except ||Same tests, terminal conditions, and limits as for Same tests, terminal conditions, and limits as for ~ footnotes at end of device type 02. MIL-STD-883-method Truth table test 7 2/3/ Tc = 25°C Subgroup 2 1/ 3 1/

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Unit

Min I Max Test limits

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15 14

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Subgroup

Repeat subgroup 7, except T_C = +125 °C. Repeat subgroup 7, except TC = -55°C.

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Truth table test

TC = 125°C

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Tc = 25°C

TABLE III. Group A inspection for device type 02 - Continued. Terminal conditions: Outputs not designated are open revisitive coupled to 000 or voltage; inputs not designated are high $\Sigma 2.0$ V_s , low Q0.8 V_s , or open.

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Couply voltages shall be either:

a. H = 2.4 V minimus and L = 0.5 V maximum when using a high speed cheeker double comparator.

b. H = 2.4 V minimus and L = 0.5 V maximum when using a high speed cheeker double comparator.

4. Terminal conditions (abl or 5.0 V) shall be as specified on figure 6 or in the altered (ten drawing, as applicable) so that all outputs are at a low logic level. 13 except T_{C} = 125 $^{\circ}$ C and the limits are 25 ns minimum and 140 ns maximum. 21 = DataShe 22

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Same tests and terminal conditions as for subgroup 9,

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- 3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity. The JAN or "J" certification shall not be used.
- 3.7 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of ROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.
- 3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.
- 3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.
- 3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).
- 3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device type described herein.
- 3.10 $\underline{\text{Certification}}.$ Certification in accordance with MIL-M-38510 is not required for this $\underline{\text{device}}.$
 - 4. QUALITY ASSURANCE PROVISIONS
- 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices priors to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test (method 1015 of MIL-STD-883); test condition D or E, using the circuit shown on figure 5 or equivalent.
 - b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical test parameters prior to burn-in is optional at the discretion of the manufacturer.
 - c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
 - d. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.
 - 4.3 Qualification inspection. Qualification inspection is not required.
 - 4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data may be used to satisfy the requirements for group C and D inspections (see 6.7).
 - 4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, and 6 shall be omitted.

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- c. Devices selected for testing in subgroups 9, 10, and 11 shall be programmed in accordance with 3.2.2.
- d. A programmability test shall be performed when programming the sample (12 devices) used in subgroups 9, 10, and 11 (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. If an additional sample is used (24 total devices), the lot shall be rejected if more than 4 devices fail to program.
- 4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.
- 4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 5 or equivalent.
 - (2) $T_A = 125^{\circ}C$ minimum.
 - (3) Test duration 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
 - c. For quality conformance inspection, the programmability sample (see 4.4.1d) shall be included in the subgroup 1 tests.
- 4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.
- 4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:
- 4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.
- 4.6 <u>Programming</u>. Using the test conditions of table IV, the following procedure shall be used for programming the device:
 - a. Connect the device as shown on figure 7a, using the fusing generator of figure 7a or the alternate circuit of figure 7b. The circuit shown on figure 7b can be used in more automated programming systems. This circuit generates a current pulse which is at the proper voltage and current levels for fast reliable programming. The input programming pulse width shall be 750 ±50 milliseconds. The number of attempts to program a given bit shall be as specified in table IV.
 - b. To address a particular word in the memory, set the input switches to the binary equivalent of that word, where a logical low level is -5.0 V and a logical high level is an open circuit. (Do not return to supply.) All output bits (B₀, B₁, . . B₇ of this word are not available for programming.
 - c. With the output current limited (as specified in table IV), apply a negative going current pulse to the pin associated with the first bit to be changed from a logical low level to a logical high level. This is most easily accomplished by connecting the negative terminal of a variable power supply output pin and manually increasing the voltage to approximately 6.0 volts.
 - d. Skipping any bit which is to remain a logical low level, repeat 4.6c for each logical low level in the word being addressed. Not more than one bit shall be programmed at a time.

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e. Set the next input address and repeat 4.6c and d. This procedure is repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A logical low level can always be changed to a logical high level, simply by repeating 4.6b and c. A logical low level, once programmed to a logical high level, cannot be reprogrammed.

TABLE IV. Programming specifications.

| Param | Value | | | |
|-----------------------------------|----------------------|-------------------------|--|--|
| Address input voltage | High logic level | Open circuit <u>1</u> / | | |
| | Low logic level | -5.0 V | | |
| Power supply voltage | +5.0 V +5%, -0% | | | |
| G ₁ voltage <u>2</u> / | -5.0 V | | | |
| G ₂ voltage | 0 V | | | |
| Device | 0 pen | | | |
| G' ₂ voltage Device | 0 V | | | |
| Maximum programming voltage | -7.0 V | | | |
| Maximum programming current | 1 100 mA | | | |
| Maximum number of attempts | 2 | | | |
| Maximum case temperature du | 75°C | | | |

- 1/ Open collector TTL gates meet this requirement.
- 2/ G₁ must be connected to -5.0 V prior to applying V_{CC} or programming voltage.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

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- 6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
 - 6.2 Ordering data. The acquisition document should specify the following:
 - a. Complete part number (see 1.2).
 - b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
 - c. Requirements for certificate of compliance, if applicable.

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- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for programming the device, including processing option.
- 6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

| GND | - - - | Electrical ground (common terminal). |
|-----------------|--------------|---|
| VTN | | Voltage level at an input terminal. |
| V | | Input clamp voltage. |
| I _{IN} | | Current flowing into an input terminal. |

- 6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer lead lengths and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.
- 6.6 <u>Substitutability</u>. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

| Military device type | Generic-industry type | | | | |
|-------------------------|--------------------------|--|--|--|--|
| 01 | HPROM- 0512, MCM 5303 | | | | |
| 0.2 | MCM 5304 | | | | |

- 6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.
- 6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.
- 6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

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Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, MC,

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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