16-bit Proprietary Microcontroller

CMOS

F^{2}MC-16L MB90670/675 Series

MB90671/672/673/T673/P673 (MB90670 Series)
MB90676/677/678/T678/P678 (MB90675 Series)

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■ DESCRIPTION

The MB90670/675 series is a member of 16-bit proprietary single-chip microcontroller F^{2}MC*^{1}-16L family designed to be combined with an ASIC (Application Specific IC) core. The MB90670/675 series is a high-performance general-purpose 16-bit microcontroller for high-speed real-time processing in various industrial equipment, OA equipment, and process control.

The instruction set of F^{2}MC-16L CPU core inherits AT architecture of F^{2}MC-8 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data (32-bit).

The MB90670/675 series has peripheral resources of UART0, UART1(SCI), an 8/10-bit A/D converter, an 8/16-bit PPG timer, a 16-bit reload timer, a 24-bit free run timer, an output compare (OCU), an input capture (ICU), DTP/external interrupt circuit, an I^{2}C*^{2} interface (in MB90675 series only). Embedded peripheral resources performs data transmission with an intelligent I/O service function without the intervention of the CPU, enabling real-time control in various applications.

*1: F^{2}MC stands for FUJITSU Flexible Microcontroller.

*2: Purchase of Fujitsu I^{2}C components conveys a license under the Philips I^{2}C Patent Rights to use these components in an I^{2}C system, provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.

■ PACKAGES

80-pin Plastic LQFP
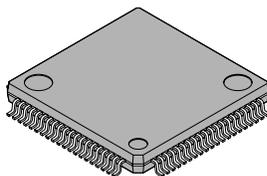
(FPT-80P-M05)

80-pin Plastic QFP
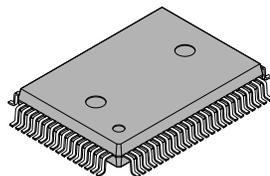
(FPT-80P-M06)

100-pin Plastic LQFP
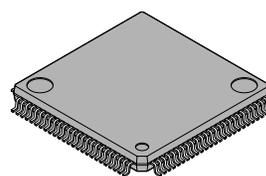
(FPT-100P-M05)

100-pin Plastic QFP

(FPT-100P-M06)

FUJITSU
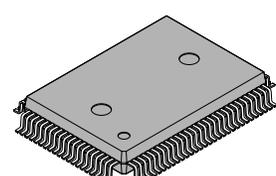
■ FEATURES

- Clock
  Embedded PLL clock multiplication circuit
  Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation
  (at oscillation of 4 MHz, 4 MHz to 16 MHz).
  Minimum instruction execution time of 62.5 ns (at oscillation of 4 MHz, four times the PLL clock, operation at
  Vcc of 5.0 V)
- CPU addressing space of 16 Mbytes
  Internal addressing of 24-bit
  External accessing can be performed by selecting 8/16-bit bus width (external bus mode)
- Instruction set optimized for controller applications
  Rich data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  High code efficiency
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Enhanced execution speed
  4-byte instruction queue
- Enhanced interrupt function
  8 levels, 32 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI²OS)
- Low-power consumption (standby) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Timebase timer mode (mode in which other than oscillation and timebase timer are stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Hardware standby mode
- Process
  CMOS technology
- I/O port
  MB90670 series: Maximum of 65 ports
  MB90675 series: Maximum of 84 ports
- Timer
  Timebase timer/watchdog timer: 1 channel
  8/16-bit PPG timer: 8-bit × 2 channels or 16-bit × 1 channel
  16-bit reload timer: 2 channels
  24-bit free run timer: 1 channel
- Input capture (ICU)
  Generates an interrupt request by latching a 24-bit free run timer counter value upon detection of an edge
  input to the pin.
- Output compare (OCU)
  Generates an interrupt request and reverse the output level upon detection of a match between the 24-bit free
  run timer counter value and the compare setting value.
- I²C interface (in MB90675 series only)
- Serial I/O port for supporting Inter IC BUS

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- UART0

  With full-duplex double buffer (8-bit length)

  Clock asynchronized or clock synchronized transmission (with start and stop bits) can be selectively used.
- UART1 (SCI)

  With full-duplex double buffer (8-bit length)

  Clock asynchronized or clock synchronized serial transmission (I/O extended serial) can be selectively used.
- DTP/external interrupt circuit (4 channels)

  A module for starting extended intelligent I/O service (EI^{2}OS) and generating an external interrupt triggered by an external input.
- Wake-up interrupt

  Receives external interrupt requests and generates an interrupt request upon an "L" level input.
- Delayed interrupt generation module

  Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)

  8-bit or 10-bit resolution can be selectively used.

  Starting by an external trigger input.

■ **PRODUCT LINEUP**

• MB90670 series

Item \ Part number	MB90671	MB90672	MB90673	MB90T673	MB90P673
Classification	Mask ROM products			External ROM product	One-time PROM product
ROM size	16 Kbytes	32 Kbytes	48 Kbytes	External ROM	48 Kbytes
RAM size	640 bytes	1.64 Kbytes	2 Kbytes		
CPU functions	Number of instructions:340 Instruction bit length:8 bits, 16 bits Instruction length:1 byte to 7 bytes Data bit length:1 bit, 8 bits, 16 bits Minimum execution time:62.5 ns (at machine clock of 16 MHz) Interrupt processing time:1.5 μs (at machine clock of 16 MHz, minimum value)				
Ports	General-purpose I/O ports (CMOS output): 57 General-purpose I/O ports (N-ch open-drain output): 8 Total: 65				
UART0	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronized transmission (4800 Kbps to 500 Kbps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.				
UART1 (SCI)	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronized transmission (2400 Kbps to 62500 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.				
8/10-bit A/D converter	Conversion precision: 10-bit or 8-bit selectable Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)				
8/16-bit PPG timer	Number of channels: 2 8-bit or 16-bit PPG operation A Pulse wave of given intervals and given duty ratios can be output. Pulse cycle: 125 ns to 16.78 s (at oscillation of 4 MHz, machine clock of 16 MHz)				
16-bit reload timer	Number of channels: 2 16-bit reload timer operation Interval: 125 ns to 131 ms (at machine clock of 16 MHz) External event count can be performed.				
24-bit free run timer	Number of channel :1 Overflow interrupts or intermediate bit interrupts may be generated.				
Output compare unit (OCU)	Number of channels: 8 Pin input factor: A match signal of compare register				

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MB90670/675 Series

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Part number\Item	MB90671	MB90672	MB90673	MB90T673	MB90P673
Input capture unit (ICU)	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)				
DTP/external interrupt circuit	Number of inputs: 4 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input. External interrupt circuit or extended intelligent I/O service (EI²OS) can be used.				
Wake-up interrupt	Number of inputs: 8 Started by an "L" level input.				
Delayed interrupt generation module	An interrupt generation module for switching tasks used in real-time operating systems.				
I²C interface	None				
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)				
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)				
Low-power consumption (standby) mode	Sleep/stop/CPU intermittent operation/timebase timer/hardware stand-by				
Process	CMOS				
Operating voltage*	2.7 V to 5.5 V				

*: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

• MB90675 series

Part number / Item	MB90676	MB90677	MB90678	MB90T678	MB90P678	MB90V670
Classification	Mask ROM products			External ROM product	One-time PROM product	Evaluation product
ROM size	32 Kbytes	48 Kbytes	64 Kbytes	None	64 Kbytes	—
RAM size	1.64 Kbytes	2 Kbytes	3 Kbytes			4 Kbytes
CPU functions	The number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock of 16 MHz) Interrupt processing time: 1.5 μs (at machine clock of 16 MHz, minimum value)					
Ports	General-purpose I/O ports (CMOS output): 74 General-purpose I/O ports (N-ch open-drain output): 10 Total: 84					
UART0	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronized transmission (4800 Kbps to 500 Kbps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.					
UART1 (SCI)	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronized transmission (2400 Kbps to 62500 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.					
8/10-bit A/D converter	Conversion precision: 10-bit or 8-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)					
8/16-bit PPG timer	Number of channels: 2 PPG operation of 8-bit or 16-bit Pulse of given intervals and given duty ratios can be output Pulse interval 125 ns to 16.78 s (at oscillation of 4 MHz, machine clock of 16 MHz)					
16-bit reload timer	Number of channels: 2 16-bit reload timer operation Interval: 125 ns to 131 ms (at machine clock of 16 MHz) External event count can be performed.					
24-bit free run timer	Number of channel :1 Overflow interrupts or intermediate bit interrupts may be generated.					
Output compare (OCU)	Number of channels: 8 Pin input factor: a match signal of compare register					

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Item \ Part number	MB90676	MB90677	MB90678	MB90T678	MB90P678	MB90V670
Input capture (ICU)	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)					
DTP/external interrupt circuit	Number of inputs: 4 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input. External interrupt circuit or extended intelligent I/O service (EI^{2}OS) can be used.					
Wake-up interrupt	Number of inputs: 8 Started by an "L" level input.					
Delayed interrupt generation module	An interrupt generation module for switching tasks used in realtime operating systems.					
I^{2}C interface	Serial I/O port for supporting Inter IC BUS					
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)					
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)					
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/timebase timer/hardware stand-by					
Process	CMOS					
Power supply voltage for operation*	2.7 V to 5.5 V					

*: Varies with conditions such as the operating frequency. (See section "■ ELECTRICAL CHARACTERISTICS.")
   Assurance for the MB90V670 is given only for operation with a tool at a power voltage of 2.7 V to 5.5 V, an
   operating temperature of 0°C to 70°C, and an operating frequency of 1.5 MHz to 16 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90671 MB90672 MB90673 MB90T673	MB90P673	MB90676 MB90677 MB90678 MB90T678	MB90P678	MB90V670
FPT-80P-M05	○	○	×	×	×
FPT-80P-M06	○	○	×	×	×
FPT-100P-M05	×	×	○	○	×
FPT-100P-M06	×	×	○	○	×

○ : Available   × : Not available

Note: For more information about each package, see section "■ PACKAGE DIMENSIONS."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

In evaluation with an evaluation product, note the difference between the evaluation chip and the chip actually used. The following items must be taken into consideration.

• The MB90V670 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.

• In the MB90V670, images from FF4400$_H$ to FFFFFF$_H$ are mapped to bank 00, and FE0000$_H$ to FF3FFF$_H$ to mapped to bank FE$_H$ and FF$_H$ only. (This setting can be changed by configuring the development tool.)

• In the MB90678/MB90P678, images from FF4000$_H$ to FFFFFF$_H$ are mapped to bank 00, and FF0000$_H$ to FF3FFF$_H$ to bank FF only.

2. Mask Options

Functions selected by optional settings and methods for setting the options are dependent on the product types.
Refer to "■ Mask Options" for detailed information.
Note that mask option is fixed in MB90V670 series.

■ PIN ASSIGNMENTS

(Top view)

Pin labels left side (1-20):
P20/A16, P21/A17, P22/A18, P23/A19, P24/TIN0, P25/TIN1, P26/TOT0, P27/TOT1, Vss, P30/ALE, P31/$\overline{RD}$, P32/$\overline{WRL}$/$\overline{WR}$, P33/$\overline{WRH}$, P34/$\overline{HRQ}$, P35/$\overline{HAK}$, P36/RDY, P37/CLK, P40/SIN0, P41/SOT0, P42/SCK0

Top (80-61):
P17/AD15/WI7, P16/AD14/WI6, P15/AD13/WI5, P14/AD12/WI4, P13/AD11/WI3, P12/AD10/WI2, P11/AD09/WI1, P10/AD08/WI0, P07/AD07, P06/AD06, P05/AD05, P04/AD04, P03/AD03, P02/AD02, P01/AD01, P00/AD00, Vcc, X1, X0, Vss

Right (60-41):
$\overline{RST}$, P80/PPG1, P77/DOT7, P76/DOT6, P75/DOT5, P74/DOT4, P73/DOT3, P72/DOT2, P71/DOT1, P70/DOT0, P67/ASR3, P66/ASR2, P65/ASR1, P64/ASR0, P63/INT3, P62/INT2, P61/INT1, P60/INT0, $\overline{HST}$, MD2

Bottom (21-40):
P43/SIN1, P44/SOT1, P45/SCK1, P46/PPG0, P47/$\overline{ATG}$, AVcc, AVRH, AVRL, AVss, P50/AN0, P51/AN1, Vss, P52/AN2, P53/AN3, P54/AN4, P55/AN5, P56/AN6, P57/AN7, MD0, MD1

(FPT-80P-M05)

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(Top view)

P15/AD13/WI5
P14/AD12/WI4
P13/AD11/WI3
P12/AD10/WI2
P11/AD09/WI1
P10/AD08/WI0
P07/AD07
P06/AD06
P05/AD05
P04/AD04
P03/AD03
P02/AD02
P01/AD01
P00/AD00
V$_{CC}$
X1

80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65

P16/AD14/WI6	1	64 X0
P17/AD15/WI7	2	63 V$_{SS}$
P20/A16	3	62 $\overline{RST}$
P21/A17	4	61 P80/PPG1
P22/A18	5	60 P77/DOT7
P23/A19	6	59 P76/DOT6
P24/TIN0	7	58 P75/DOT5
P25/TIN1	8	57 P74/DOT4
P26/TOT0	9	56 P73/DOT3
P27/TOT1	10	55 P72/DOT2
V$_{SS}$	11	54 P71/DOT1
P30/ALE	12	53 P70/DOT0
P31/$\overline{RD}$	13	52 P67/ASR3
P32/$\overline{WRL}$/$\overline{WR}$	14	51 P66/ASR2
P33/$\overline{WRH}$	15	50 P65/ASR1
P34/$\overline{HRQ}$	16	49 P64/ASR0
P35/$\overline{HAK}$	17	48 P63/INT3
P36/RDY	18	47 P62/INT2
P37/CLK	19	46 P61/INT1
P40/SIN0	20	45 P60/INT0
P41/SOT0	21	44 $\overline{HST}$
P42/SCK0	22	43 MD2
P43/SIN1	23	42 MD1
P44/SOT10	24	41 MD0

25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

P45/SCK1
P46/PPG0
P47/$\overline{ATG}$
AV$_{CC}$
AVRH
AVRL
AV$_{SS}$
P50/AN0
P51/AN1
V$_{SS}$
P52/AN2
P53/AN3
P54/AN4
P55/AN5
P56/AN6
P57/AN7

(FPT-80P-M06)

(Continued)

(Top view)

Top pins (left to right, pins 100–76):
P21/A17 (100), P20/A16 (99), P17/AD15/WI7 (98), P16/AD14/WI6 (97), P15/AD13/WI5 (96), P14/AD12/WI4 (95), P13/AD11/WI3 (94), P12/AD10/WI2 (93), P11/AD09/WI1 (92), P10/AD08/WI0 (91), P07/AD07 (90), P06/AD06 (89), P05/AD05 (88), P04/AD04 (87), P03/AD03 (86), P02/AD02 (85), P01/AD01 (84), P00/AD00 (83), Vcc (82), X1 (81), X0 (80), Vss (79), PB2 (78), PB1 (77), PB0 (76)

Left pins (top to bottom, pins 1–25):
P22/A18 (1)
P23/A19 (2)
P24/TIN0 (3)
P25/TIN1 (4)
P26/TOT0 (5)
P27/TOT1 (6)
P30/ALE (7)
P31/RD (8)
Vss (9)
P32/WRL/WR (10)
P33/WRH (11)
P34/HRQ (12)
P35/HAK (13)
P36/RDY (14)
P37/CLK (15)
P40/SIN0 (16)
P41/SOT0 (17)
P42/SCK0 (18)
P43/SIN1 (19)
P44/SOT1 (20)
Vcc (21)
P45/SCK1 (22)
P46/PPG0 (23)
P47/ATG (24)
P80/PPG1 (25)

Right pins (top to bottom, pins 75–51):
RST (75)
PA7 (74)
PA6 (73)
PA5 (72)
PA4 (71)
PA3 (70)
PA2 (69)
PA1 (68)
PA0 (67)
P77/DOT7 (66)
P76/DOT6 (65)
P75/DOT5 (64)
P74/DOT4 (63)
P73/DOT3 (62)
P72/DOT2 (61)
P71/DOT1 (60)
P70/DOT0 (59)
P67/ASR3 (58)
P66/ASR2 (57)
P65/ASR1 (56)
P64/ASR0 (55)
P63/INT3 (54)
P62/INT2 (53)
P61/INT1 (52)
P60/INT0 (51)

Bottom pins (left to right, pins 26–50):
P81 (26), P82 (27), P83 (28), P84 (29), P85 (30), P86 (31), AVcc (32), AVRH (33), AVRL (34), AVss (35), P50/AN0 (36), P51/AN1 (37), Vss (38), P52/AN2 (39), P53/AN3 (40), P54/AN4 (41), P55/AN5 (42), P56/AN6 (43), P57/AN7 (44), P90/SDA (45), P91/SCL (46), MD0 (47), MD1 (48), MD2 (49), HST (50)

(FPT-100P-M05)

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(Top view)

Left side pins:

Pin	Signal
1	P20/A16
2	P21/A17
3	P22/A18
4	P23/A19
5	P24/TIN0
6	P25/TIN1
7	P26/TOT0
8	P27/TOT1
9	P30/ALE
10	P31/$\overline{RD}$
11	Vss
12	P32/$\overline{WRL}$/$\overline{WR}$
13	P33/$\overline{WRH}$
14	P34/$\overline{HRQ}$
15	P35/$\overline{HAK}$
16	P36/RDY
17	P37/CLK
18	P40/SIN0
19	P41/SOT0
20	P42/SCK0
21	P43/SIN1
22	P44/SOT1
23	Vcc
24	P45/SCK1
25	P46/PPG0
26	P47/$\overline{ATG}$
27	P80/PPG1
28	P81
29	P82
30	P83

Right side pins:

Pin	Signal
80	PB2
79	PB1
78	PB0
77	$\overline{RST}$
76	PA7
75	PA6
74	PA5
73	PA4
72	PA3
71	PA2
70	PA1
69	PA0
68	P77/DOT7
67	P76/DOT6
66	P75/DOT5
65	P74/DOT4
64	P73/DOT3
63	P72/DOT2
62	P71/DOT1
61	P70/DOT0
60	P67/ASR3
59	P66/ASR2
58	P65/ASR1
57	P64/ASR0
56	P63/INT3
55	P62/INT2
54	P61/INT1
53	P60/INT0
52	$\overline{HST}$
51	MD2

Top side pins:

Pin	Signal
100	P17/AD15/WI7
99	P16/AD14/WI6
98	P15/AD13/WI5
97	P14/AD12/WI4
96	P13/AD11/WI3
95	P12/AD10/WI2
94	P11/AD09/WI1
93	P10/AD08/WI0
92	P07/AD07
91	P06/AD06
90	P05/AD05
89	P04/AD04
88	P03/AD03
87	P02/AD02
86	P01/AD01
85	P00/AD00
84	Vcc
83	X1
82	X0
81	Vss

Bottom side pins:

Pin	Signal
31	P84
32	P85
33	P86
34	AVCC
35	AVRH
36	AVRL
37	AVSS
38	P50/AN0
39	P51/AN1
40	VSS
41	P52/AN2
42	P53/AN3
43	P54/AN4
44	P55/AN5
45	P56/AN6
46	P57/AN7
47	P90/SDA
48	P91/SCL
49	MD0
50	MD1

(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.				Pin name	Circuit type	Function
LQFP -80[*1]	QFP -80[*2]	LQFP -100[*3]	QFP -100[*4]			
62	64	80	82	X0	A (Oscillation)	Crystal oscillator pins
63	65	81	83	X1		
39 to 41	41 to 43	47 to 49	49 to 51	MD0 to MD2	F (CMOS)	Input pins for selecting operation modes Connect directly to V_{CC} or V_{SS}.
60	62	75	77	$\overline{RST}$	H (CMOS/H)	External reset request input
42	44	50	52	$\overline{HST}$	G (CMOS/H)	Hardware standby input pin
65 to 72	67 to 74	83 to 90	85 to 92	P00 to P07	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				AD00 to AD07		I/O pins for the lower 8-bit of the external address data bus This function is valid in the mode where the external bus is valid.
73 to 78, 79, 80	75 to 80, 1, 2	91 to 96, 97, 98	93 to 98, 99, 100	P10 to P15, P16, P17	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				AD08 to AD13, AD14, AD15		I/O pins for the upper 8-bit of the external address data bus This function is valid in the mode where the external bus is valid.
				WI0 to WI5, WI6, WI7		I/O pins for wake-up interrupts This function is valid in the single-chip mode. Because the input of the DTP/external interrupt circuit is used as required when the DTP/external interrupt circuit is enabled, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
1, 2, 3, 4	3, 4, 5, 6	99, 100, 1, 2	1, 2, 3, 4	P20, P21, P22, P23	B (CMOS)	General-purpose I/O port This function becomes valid in the single-chip mode or the external address output control register is set to select a port.
				A16, A17, A18, 19		Output pins for the external address bus of A16 to A19 This function is valid in the mode where the external bus is valid and the upper address control register is set to select an address.

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*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

Pin no.				Pin name	Circuit type	Function
LQFP-80*1	QFP-80*2	LQFP-100*3	QFP-100*4			
5, 6	7, 8	3, 4	5, 6	P24, P25	E (CMOS/H)	General-purpose I/O port This function is always valid.
				TIN0, TIN1		Event input pins of 16-bit reload timer 0 and 1 Because this input is used as required when the 16-bit reload timer is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
7, 8	9, 10	5, 6	7, 8	P26, P27	E (CMOS/H)	General-purpose I/O port This function is valid when outputs from 16-bit reload timer 0 and 1 are disabled.
				TOT0, TOT1		Output pins for 16-bit reload timer 0 and 1 This function is valid when output from 16-bit reload timer 0 and 1 are enabled.
10	12	7	9	P30	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				ALE		Address latch enable output pin This function is valid in the mode where the external bus is valid.
11	13	8	10	P31	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				$\overline{RD}$		Read strobe output pin for the data bus This function is valid in the mode where the external bus is valid.
12	14	10	12	P32	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode or $\overline{WRL}/\overline{WR}$ pin output is disabled.
				$\overline{WRL}$ $\overline{WR}$		Write strobe output pin for the data bus This function is valid when $\overline{WRL}/\overline{WR}$ pin output is enabled in the mode where external bus is valid. $\overline{WRL}$ is used for holding the lower 8-bit for write strobe in 16-bit access operations, while $\overline{WR}$ is used for holding 8-bit data for write strobe in 8-bit access operations.
13	15	11	13	P33	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode, in the external bus 8-bit mode, or $\overline{WRH}$ pin output is disabled.
				$\overline{WRH}$		Write strobe output pin for the upper 8-bit of the data bus This function is valid when the external bus 16-bit mode is selected in the mode where the external bus is valid, and $\overline{WRH}$ output pin is enabled.

(Continued)

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
14	16	12	14	P34	B (CMOS)	General-purpose I/O port This function is valid when both the single-chip mode and the hold function are disabled.
				HRQ		Hold request input pin This function is valid in the mode where the external bus is valid or when the hold function is enabled.
15	17	13	15	P35	B (CMOS)	General-purpose I/O port This function is valid when both the single-chip mode and the hold function are disabled.
				$\overline{\text{HAK}}$		Hold acknowledge output pin This function is valid in the mode where the external bus is valid or when the hold function is enabled.
16	18	14	16	P36	B (CMOS)	General-purpose I/O port This function is valid when both the single-chip mode and the external ready function are disabled.
				RDY		Ready input pin This function is valid when the external ready function is enabled in the mode where the external bus is valid.
17	19	15	17	P37	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode or when the CLK output is disabled.
				CLK		CLK output pin This function is valid when CLK output is disabled in the mode where the external bus is valid.
18	20	16	18	P40	E (CMOS/H)	General-purpose I/O port This function is always valid.
				SIN0		Serial data input pin of UART0 Because this input is used as required when UART0 is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
19	21	17	19	P41	E (CMOS/H)	General-purpose I/O port This function is valid when serial data output from UART0 is disabled.
				SOT0		Serial data output pin of UART0 This function is valid when serial data output from UART0 is enabled.

(Continued)

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
20	22	18	20	P42	E (CMOS/H)	General-purpose I/O port This function is valid when clock output from UART0 is disabled.
				SCK0		Clock I/O pin of UART0 This function is valid when clock output from UART0 is enabled. Because this input is used as required when UART0 is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
21	23	19	21	P43	E (CMOS/H)	General-purpose I/O port This function is always valid.
				SIN1		Serial data input pin of UART1 (SCI) Because this input is used as required when UART1 (SCI) is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
22	24	20	22	P44	E (CMOS/H)	General-purpose I/O port This function is valid when serial data output from UART1 (SCI) is disabled.
				SOT1		Serial data output pin of UART1 (SCI) This function is valid when serial data output from UART1 (SCI) is enabled.
23	25	22	24	P45	E (CMOS/H)	General-purpose I/O port This function is valid when clock output from UART1 (SCI) is disabled.
				SCK1		Clock I/O pin of UART1 (SCI) This function is valid when clock output from UART1 (SCI) is enabled. Because this input is used as required when UART1 (SCI) is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
24	26	23	25	P46	E (CMOS/H)	General-purpose I/O port This function is valid when waveform output from 8/16-bit PPG timer 0 is disabled.
				PPG0		Output pin of 8/16-bit PPG timer 0 This function is valid when waveform output from 8/16-bit PPG timer 0 is enabled.

(Continued)

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
25	27	24	26	P47	E (CMOS/H)	General-purpose I/O port This function is always valid.
				$\overline{\text{ATG}}$		Trigger input pin of the 8/10-bit A/D converter Because this input is used as required when the 8/10-bit A/D converter is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
30, 31, 33, 34, 35 to 38	32, 33, 35, 36, 37 to 40	36, 37, 38, 39, 41 to 44	38, 39, 40, 41, 43 to 46	P50, P51, P52, P53, P54 to P57	C (CMOS/H)	I/O port of an open-drain type The input function is valid when the analog input enable register is set to select a port.
				AN0, AN1, AN2, AN3, AN4 to AN7		Analog input pins of the 8/10-bit A/D converter This function is valid when the analog input enable register is set to select AD.
43 to 46	45 to 48	51 to 54	53 to 56	P60 to P63	E (CMOS/H)	General-purpose I/O port This function is always valid.
				INT0 to INT3		Request input pins of the DTP/external interrupt circuit Because this input is used as required when the DTP/external interrupt circuit is performing input operations, and it is necessary to stop outputs from other functions unless such outputs are made intentionally.
47 to 50	49 to 52	55 to 58	57 to 60	P64 to P67	E (CMOS/H)	General-purpose I/O port This function is always valid.
				ASR0 to ASR3		Sample data input pins for ICU0 to ICU3 Because this input is used as required when the input capture (ICU) is performing input operations, and it is necessary to stop outputs from other functions unless such outputs are made intentionally.
51 to 58	53 to 60	59 to 66	61 to 68	P70 to P77	E (CMOS/H)	General-purpose I/O port This function is valid when waveform output from the output compare (OCU) is disabled.
				DOT0 to DOT7		Waveform output pins of OCU0 and OCU1 This function is valid when waveform output from the output compare (OCU) is enabled and output from the port is selected.

(Continued)

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

(Continued)

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
59	61	25	27	P80	E (CMOS/H)	General-purpose I/O port This function is valid when waveform output from 8/16-bit PPG timer 1 is disabled.
				PPG1		Output pin of 8/16-bit PPG timer 1 This function is valid when waveform output from 8/16-bit PPG timer 1 is enabled.
—	—	26 to 31	28 to 33	P81 to P86	E (CMOS/H)	General-purpose I/O port This function is always valid.
—	—	45	47	P90	D (NMOS/H)	I/O port of an open-drain type This function is always valid.
				SDA		I/O pin of the I^2C interface This function is valid when operation of the I^2C interface is enabled. Hold the port output in the high-impedance status (PDR = 1) when the I^2C interface is in operation.
—	—	46	48	P91	D (NMOS/H)	I/O port of an open-drain type This function is always valid.
				SCL		Clock I/O pin of the I^2C interface This function is valid when operation of the I^2C interface is enabled. Hold the port output in the high-impedance status (PDR = 1) when the I^2C interface is in operation.
—	—	67 to 74	69 to 76	PA0 to PA7	E (CMOS/H)	General-purpose I/O port This function is always valid.
—	—	76 to 78	78 to 80	PB0 to PB2	E (CMOS/H)	General-purpose I/O port This function is always valid.
64	66	21, 82	23, 84	V_{CC}	Power supply	Power supply to the digital circuit
9, 32, 61	11, 34, 63	9, 40, 79	11, 42, 81	V_{SS}	Power supply	Ground level of the digital circuit
26	28	32	34	AV_{CC}	Power supply	Power supply to the analog circuit Make sure to turn on/turn off this power supply with a voltage exceeding AV_{CC} applied to V_{CC}.
27	29	33	35	AVRH	Power supply	Reference voltage input to the analog circuit Make sure to turn on/turn off this power supply with a voltage exceeding AVRH applied to AV_{CC}.
28	30	34	36	AVRL	Power supply	Reference voltage input to the analog circuit
29	31	35	37	AV_{SS}	Power supply	Ground level of the analog circuit

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1 P-ch N-ch Clock input X0 Standby control signal	• External clock frequency 3 MHz to 32 MHz • Oscillation feedback resistor approx. 1MΩ
B	R P-ch Digital output N-ch Digital output Digital input Standby control signal	• CMOS level input/output (with standby control) • Pull-up option selectable (with standby control) • No pull-up resistor in the MB90V670
C	Digital output A/D input Digital input A/D disable	• N-ch open-drain output • CMOS level hystheresis input (with A/D control)
D	P-ch N-ch Digital output Digital input Standby control signal	• NMOS open-drain output • CMOS level hysteresis input (with standby control)

(Continued)

(Continued)

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input (with standby control) • Pull-up option selectable (with standby control) • No pull-up resistor in the MB90V670
F		• CMOS level input/output (without standby control) • Pull-up/pull-down option selectable (without stand-by control) • In mask ROM versions, MD2 pin is fixed to pull-down resistor, and optionally selectable the resistor in other pins. • The MB90V670 has no pull-up/pull-down resistors.
G		• CMOS level hysteresis input (without standby control)
H		• CMOS level hysteresis input (without standby control) • Pull-up option selectable (without standby control) • No pull-up resistor in the MB90V670
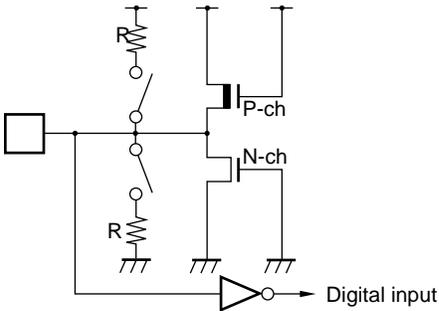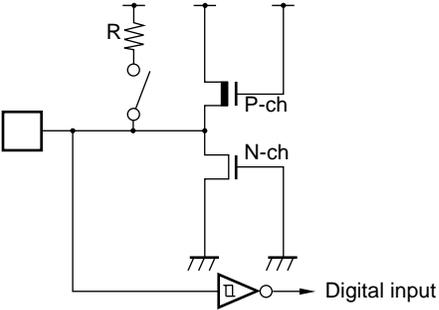
■ HANDLING DEVICES

1. Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS}.

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC}, AVRH) and analog input voltages not exceed the digital voltage (V_{CC}).

2. Connection of Unused Pins

Leaving unused pins open may result in abnormal operations. Clamp the pin level by connecting it to a pull-up or a pull-down resistor.

3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

• Using external clock

X0
Open — X1
MB90670/675 series
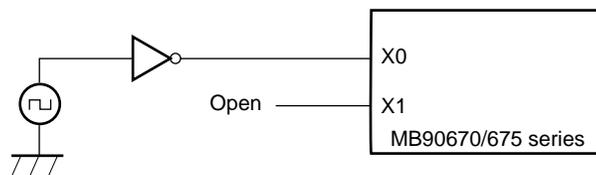
4. Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level and abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pin near the device.

5. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an grand area for stabilizing the operation.

6. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

7. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

8. "MOV @AL, AH", "MOVW @AL, AH" Instructions

When the above instruction is performed to I/O space, an unnecessary writing operation (#FF, #FFFF) may be performed in the internal bus.
Use the compiler function for inserting an NOP instruction before the above instructions to avoid the writing operation.
Accessing RAM space with the above instruction does not cause any problem.

9. Initialization

In the device, there are internal registers which is initialized only by a power-on reset. To initialize these registers, turning on the power again.

**10. Caution on operations during PLL clock mode**

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ PROGRAMMING TO THE ONE-TIME PROM ON THE MB90P673/P678

The MB90P673 and MB90P678 has a PROM mode for emulation operation of the MBM27C1000/1000A, to which writing codes by a general-purpose ROM writer can be done via a dedicated adapter. Please note that the device is not compatible with the electronic signature (device ID code) mode.

1. Writing Sequence

The memory map for the PROM mode is shown as follows. Write option data to the option setting area according by referring to "7. PROM Option Bit Map".

Normal operation mode	PROM mode
FFFFFF$_H$ — Program area (PROM)	1FFFFF$_H$ — Program area (PROM)
Address*2 —	Address*1 —
010000$_H$	
ROM image	
004000$_H$	0002C$_H$ — Option setting area
000000$_H$	00000$_H$

Type	Address*1	Address*2	Number of bytes
MB90P673	14000$_H$	FF4000$_H$	48 Kbytes
MB90P678	10000$_H$	FF0000$_H$	64 Kbytes

Note: The ROM image size for bank 00 is 48 Kbytes (ROM image for between FF4000$_H$ to FFFFFF$_H$).
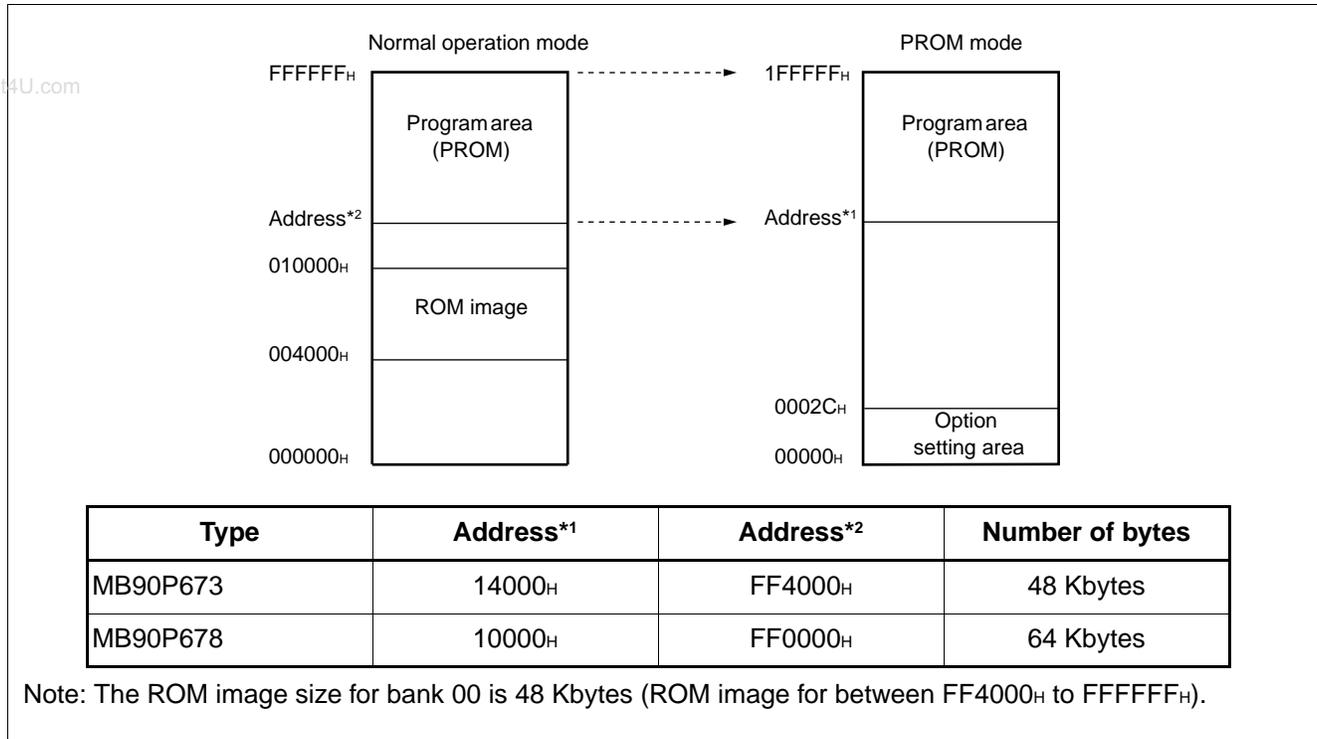
Write data to the one-time PROM microcontrollers according to the following sequence.

(1) Set the PROM programer to select the MBM27C1000/1000A.

(2) Load the program data to the ROM programer address *1 to 1FFFF$_H$. To select a PROM option, load the option data from 00000$_H$ to 0002C$_H$ referring to "7. PROM Option Bit Map".

(3) Set the chip to the adapter socket and load the socket to the ROM programer. Make sure that the device and adapter socket are properly oriented.

(4) Program from 00000$_H$ to 1FFFF$_H$.

Notes:
• In mask-ROM products, there is no PROM mode and it is impossible to read data by a ROM programer.
• Contact sales personnel when purchasing a ROM programer.

2. Program Mode

In the MB90P673/P678, all the bits are set to "1" upon shipping from FUJITSU or erasing operation. To write data, set desired bit selectively to "0". However it is impossible to write electronically to the bits.

3. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked One-time PROM microcomputer program.

```
┌─────────────────────────┐
│     Program, verify     │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│          Aging          │
│      +150°C, 48 h       │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│    Data verification    │
└─────────────────────────┘
            │
            ▼
   (      Assembly      )
```
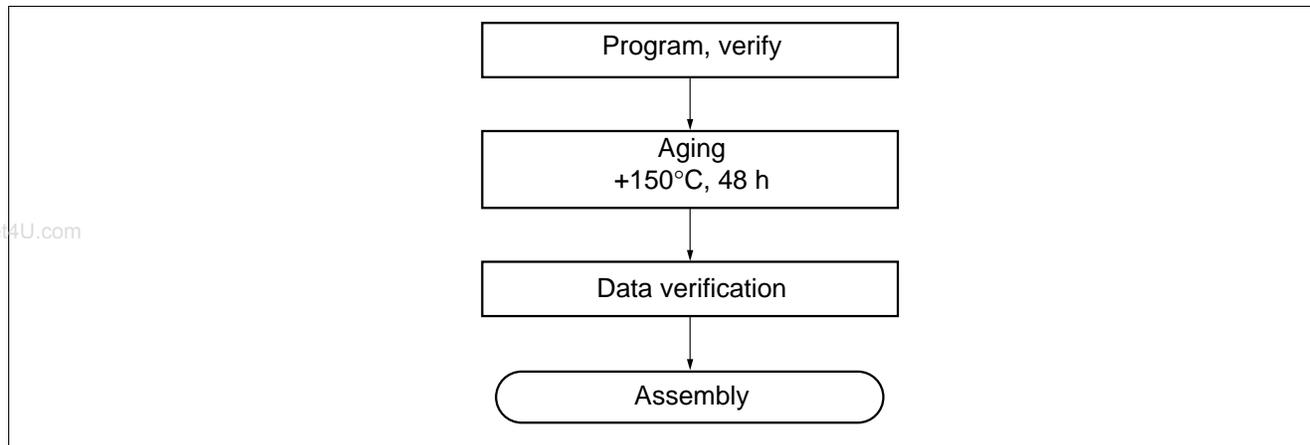
4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked One-time PROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

5. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part no.		MB90P673PF	MB90P673PFV	MB90P678PF	MB90P678PFV
Package		QFP-80	LQFP-80	QFP-100	LQFP-100
Compatible socket adapter Sun Hayato Co., Ltd.		ROM-80QF-32DP-16L	ROM-80SQF-32DP-16L	ROM-100QF-32DP-16L	ROM-100SQF-32DP-16L
Recommended programmer manufacturer and programmer name	Minato Electronics Inc.				
	1890A	—	—	—	Recommended
	1891	—	—	—	Recommended
	1930	—	—	—	Recommended
	Data I/O Co., Ltd.				
	UNISITE	—	—	—	Recommended
	3900	—	—	—	Recommended
	2900	—	—	—	Recommended

Inquiry: San Hayato Co., Ltd.: TEL: (81)-3-3986-0403
                                 FAX: (81)-3-5396-9106

Minato Electronics Inc.: TEL: USA (1)-916-348-6066
                          JAPAN (81)-45-591-5611

Data I/O Co., Ltd.: TEL: USA/ASIA (1)-206-881-6444
                     EUROPE (49)-8-985-8580

6. Pin Assignment for EPROM Mode

- MBM27C1000/1000A pin compatible

MBM27C1000/1000A		MB90P673/MB90P678	
Pin no.	Pin name	Pin no.	Pin name
1	V_{PP}	Refer to pin assignments.	MD2
2	OE		P32
3	A15		P17
4	A12		P14
5	A07		P27
6	A06		P26
7	A05		P25
8	A04		P24
9	A03		P23
10	A02		P22
11	A01		P21
12	A00		P20
13	D00		P00
14	D01		P01
15	D02		P02
16	GND		V_{SS}

MBM27C1000/1000A		MB90P673/MB90P678	
Pin no.	Pin name	Pin no.	Pin name
32	V_{CC}	Refer to pin assignments.	V_{CC}
31	PGM		P33
30	N.C.		—
29	A14		P16
28	A13		P15
27	A08		P10
26	A09		P11
25	A11		P13
24	A16		P30
23	A10		P12
22	CE		P31
21	D07		P07
20	D06		P06
19	D05		P05
18	D04		P04
17	D03		P03

- Pin assignments for products not compatible with MBM27C1000/1000A

Pin no.	Pin name	processing
Refer to pin assignments.	MD0 MD1 X0	Connect a pull-up resistor of 4.7 kΩ.
	X1	OPEN
	AV_{CC} AVRH P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 P80 to P86 P90 P91 PA0 to PA7 PB0 to PB2	Connect a pull-up resistor having a resistance of approximately 1 MΩ to each pin.

- Power supply, GND connected pin

Type	Pin no.	Pin name
Power supply	Refer to pin assignments.	$\overline{HST}$ V_{CC}
GND	Refer to pin assignments.	P34 P35 P36 $\overline{RST}$ AVRL AV_{SS} V_{SS}

Note: Only MB90675 series has P81 to P86, P90, P91, PA0 to PA7, PB0 to PB2 pins.

7. PROM Option Bit Map

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00000_H	Vacancy	$\overline{RST}$ Pull-up 1: No 0: Yes	Vacancy	MD1 Pull-up 1: No 0: Yes	MD1 Pull-down 1: No 0: Yes	MD0 Pull-up 1: No 0: Yes	MD0 Pull-down 1: No 0: Yes	Vacancy
00004_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
00008_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0000C_H	P27 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
00010_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
00014_H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0001C_H	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
00020_H	P77 Pull-up 1: No 0: Yes	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
00024_H	Vacancy	P86 Pull-up 1: No 0: Yes	P85 Pull-up 1: No 0: Yes	P84 Pull-up 1: No 0: Yes	P83 Pull-up 1: No 0: Yes	P82 Pull-up 1: No 0: Yes	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes
00028_H	PA5 Pull-up 1: No 0: Yes	PA4 Pull-up 1: No 0: Yes	PA3 Pull-up 1: No 0: Yes	PA2 Pull-up 1: No 0: Yes	PA1 Pull-up 1: No 0: Yes	PA0 Pull-up 1: No 0: Yes	Vacancy	Vacancy
0002C_H	Vacancy	Vacancy	Vacancy	PB2 Pull-up 1: No 0: Yes	PB1 Pull-up 1: No 0: Yes	PB0 Pull-up 1: No 0: Yes	PA7 Pull-up 1: No 0: Yes	PA6 Pull-up 1: No 0: Yes

Notes:
- Data "1" must be programed to the reserved bits and address other than listed above.
- Only MB90P678 has pull-up options for P81 to P86, PA0 to PA7, and PB0 to PB2 pins.
- Data "1" must be programed for the MB90P673.

■ BLOCK DIAGRAM
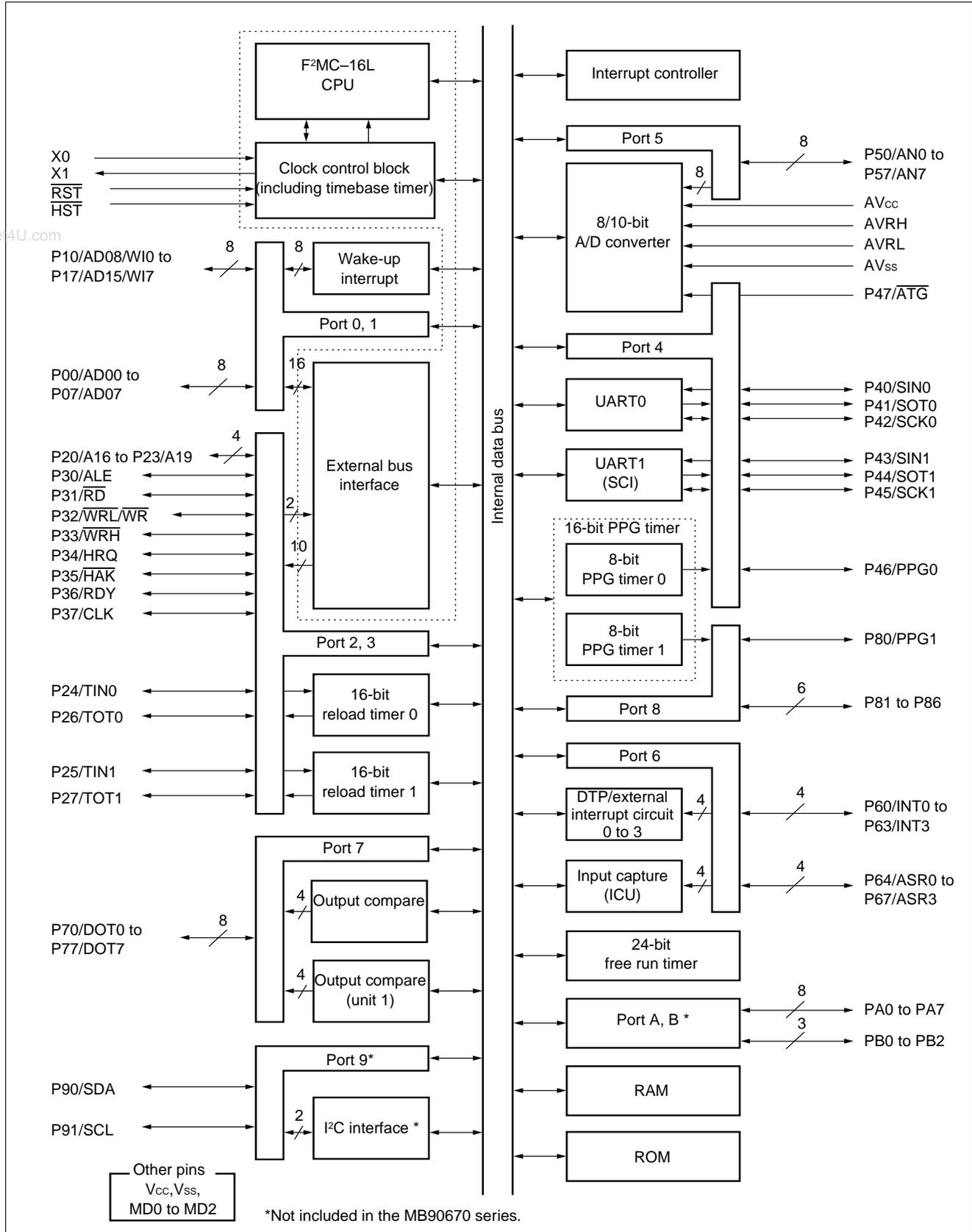
*Not included in the MB90670 series.

■ MEMORY MAP
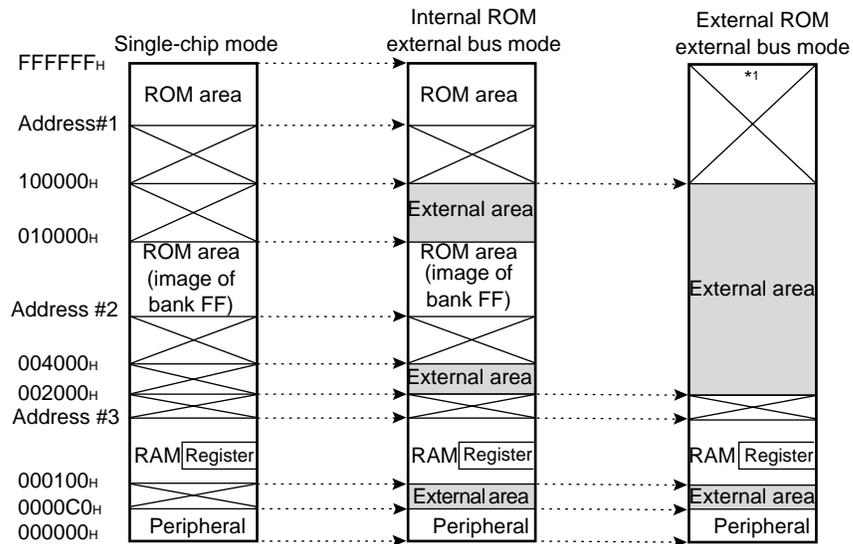
Part number	Address #1*2	Address #2*2	Address #3*2
MB90671	FFC000H	00C000H	000380H
MB90672	FF8000H	008000H	000780H
MB90673	FF4000H	004000H	000900H
MB90T673	—	—	000900H
MB90P673	FF4000H	004000H	000900H
MB90676	FF8000H	008000H	000780H
MB90677	FF4000H	004000H	000900H
MB90678	FF0000H	004000H	000D00H
MB90T678	—	—	000D00H
MB90P678	FF0000H	004000H	000D00H

☐ : Internal access memory

▨ : External access memory

⊠ : Inhibited area

*1: The same external memory is accessed for bank 0F, 1F, 2F through FF.
*2: Addresses #1, #2 and #3 are unique to the product type.

Notes:
- The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 is assigned to the same address, enabling reference of the table on the ROM without stating "far".
  However, the ROM area of the MB90678/P678 exceeds 48 Kbytes, and for this reason, the image from FF4000H to FFFFFFH is reflected on bank 00 and image from FF0000H to FF3FFFH bank FF only.
- In the MB90670/675 series, the upper 4-bit of the address are not output to the external bus. For this reason, the maximum area accessible is 1 Mbyte. The same address is accessed through different banks in different images.
  For example, accessing "A00000H" and "B00000H" accesses the same address on the external bus.
- To prevent the memory or I/O from being accessed through images, and the data from being destroyed, it is recommended to limit number of banks to a maximum of 16 so that the banks are mapped without interfering each other. Caution must be also taken when masking the upper address with the external address output control register (HACR).

# ■ F2MC-16L CPU PROGRAMMING MODEL

(1) Dedicated Registers

AH	AL

: Accumulator (A)
Dual 16-bit register used for storing results of calculation etc. The two 16-bit registers can be combined to be used as a 32-bit register.

USP

: User stack pointer (USP)
The 16-bit pointer indicating a user stack address.

SSP

: System stack pointer (SSP)
The 16-bit pointer indicating the status of the system stack address.

PS

: Processor status (PS)
The 16-bit register indicating the system status.

PC

: Program counter (PC)
The 16-bit register indicating storing location of the current instruction code.

DPR

: Direct page register (DPR)
The 8-bit register for specifying bit 8 through 15 of the operand address in the short direct addressing mode.

PCB

: Program bank register (PCB)
The 8-bit register indicating the program space.

DTB

: Data bank register (DTB)
The 8-bit register indicating the data space.

USB

: User stack bank register (USB)
The 8-bit register indicating the user stack space.

SSB

: System stack bank register (SSB)
The 8-bit register indicating the system stack space.

ADB

: Additional data bank register (ADB)
The 8-bit register indicating the additional space.

←— 8-bit —→
←————— 16-bit —————→
←——————— 32-bit ———————→

(2) General-purpose Registers

Maximum of 32 banks

R7	R6
R5	R4
R3	R2
R1	R0
RW3	
RW2	
RW1	
RW0	

RW7
RW6
RW5
RW4

RL3
RL2
RL1
RL0

$000180_H + (RP \times 10_H) \longrightarrow$

16-bit

. . .

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(3) Processor Status (PS)

	ILM			RP				CCR							
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PS	ILM2	ILM1	ILM0	B4	B3	B2	B1	B0	—	I	S	T	N	Z	V	C
Initial value	0	0	0	0	0	0	0	0	—	0	1	X	X	X	X	X

— : Unused
X : Indeterminate

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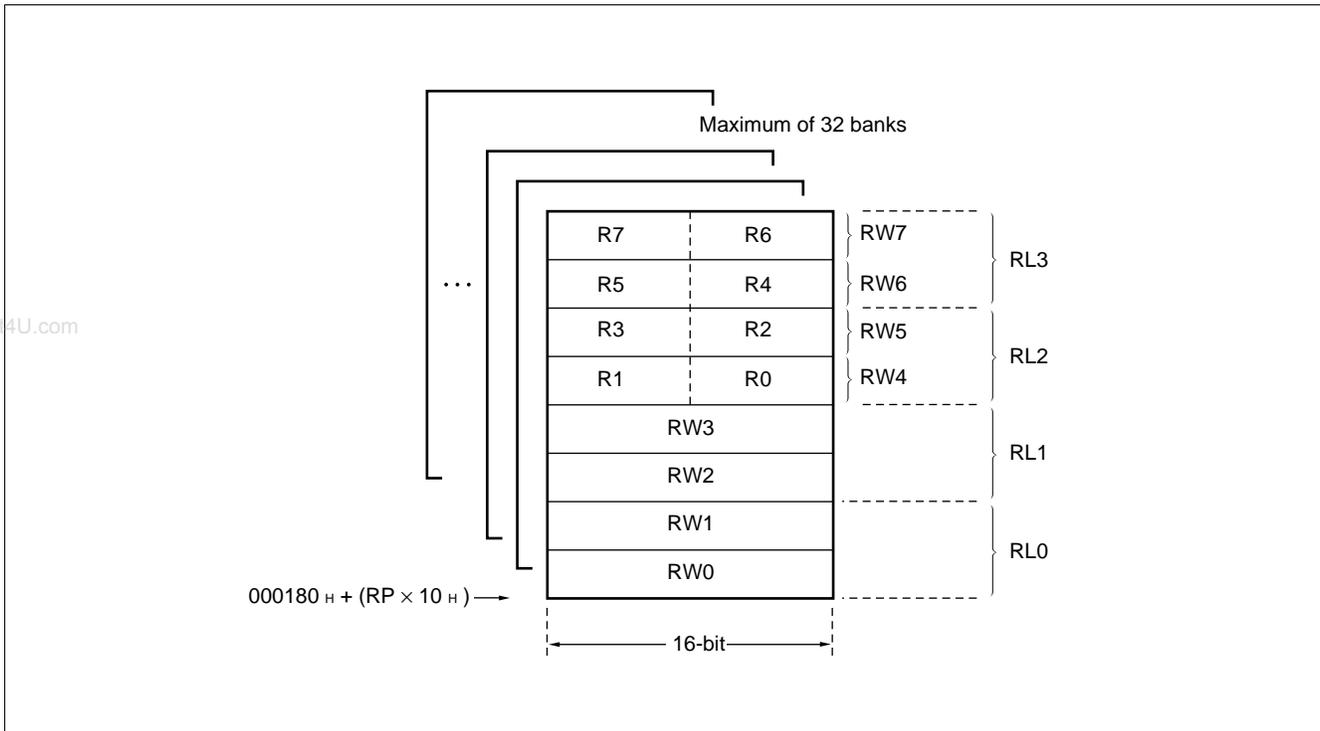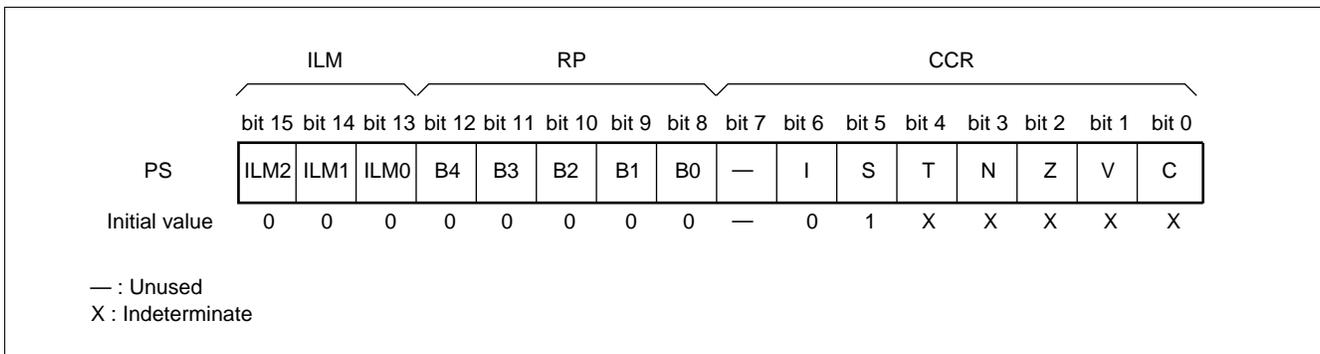
■ I/O MAP

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000000$_H$	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXX$_B$
000001$_H$	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX$_B$
000002$_H$	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX$_B$
000003$_H$	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX$_B$
000004$_H$	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX$_B$
000005$_H$	PDR5	Port 5 data register	R/W	Port 5	1 1 1 11 1 1 1$_B$
000006$_H$	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXX$_B$
000007$_H$	PDR7	Port 7 data register	R	Port 7	XXXXXXXX$_B$
000008$_H$	PDR8	Port 8 data register	R/W	Port 8*[5]	–XXXXXXX$_B$
000009$_H$	PDR9	Port 9 data register	R/W	Port 9*[5]	– – – – – – 1 1 $_B$
00000A$_H$	PDRA	Port A data register	R/W	Port A*[5]	XXXXXXXX$_B$
00000B$_H$	PDRB	Port B data register	R/W	Port B*[5]	– – – – – XXX$_B$
00000C$_H$ to 00000E$_H$		(Vacancy)*[3]			
00000F$_H$	EIFR	Wake-up interrupt flag register	R/W	Wake-up interrupt	– – – – – – – 0$_B$
000010$_H$	DDR0	Port 0 data direction register	R/W	Port 0	00000000$_B$
000011$_H$	DDR1	Port 1 data direction register	R/W	Port 1	00000000$_B$
000012$_H$	DDR2	Port 2 data direction register	R/W	Port 2	00000000$_B$
000013$_H$	DDR3	Port 3 data direction register	R/W	Port 3	00000000$_B$
000014$_H$	DDR4	Port 4 data direction register	R/W	Port 4	00000000$_B$
000015$_H$	ADER	Analog input enable register	R/W	Port 5, analog input	11111111$_B$
000016$_H$	DDR6	Port 6 data direction register	R/W	Port 6	00000000$_B$
000017$_H$	DDR7	Port 7 data direction register	R/W	Port 7	00000000$_B$
000018$_H$	DDR8	Port 8 data direction register	R/W	Port 8*[5]	–0000000$_B$
000019$_H$		(Vacancy)*[3]			
00001A$_H$	DDRA	Port A data direction register	R/W	Port A*[5]	00000000$_B$
00001B$_H$	DDRB	Port B data direction register	R/W	Port B*[5]	– – – – – 000$_B$
00001C$_H$ to 00001E$_H$		(Vacancy)*[3]			
00001F$_H$	EICR	Wake-up interrupt enable register	W	Wake-up interrupt	00000000$_B$

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
000020H	UMC0	Mode control register 0	R/W!	UART0	00000100B
000021H	USR0	Status register 0	R/W!		00010000B
000022H	UIDR0/ UODR0	Input data register 0/ output data register 0	R/W		XXXXXXXXB
000023H	URD0	Rate and data register 0	R/W		00000000B
000024H	SMR1	Mode register 1	R/W	UART1 (SCI)	00000000B
000025H	SCR1	Control register 1	R/W!		00000100B
000026H	SIDR1/ SODR1	Input data register 1/ output data register 1	R/W		XXXXXXXXB
000027H	SSR1	Status register 1	R/W!		00001–00B
000028H	ENIR	DTP/interrupt enable register	R/W	DTP/external in-terrupt circuit	– – – – 0000B
000029H	EIRR	DTP/interrupt factor register	R/W		– – – – 0000B
00002AH	ELVR	Request level setting register	R/W		00000000B
00002BH	(Vacancy)*3				
00002CH	ADCS	A/D convertor control status reg-ister	R/W!	8/10-bit A/D converter	00000000B
00002DH					00000000B
00002EH	ADCR	A/D convertor data register	R/W!*4		XXXXXXXXB
00002FH					000000XXB
000030H	PPGC0	PPG0 operating mode control register	R/W!	8/16-bit PPG timer 0	0–000001B
000031H	PPGC1	PPG1 operating mode control register	R/W!	8/16-bit PPG timer 1	00000000B
000032H	(Vacancy)*3				
000033H					
000034H	PRLL0	PPG0 reload register	R/W	8/16-bit PPG timer 0	XXXXXXXXB
000035H	PRLH0		R/W		XXXXXXXXB
000036H	PRLL1	PPG1 reload register	R/W	8/16-bit PPG timer 1	XXXXXXXXB
000037H	PRLH1		R/W		XXXXXXXXB
000038H	TMCSR0	Timer control status register 0	R/W!	16-bit reload timer 0	00000000B
000039H					– – – – 0000B
00003AH	TMR0/ TMRLR0	16-bit timer register 0/ 16-bit reload register 0	R/W		XXXXXXXXB
00003BH					XXXXXXXXB
00003CH	TMCSR1	Timer control status register 1	R/W!	16-bit reload timer 1	00000000B
00003DH					– – – – 0000B
00003EH	TMR1/ TMRLR1	16-bit timer register 1/ 16-bit reload register 1	R/W		XXXXXXXXB
00003FH					XXXXXXXXB

(Continued)

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000040_H	IBSR	I^2C bus status register	R	I^2C interface*6	00000000_B
000041_H	IBCR	I^2C bus control register	R/W		00000000_B
000042_H	ICCR	I^2C bus clock control register	R/W		$- - 0XXXXX_B$
000043_H	IADR	I^2C bus address register	R/W		$-XXXXXXX_B$
000044_H	IDAR	I^2C bus data register	R/W		$XXXXXXXX_B$
000045_H to $00004F_H$	(Vacancy)*3				
000050_H	TCCR	Free-run timer control register	R/W!	24-bit free-run timer	11000000_B
000051_H					$- - 111111_B$
000052_H	ICC	ICU control register	R/W	Input capture (ICU)	00000000_B
000053_H					00000000_B
000054_H	TCRL	Free-run timer lower data register	R	24-bit free-run timer	00000000_B
000055_H					00000000_B
000056_H	TCRH	Free-run timer upper data register	R		00000000_B
000057_H					00000000_B
000058_H	CCR00	OCU control register 00	R/W	Output compare (OCU) (unit 0)	11110000_B
000059_H					$- - - - 0000_B$
$00005A_H$	CCR01	OCU control register 01	R/W		$- - - - 0000_B$
$00005B_H$					00000000_B
$00005C_H$	CCR10	OCU control register 10	R/W	Output compare (OCU) (unit 1)	11110000_B
$00005D_H$					$- - - - 0000_B$
$00005E_H$	CCR11	OCU control register 11	R/W		$- - - - 0000_B$
$00005F_H$					00000000_B
000060_H	ICDR0L	ICU lower data register 0	R	Input capture (ICU)	$XXXXXXXX_B$
000061_H					$XXXXXXXX_B$
000062_H	ICDR0H	ICU upper data register 0	R		$XXXXXXXX_B$
000063_H					00000000_B
000064_H	ICDR1L	ICU lower data register 1	R		$XXXXXXXX_B$
000065_H					$XXXXXXXX_B$
000066_H	ICDR1H	ICU upper data register 1	R		$XXXXXXXX_B$
000067_H					00000000_B
000068_H	ICDR2L	ICU lower data register 2	R		$XXXXXXXX_B$
000069_H					$XXXXXXXX_B$

(Continued)

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
00006A$_H$	ICDR2H	ICU upper data register 2	R	Input capture (ICU)	XXXXXXXX$_B$
00006B$_H$					00000000$_B$
00006C$_H$	ICDR3L	ICU lower data register 3	R		XXXXXXXX$_B$
00006D$_H$					XXXXXXXX$_B$
00006E$_H$	ICDR3H	ICU upper data register 3	R		XXXXXXXX$_B$
00006F$_H$					00000000$_B$
000070$_H$	CPR00L	OCU compare lower data register 0	R/W	Output compare (OCU) (unit 0)	00000000$_B$
000071$_H$					00000000$_B$
000072$_H$	CPR00H	OCU compare upper data register 0	R/W		00000000$_B$
000073$_H$					00000000$_B$
000074$_H$	CPR01L	OCU compare lower data register 1	R/W		00000000$_B$
000075$_H$					00000000$_B$
000076$_H$	CPR01H	OCU compare upper data register 1	R/W		00000000$_B$
000077$_H$					00000000$_B$
000078$_H$	CPR02L	OCU compare lower data register 2	R/W		00000000$_B$
000079$_H$					00000000$_B$
00007A$_H$	CPR02H	OCU compare upper data register 2	R/W		00000000$_B$
00007B$_H$					00000000$_B$
00007C$_H$	CPR03L	OCU compare lower data register 3	R/W		00000000$_B$
00007D$_H$					00000000$_B$
00007E$_H$	CPR03H	OCU compare upper data register 3	R/W		00000000$_B$
00007F$_H$					00000000$_B$
000080$_H$	CPR04L	OCU compare lower data register 4	R/W	Output compare (OCU) (unit 1)	00000000$_B$
000081$_H$					00000000$_B$
000082$_H$	CPR04H	OCU compare upper data register 4	R/W		00000000$_B$
000083$_H$					00000000$_B$
000084$_H$	CPR05L	OCU compare lower data register 5	R/W		00000000$_B$
000085$_H$					00000000$_B$
000086$_H$	CPR05H	OCU compare upper data register 5	R/W		00000000$_B$
000087$_H$					00000000$_B$
000088$_H$	CPR06L	OCU compare lower data register 6	R/W		00000000$_B$
000089$_H$					00000000$_B$
00008A$_H$	CPR06H	OCU compare upper data register 6	R/W		00000000$_B$
00008B$_H$					00000000$_B$

(Continued)

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Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
00008C$_H$	CPR07L	OCU compare lower data register 7	R/W	Output compare (OCU) (unit 1)	00000000$_B$
00008D$_H$					00000000$_B$
00008E$_H$	CPR07H	OCU compare upper data register 7	R/W		00000000$_B$
00008F$_H$					00000000$_B$
000090$_H$ to 00009E$_H$		(System reservation area)*1			
00009F$_H$	DIRR	Delayed interrupt factor generation/ cancellation register	R/W	Delayed interrupt generation module	– – – – – – – 0$_B$
0000A0$_H$	LPMCR	Low-power consumption mode control register	R/W!	Low-power consumption (stand-by) mode	00011000$_B$
0000A1$_H$	CKSCR	Clock selection register	R/W!	Low-power consumption (stand-by) mode	11111100$_B$
0000A2$_H$ to 0000A4$_H$		(Vacancy)*3			
0000A5$_H$	ARSR	Automatic ready function select register	W	External bus pin	0011 – – 00$_B$
0000A6$_H$	HACR	Upper address control register	W	External bus pin	– – – – 0000$_B$
0000A7$_H$	EPCR	Bus control signal select register	W	External bus pin	0000*00–$_B$
0000A8$_H$	WDTC	Watchdog timer control register	R/W!	Watchdog timer	XXXXX111$_B$
0000A9$_H$	TBTC	Timebase timer control register	R/W!	Timebase timer	1 – – 00100$_B$
0000AA$_H$ to 0000AF$_H$		(Vacancy)*3			
0000B0$_H$	ICR00	Interrupt control register 00	R/W!	Interrupt controller	00000111$_B$
0000B1$_H$	ICR01	Interrupt control register 01	R/W!		00000111$_B$
0000B2$_H$	ICR02	Interrupt control register 02	R/W!		00000111$_B$
0000B3$_H$	ICR03	Interrupt control register 03	R/W!		00000111$_B$
0000B4$_H$	ICR04	Interrupt control register 04	R/W!		00000111$_B$
0000B5$_H$	ICR05	Interrupt control register 05	R/W!		00000111$_B$
0000B6$_H$	ICR06	Interrupt control register 06	R/W!		00000111$_B$
0000B7$_H$	ICR07	Interrupt control register 07	R/W!		00000111$_B$
0000B8$_H$	ICR08	Interrupt control register 08	R/W!		00000111$_B$
0000B9$_H$	ICR09	Interrupt control register 09	R/W!		00000111$_B$

(Continued)

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
0000BA$_H$	ICR10	Interrupt control register 10	R/W!		00000111$_B$
0000BB$_H$	ICR11	Interrupt control register 11	R/W!		00000111$_B$
0000BC$_H$	ICR12	Interrupt control register 12	R/W!	Interrupt controller	00000111$_B$
0000BD$_H$	ICR13	Interrupt control register 13	R/W!		00000111$_B$
0000BE$_H$	ICR14	Interrupt control register 14	R/W!		00000111$_B$
0000BF$_H$	ICR15	Interrupt control register 15	R/W!		00000111$_B$
0000C0$_H$ to 0000FF$_H$		(External area)*2			

Descriptions for read/write

R/W: Readable and writable
R: Read only
W: Write only
R/W!: Bits for reading operation only or writing operation only are included. Refer to the register lists for specific resource for detailed information.

Descriptions for initial value

0   : The initial value of this bit is "0".
1   : The initial value of this bit is "1".
*   : The initial value of this bit is "1" or "0" (decided by levels on pins of MD0 through MD2).
X   : The initial value of this bit is indeterminate.
–   : This bit is not used. The initial value is indeterminate.

*1: Access prohibited.

*2: This area is the only external access area having an address of 0000FF$_H$ or lower. An access operation to this area is handled as that to external I/O area.

*3: The area corresponding to the "(Vacancy)" on the I/O map is reserved, and accessing operation to this area is handled as that to internal area. No access signal to external devices are generated.

*4: Only bit 15 is writable. Reading bit 10 through bit 15 returns "0" as a reading result.

*5: In the MB90670 series, P81 through P86, P90, P91, PA0 through PA7, PB0 through PB2 are not present. For this reason, bits corresponding to these pins are not used.

*6: The MB90670 series does not have the I^{2}C interface. For this reason, this area is "(Vacancy)" in the MB90670 series.

Note: For bits that is only allowed to program, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.
For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt source	EI²OS support	Interrupt vector		Interrupt control register		Priority*4
		Number	Address	ICR	Address	
Reset	×	# 08	08_H	$FFFFDC_H$	—	—	High
INT9 instruction	×	# 09	09_H	$FFFFD8_H$	—	—	
Exception	×	# 10	$0A_H$	$FFFFD4_H$	—	—	
DTP/external interrupt circuit Channel 0	△	# 11	$0B_H$	$FFFFD0_H$	ICR00	$0000B0_H$*2	
DTP/external interrupt circuit Channel 1	△	# 12	$0C_H$	$FFFFCC_H$			
DTP/external interrupt circuit Channel 2	△	# 13	$0D_H$	$FFFFC8_H$	ICR01	$0000B1_H$*2	
DTP/external interrupt circuit Channel 3	△	# 14	$0E_H$	$FFFFC4_H$			
Output compare Channel 0	△	# 15	$0F_H$	$FFFFC0_H$	ICR02	$0000B2_H$*2	
Output compare Channel 1	△	# 16	10_H	$FFFFBC_H$			
Output compare Channel 2	△	# 17	11_H	$FFFFB8_H$	ICR03	$0000B3_H$*2	
Output compare Channel 3	△	# 18	12_H	$FFFFB4_H$			
Output compare Channel 4	△	# 19	13_H	$FFFFB0_H$	ICR04	$0000B4_H$*2	
Output compare Channel 5	△	# 20	14_H	$FFFFAC_H$			
Output compare Channel 6	△	# 21	15_H	$FFFFA8_H$	ICR05	$0000B5_H$*2	
Output compare Channel 7	△	# 22	16_H	$FFFFA4_H$			
24-bit free-run timer Overflow	△	# 23	17_H	$FFFFA0_H$	ICR06	$0000B6_H$*2	
24-bit free-run timer Intermediate bit	△	# 24	18_H	$FFFF9C_H$			
Input capture Channel 0	△	# 25	19_H	$FFFF98_H$	ICR07	$0000B7_H$*2	
Input capture Channel 1	△	# 26	$1A_H$	$FFFF94_H$			
Input capture Channel 2	△	# 27	$1B_H$	$FFFF90_H$	ICR08	$0000B8_H$*2	
Input capture Channel 3	△	# 28	$1C_H$	$FFFF8C_H$			
16-bit reload timer/ 8/16-bit PPG timer 0	△	# 29	$1D_H$	$FFFF88_H$	ICR09	$0000B9_H$*2, *3	
16-bit reload timer/ 8/16-bit PPG timer 1	△	# 30	$1E_H$	$FFFF84_H$			
8/10-bit A/D converter measurement complete	○	# 31	$1F_H$	$FFFF80_H$	ICR10	$0000BA_H$	
Wake-up interrupt	×	# 33	21_H	$FFFF78_H$	ICR11	$0000BB_H$*2	
Timebase timer interval interrupt	×	# 34	22_H	$FFFF74_H$			Low

(Continued)

(Continued)

Interrupt source	EI²OS support	Interrupt vector		Interrupt control register		Priority*4
		Number	Address	ICR	Address	
UART1 (SCI) transmission complete	△	# 35	23$_H$	FFFF70$_H$	ICR12	0000BC$_H$*2	High
UART0 transmission complete	△	# 36	24$_H$	FFFF6C$_H$			
UART1 (SCI) reception complete	◎	# 37	25$_H$	FFFF68$_H$	ICR13	0000BD$_H$*2	
I²C interface*1	×	# 38	26$_H$	FFFF64$_H$			
UART0 reception complete	◎	# 39	27$_H$	FFFF60$_H$	ICR14	0000BE$_H$	
Delayed interrupt generation module	×	# 42	2A$_H$	FFFF54$_H$	ICR15	0000BF$_H$	Low

○ : Can be used
× : Can not be used
◎ : Can be used. With EI²OS stop function.
△ : Can be used if interrupt request using ICR are not commonly used.

*1: In MB90670 series, this interrupt vector is not used because the series does not have the I²C interface.

*2: • Interrupt levels for peripherals that commonly use the ICR register are in the same level.

  • When the extended intelligent I/O service (EI²OS) is specified in a peripheral device commonly using the ICR register, only one of the functions can be used.

  • When the extended intelligent I/O service (EI²OS) is specified for one of the peripheral functions, interrupts can not be used on the other function.

*3: Only 16-bit reload timer conforms to the extended intelligent I/O service (EI²OS). Because the 8/16-bit PPG timer does not conform to the extended intelligent I/O service (EI²OS), disable interrupts of the 8/16-bit PPG timer when using the extended intelligent I/O service (EI²OS) in the 16-bit reload timer.

*4: The level shows priority of same level of interrupt invoked simultaneously.

■ PERIPHERALS

1. I/O Port

(1) Input/output Port

Port 0 to 4, 6, 8, A, and B are general-purpose I/O ports having a combined function as an external bus pin and a resource input. The input output ports function as general-purpose I/O port only in the single-chip mode. In the external bus mode, the ports are configured as external bus pins, and part of pins for port 3 can be configured as general-purpose I/O port by setting the bus control signal select register (ECSR). Each pin corresponding to upper 4-bit of the port 2 can be switched between a resource and a port bitwise.

Only MB90675 series has port A and port B.

- Operation as output port
  The pin is configured as an output port by setting the corresponding bit of the DDR register to "1".
  Writing data to PDR register when the port is configured as output, the data is retained in the output latch in the PDR and directly output to the pin.

  The value of the pin (the same value retained in the output latch of PDR) can be read out by reading the PDR register.

  Note: When a read-modify-write instruction (e.g. bit set instruction) is performed to the port data register, the destination bit of the operation is set to the specified value, not affecting the bits configured by the DDR register for output, however, values of bits configured by the DDR register as inputs are changed because input values to the pins are written into the output latch. To avoid this situation, configure the pins by the DDR register as output after writing output data to the PDR register when configuring the bit used as input as outputs.

- Operation as input port
  The pin is configured as an input by setting the corresponding bit of the DDR register to "0".
  When the pin is configured as an input, the output buffer is turned-off and the pin is put into a high-impedance status.
  When a data is written into the PDR register, the data is retained in the output latch of the PDR, but pin outputs are unaffected.
 Reading the PDR register reads out the pin level ("0" or "1")

- Block diagram

Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode
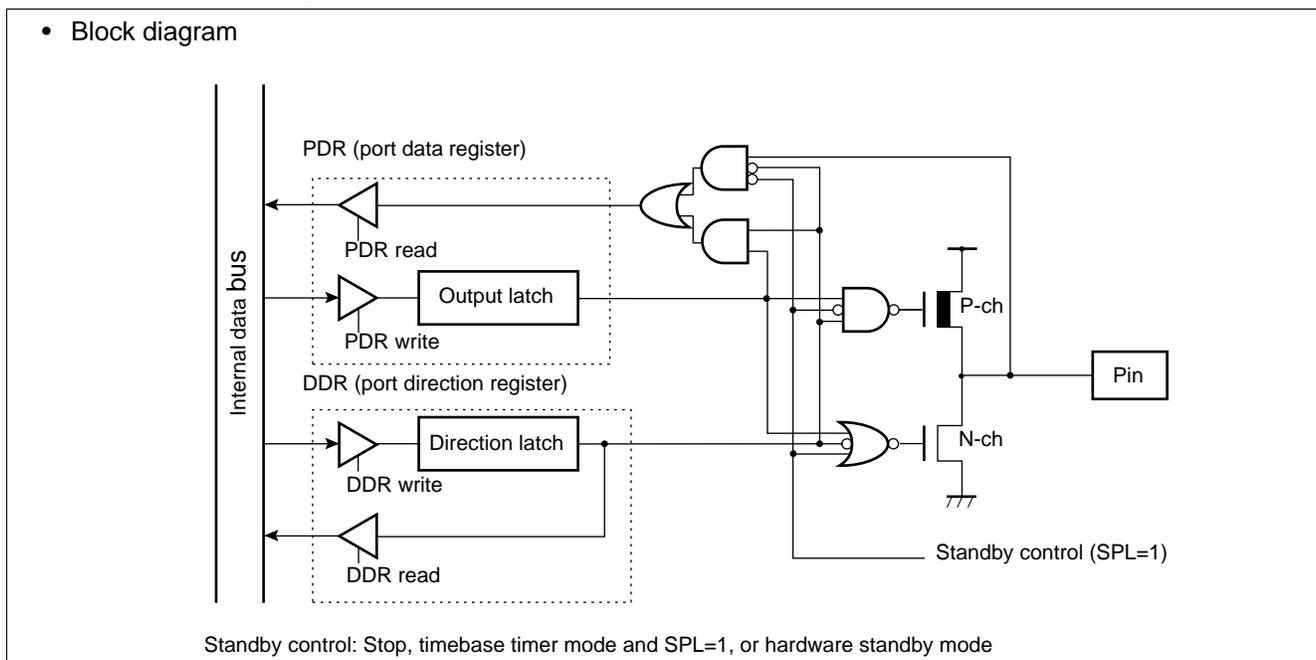
(2) N-ch Open-drain Port

Port 5 and port 9 are general-purpose I/O ports having a combined function as resource input/output. Each pin can be switched between resource and port bitwise.

Only MB90675 series has port 9.

- Operation as output port
  When a data is written into the PDR register, the data is latched to the output latch of PDR. When the output latch value is set to "0", the output transistor is turned on and the pin status is put into an "L" level output, while writing "1" turns off the transistor and put the pin in a high-impedance status.
  If the output pin is pulled-up, setting output latch value to "1" puts the pin in the pull-up status.
  Reading the PDR register returns the pin value (same as the output latch value in the PDR).

  Note: Execution of a read-modify-write instruction (e.g. bit set instruction) reads out the output latch value rather than the pin value, leaving output latch that is not manipulated unchanged.

- Operation as input port
  Setting corresponding bit of the PDR register to "1" turns off the output transistor and the pin is put into a high-impedance status.
  Reading the PDR register returns the pin level ("0" or "1").

- Block diagram of port 5
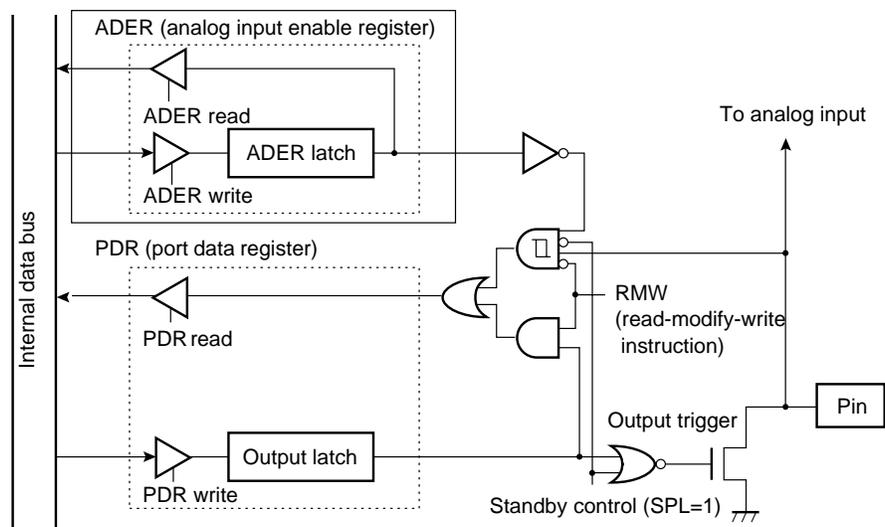
Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

- Block diagram of port 9
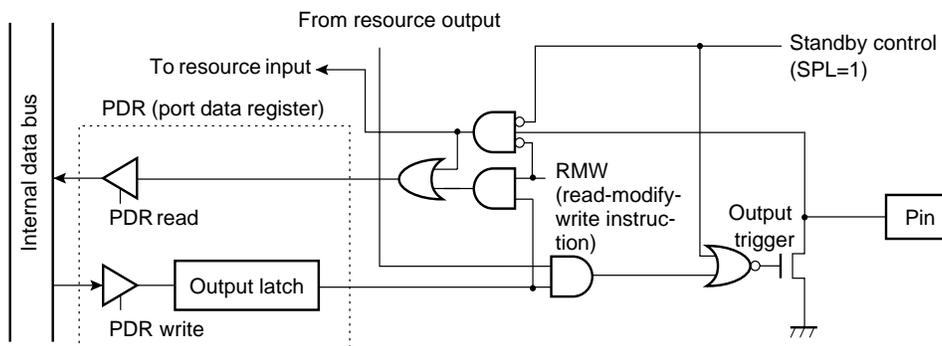
Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

(3) Output Port

Port 7 is a general-purpose output port having a combined function as an output compare (OCU) output. Note that only OCU output can be output when the pin is configured as an output, and it is not used for outputting given data by writing to the data register. Each pin can be switched between an output compare output and a port bitwise.

• Operation as output port (operation of OCU output)
Setting the corresponding bit of the DDR register to "1" configures the pin as an output port. In this case, lower 4-bit of CCR01 and CCR register are output.

When configured as an output, the output buffer is turned on and data retained in the output latch in the PDR of the output compare is output to the pin.

Writing data to DOT bit of the OCU control register (CCR01, CCR11) corresponding to each pin writes data in synchronization to a match operation of the output compare and output to the pin.

Reading the PDR register returns the pin level (same as the output latch value of the PDR).

When output of output compare is enabled, an output value from the output compare can be read out.

• Operation as input port
Setting corresponding bit of the DDR register to "0" configures the pin as input port.

When the pin is configured as an input port, the output buffer is turned off and the pin is put into a high-impedance status.

Reading the PDR register returns the pin level ("0" or "1").

• Block diagram
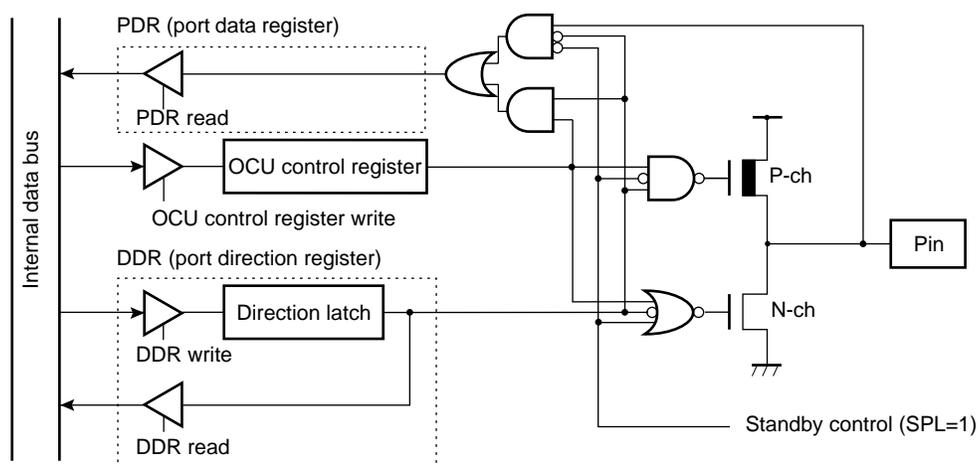
Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

(4) Register Configuration

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000000H	(PDR1)	P07	P06	P05	P04	P03	P02	P01	P00	Port 0 data register (PDR0)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	
000001H	P17	P16	P15	P14	P13	P12	P11	P10	(PDR0)	Port 1 data register (PDR1)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000002H	(PDR3)	P27	P26	P25	P24	P23	P22	P21	P20	Port 2 data register (PDR2)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	
000003H	P37	P36	P35	P34	P33	P32	P31	P30	(PDR2)	Port 3 data register (PDR3)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000004H	(PDR5)	P47	P46	P45	P44	P43	P42	P41	P40	Port 4 data register (PDR4)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	
000005H	P57	P56	P55	P54	P53	P52	P51	P50	(PDR4)	Port 5 data register (PDR5)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000006H	(PDR7)	P67	P66	P65	P64	P63	P62	P61	P60	Port 6 data register (PDR6)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	
000007H	P77	P76	P75	P74	P73	P72	P71	P70	(PDR6)	Port 7 data register (PDR7)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000008H	(PDR9)	—	P86	P85	P84	P83	P82	P81	P80	Port 8 data register (PDR8)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	
000009H	—	—	—	—	—	—	P91	P90	(PDR8)	Port 9 data register (PDR9)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
00000AH	(PDRB)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A data register (PDRA)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	
00000BH	—	—	—	—	—	PB2	PB1	PB0	(PDRA)	Port B data register (PDRB)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

(Continued)

(Continued)

Address	bit-15 . . . . bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000010H	(DDR1)	P07	P06	P05	P04	P03	P02	P01	P00	Port 0 data direction register (DDR0)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 . . . . bit 0	
000011H	P17	P16	P15	P14	P13	P12	P11	P10	(DDR0)	Port 1 data direction register (DDR1)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 . . . . bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000012H	(DDR3)	P27	P26	P25	P24	P23	P22	P21	P20	Port 2 data direction register (DDR2)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 . . . . bit 0	
000013H	P37	P36	P35	P34	P33	P32	P31	P30	(DDR2)	Port 3 data direction register (DDR3)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 . . . . bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000014H	(ADER)	P47	P46	P45	P44	P43	P42	P41	P40	Port 4 data direction register (DDR4)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 . . . . bit 0	
000015H	P57	P56	P55	P54	P53	P52	P51	P50	(DDR4)	Analog input enable register (ADER)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000016H	(DDR7)	P67	P66	P65	P64	P63	P62	P61	P60	Port 6 data direction register (DDR6)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	
000017H	P77	P76	P75	P74	P73	P72	P71	P70	(DDR6)	Port 7 data direction register (DDR7)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000018H	(Vacancy)	—	P86	P85	P84	P83	P82	P81	P80	Port 8 data direction register (DDR8)
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
00001AH	(DDRB)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A data direction register (DDRA)
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	
00001BH	—	—	—	—	—	PB2	PB1	PB0	(DDRA)	Port B data direction register (DDRB)
					R/W	R/W	R/W	R/W		

Note: Only MB90675 series has P81 through P86, P90, PA0 through PA7, and PB0 through PB2, and MB90670 series does not have such pins.

2. Timebase Timer

The timebase timer is a 18-bit free run counter (timebase counter) for counting up in synchronization to the internal count clock (divided-by-2 of oscillation) with an interval timer function for selecting an interval time from four types of 2^{12}/HCLK, 2^{14}/HCLK, 2^{16}/HCLK, and 2^{19}/HCLK.

The timebase timer also has a function for supplying operating clocks for the timer output for the oscillation stabilization time or the watchdog timer etc.

(1) Register Configuration

• Timebase timer control register (TBTC)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · ·bit 0	Initial value
0000A9$_H$	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0	(WDTC)	1--00100$_B$
	R/W	—	—	R/W	R/W	W	R/W	R/W		

R/W : Readable and writable
W : Read only
— : Unused

(2) Block Diagram

OF   : Overflow
HCLK : Oscillation clock
*1   : Switch machine clock from oscillation clock to PLL clock
*2   : Interrupt number
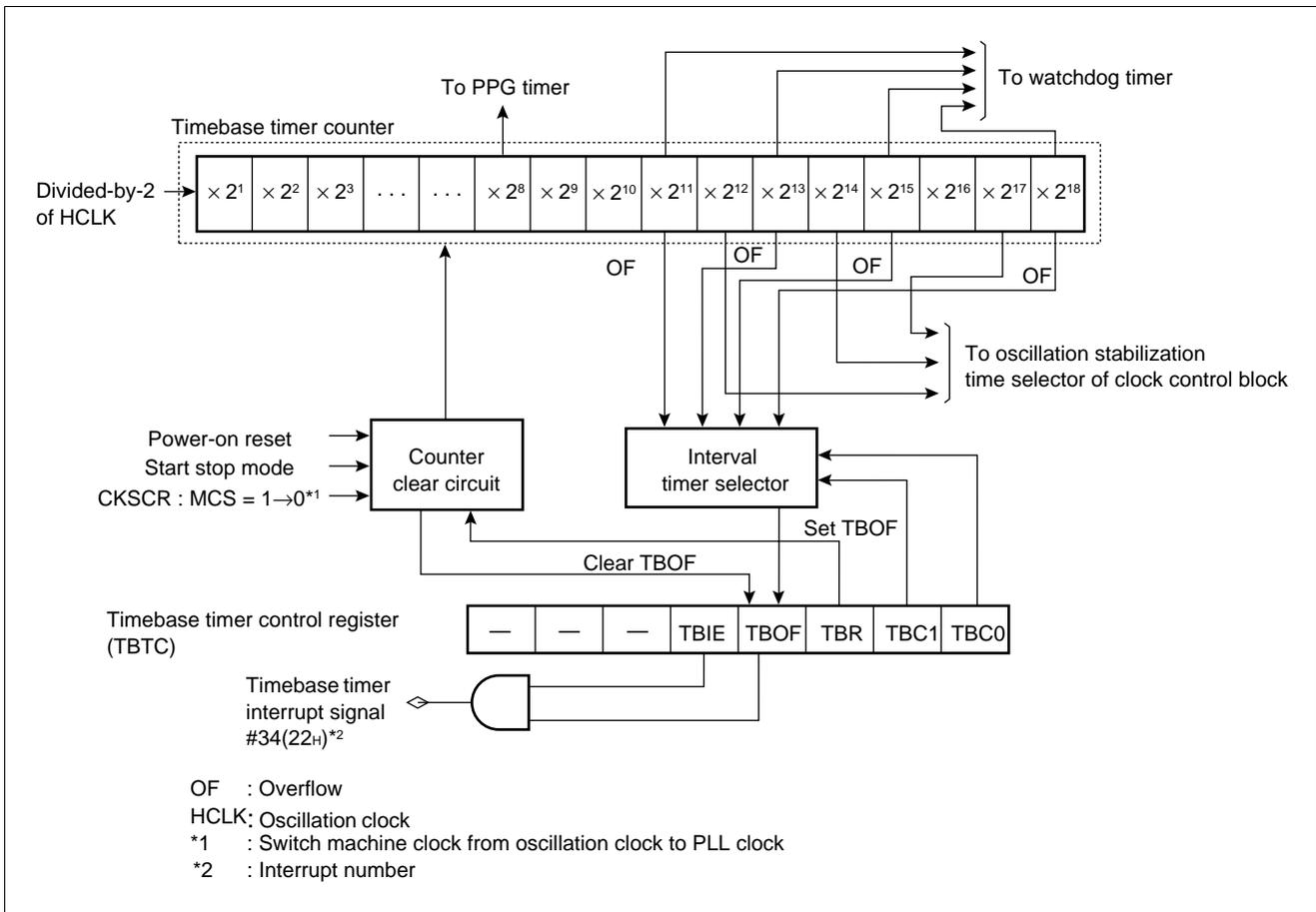
3. Watchdog Timer

The watchdog timer is a 2-bit counter operating with an output of the timebase timer and resets the CPU when the counter is not cleared for a preset period of time.

(1) Register Configuration

• Watchdog timer control register (WDTC)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A8$_H$	(TBTC)	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXX111$_B$
		R	R	R	R	R	W	W	W	

R : Read only
W : Write only
X : Indeterminate

(2) Block Diagram

Watchdog timer control register (WDTC)

| PONR | STBR | WRST | ERST | SRST | WTE | WT1 | WT0 |

2

Watchdog timer

Start sleep mode
Start hold status
Start stop mode

Counter clear control circuit → Count clock selector → 2-bit counter → Watchdog reset generation circuit → To internal reset generation circuit

CLR and start
Overflow
CLR
CLR

Clear
4

(Timebase timer counter)

Divided-by-2 of HCLK

$\times 2^1$ | $\times 2^2$ | · · · | $\times 2^8$ | $\times 2^9$ | $\times 2^{10}$ | $\times 2^{11}$ | $\times 2^{12}$ | $\times 2^{13}$ | $\times 2^{14}$ | $\times 2^{15}$ | $\times 2^{16}$ | $\times 2^{17}$ | $\times 2^{18}$

HCLK: Oscillation clock
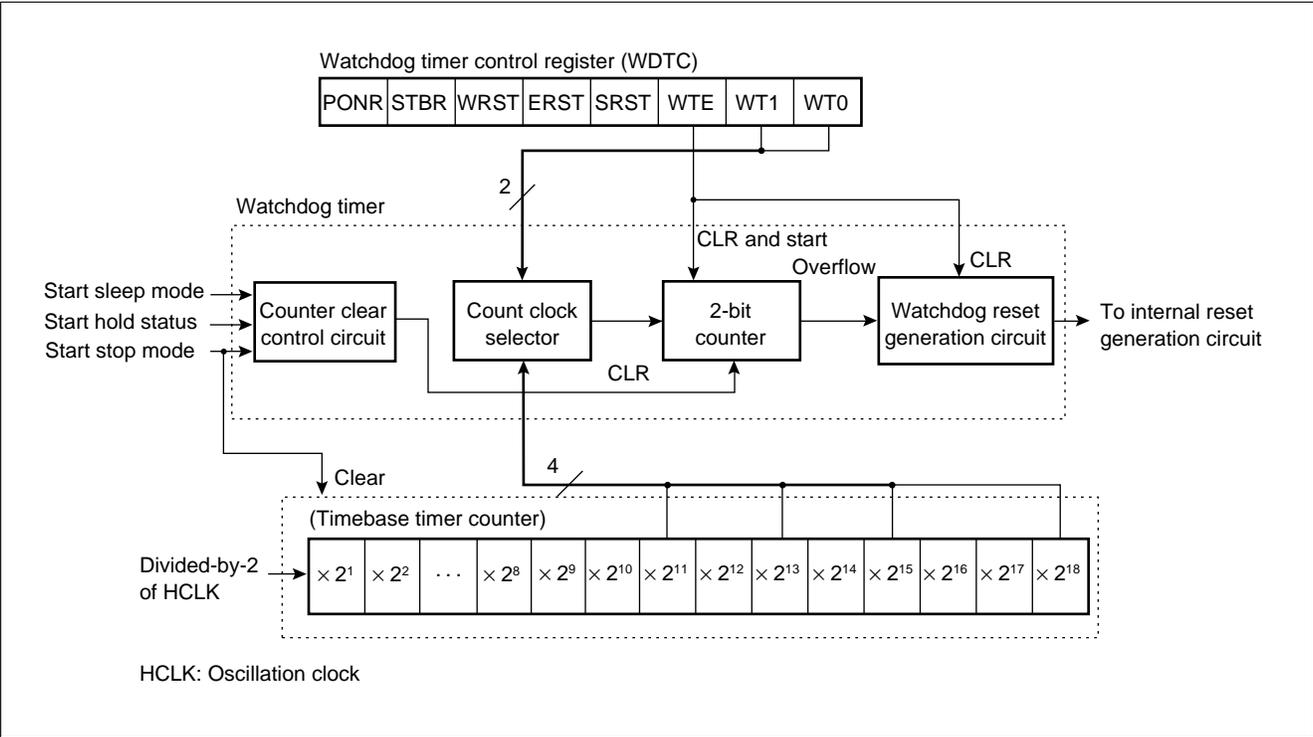
4. 8/16-bit PPG Timer

The 8/16-bit PPG timer is 2-channel reload timer module for outputting pulse having given frequencies/duty ratios.

The two modules performs the following operation by combining functions.
- 8-bit PPG output 2-channel independent operation mode
  This is a mode for operating independent 2-channel 8-bit PPG timer, in which PPG0 and PPG1 pins correspond to outputs from PPG0 and PPG1 respectively.
- 16-bit PPG output operation mode
  In this mode, PPG0 and PPG1 are combined to be operated as a 1-channel 8/16-bit PPG timer operating as a 16-bit timer. Because PPG0 and PPG1 outputs are reversed by an underflow from PPG1 outputting the same output pulses from PPG0 and PPG1 pins.
- 8 + 8-bit PPG output operation mode
  In this mode, PPG0 is operated as an 8-bit prescaler, in which an underflow output of PPG0 is used as a clock source for PPG1. A toggle output of PPG0 and PPG output of PPG1 are output from PPG0 and PPG1 respectively.

The module can also be used as a D/A converter with an external add-on circuit.

(1) Register Configuration

- PPG0 operating mode control register (PPGC0)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000030H	(PPGC1)	PEN0	—	POE0	PIE0	PUF0	PCM1	PCM0	RESV	0 - 000001 B
		R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG1 operating mode control register (PPGC 1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
000031H	PEN1	PCS1	POE1	PIE1	PUF1	MD1	MD0	RESV	(PPGC0)	00000001 B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- PPG reload register (PRLL0,PRLH0,PRLL1,PRLH1)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PRLH0:000035H PRLH1:000037H	(PRLH0,PRLH1)									XXXXXXXX B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
PRLL0:000034H PRLL1:000036H									(PRLL0,PRLL1)	XXXXXXXX B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

R/W : Readable and writable
— : Unused
X : Indeterminate

(2) Block Diagram
- Block diagram of 8/16-bit PPG timer 0

Data bus for "H" digits

Data bus for "L" digits

PPG0 reload register

PPG0 operating mode control register (PPGC0)

| PEN0 | — | POE0 | PIE0 | PUF0 | PCM1 | PCM0 | RESV |

PRLH0   PRLL0

Temporary buffer (PRLBH0)

R
S   Q

Interrupt request #29 (1D$_H$)*

Reload selector (L/H selector)

Select signal

2   Mode control signal

Count value   reload

Clear

PPG1 underflow
PPG0 underflow (to PPG1)

Pulse selector

Down counter (PCNT0)   Underflow

CLK

PPG0 output latch

Pin

P46/PPG0

Reverse

PPG output control circuit

Timebase timer output (512/HCLK)
Peripheral clock (16/φ)
Peripheral clock (4/φ)
Peripheral clock (1/φ)

Count clock selector

2

Select signal

* : Interrupt number
HCLK : Oscillation clock
φ : Machine clock frequency

• Block diagram of 8/16-bit PPG timer 1

* : Interrupt number
HCLK : Oscillation clock
ϕ : Machine clock frequency

5. 16-bit Reload Timer

The 16-bit reload timer has an internal clock mode for counting down in synchronization to three types of internal clocks and an event count mode for counting down detecting a given edge of the pulse input to the external bus pin, and either of the two functions can be selectively used.

For this timer, an "underflow" is defined as the counter value of "0000$_H$" to "FFFF$_H$". According to this definition, an underflow occurs after [reload register setting value + 1] counts.

In operating the counter, the reload mode for repeating counting operation after reloading a counter setting value after an underflow or the one-shot mode for stopping the counting operation after an underflow can be selectively used.

Because the timer can generate an interrupt upon an underflow, the timer conforms to the extended intelligent I/O service (EI^{2}OS).

The MB90670/675 series has 2 channels of 16-bit reload timers.

(1) Register Configuration

- Timer control status register upper digits (TMCSR0,TMCSR1 : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · · bit 0	Initial value
TMCSR0:000039$_H$ TMCSR1:00003D$_H$	—	—	—	—	CSL1	CSL0	MOD2	MOD1	(TMCSR : L)	- - - -0000$_B$
	—	—	—	—	R/W	R/W	R/W	R/W		

- Timer control status register lower digits (TMCSR0,TMCSR1 : L)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TMCSR0:000038$_H$ TMCSR1:00003C$_H$	(TMCSR : H)	MOD1	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- 16-bit timer register 0, 1 (TMR0,TMR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003A$_H$ 00003B$_H$ 00003E$_H$ 00003F$_H$	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	XXXXXXXX$_B$ XXXXXXXX$_B$ XXXXXXXX$_B$ XXXXXXXX$_B$

- 16-bit reload register 0, 1 (TMRL0,TMRL1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003A$_H$ 00003B$_H$ 00003E$_H$ 00003F$_H$	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	XXXXXXXX$_B$ XXXXXXXX$_B$ XXXXXXXX$_B$ XXXXXXXX$_B$

R/W : Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

(2) Block Diagram

Internal data bus

TMRLR0*1
<TMRLR1>

16-bit reload register

reload signal

reload control circuit

TMRR0*1
<TMR1>

16-bit timer register (down counter) UF

CLK

Count clock generation circuit

Prescaler

φ

3

Gate input

Valid clock decision circuit

Wait signal

Clear

CLK

To UART0, 1*1
<To 8/10-bit A/D converter>

Internal clock

Output control circuit

Pin

Input control circuit

Clock selector

Output generation circuit

Pin

External clock

Reverse

EN

P26/TOT0*1
<P27/TOT1>

P24/TIN0*1
<P25/TIN1>

3

2

Select signal

Function select

Operation control circuit

| — | — | — | — | CSL1 | CSL0 | MOD2 | MOD1 | MOD0 | OUTE | OUTL | RELD | INTE | UF | CNTE | TRG |

Timer control status register (TMCSR0)*1
<TMCSR1>

Interrupt request signal
#29 (1D$_H$)*2
<#30 (1E$_H$)>

*1 :The timer has ch.0 and ch.1, and listed in the parenthesis <> are for ch.1.

*2 :Interrupt number
φ :Machine clock frequency

6. 24-bit Free run Timer

The 24-bit free-run timer is a 24-bit up counter for counting up in synchronization to divided-by-3 or divided-by-4 of the machine clock, in which an interrupt factor can be selected from the overflow interrupt and four types of timer intermediate bit interrupt to be operated as an interval timer.

The free-run timer can be used to generating reference timing signals for the input capture (ICU) and output compare (OCU).

(1) Register Configuration

- Free-run timer control register upper digits (TCCR : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · · bit 0	Initial value
000051H	—	—	RESV	RESV	RESV	RESV	RESV	PR0	(TCCR : L)	- -111111 B
	—	—	R/W	R/W	R/W	R/W	R/W	R/W		

- Free-run timer control register lower digits (TCCR : L)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000050H	(TCCR : H)	STP	CLR	IVF	IVFE	TIM	TIME	TIS1	TIS0	11000000B
		W	W	R/W	R/W	R/W	R/W	R/W	R/W	

- Free-run timer upper data register (TCRH)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000056H 000057H	—	—	—	—	—	—	—	—	T23	T22	T21	T20	T19	T18	T17	T16	00000000B 00000000B
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

- Free-run timer lower data register (TCRL)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000054H 000055H	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	00000000B 00000000B
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

R/W : Readable and writable
R : Read only
W : Write only
— : Unused

(2) Block Diagram
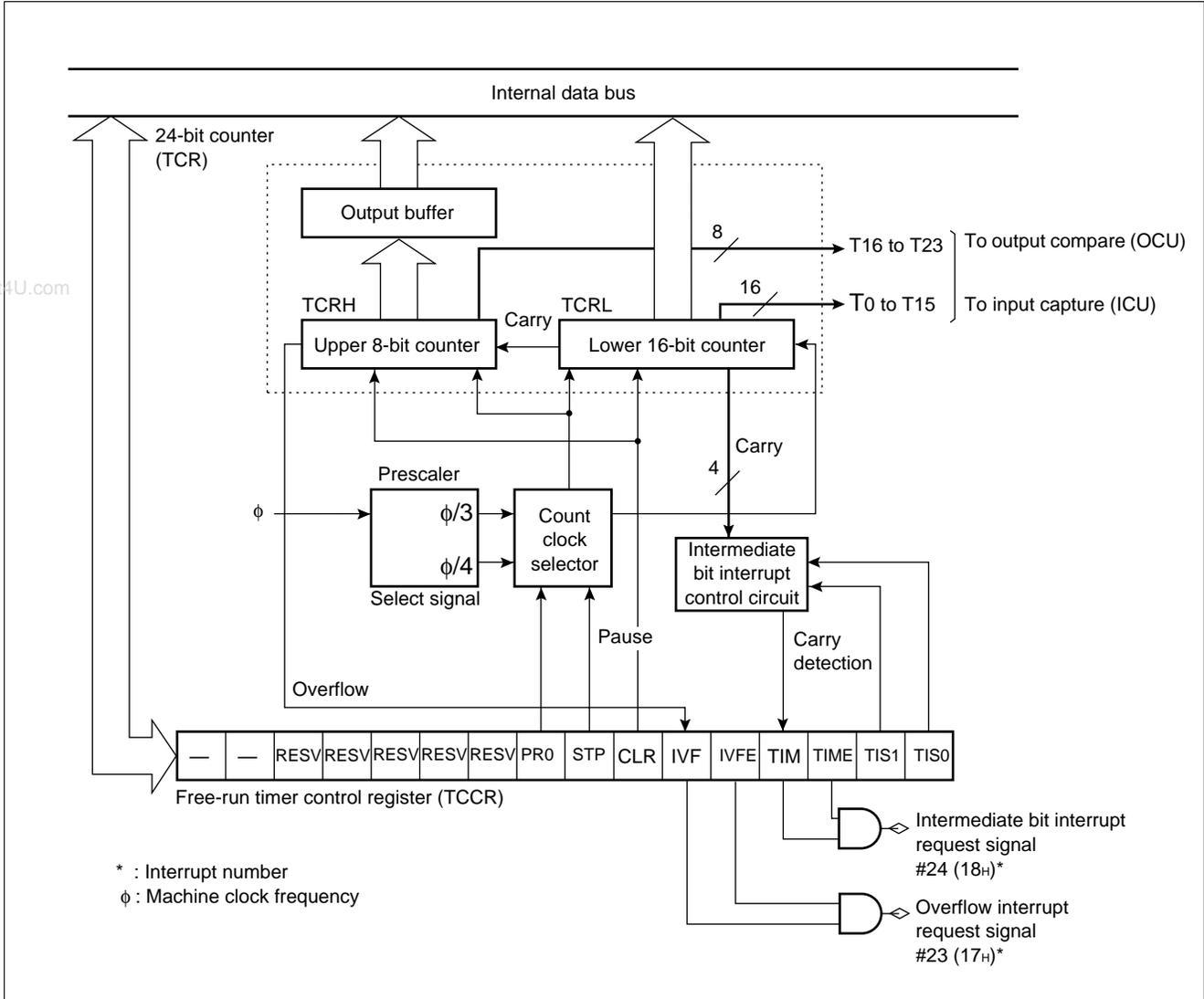
7. Input Capture (ICU)

The input capture (ICU) generates an interrupt request to the CPU simultaneously with a storing operation of current counter value of the 24-bit free run timer to the ICU data register (ICDR) upon an input of a trigger edge to the external pin.

There are four sets (four channels) of the input capture external pins and ICU data registers (ICDR), enabling measurements of maximum of four events.
- The input capture has four sets of external input pins (ASR0 to ASR3) and ICU registers (ICDR), enabling measurements of maximum of four events.
- A trigger edge direction can be selected from rising/falling/both edges.
- The input capture can be set to generate an interrupt request at the storage timing of the counter value of the 24-bit free run timer to the ICU data register (ICDR).
- The input compare conforms to the extended intelligent I/O service (EI^{2}OS).
- The input capture function is suited for measurements of intervals (frequencies) and pulse-widths.

(1) Register Configuration

- ICU control register upper digits (ICC : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · · bit 0	Initial value
000053$_H$	IRE3	IRE2	IRE1	IRE0	IR3	IR2	IR1	IR0	(ICC : L)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- ICU control register lower digits (ICC : L)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000052$_H$	(ICC : H)	EG3B	EG3A	EG2B	EG2A	EG1B	EG1A	EG0B	EG0A	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- ICU upper data register 0 to 3 (ICDR0H to ICDR3H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ICDR0H : 000063$_H$ ICDR1H : 000067$_H$ ICDR2H : 00006B$_H$ ICDR3H : 00006F$_H$	—	—	—	—	—	—	—	—	00000000$_B$
	R	R	R	R	R	R	R	R	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ICDR0H : 000062$_H$ ICDR1H : 000066$_H$ ICDR2H : 00006A$_H$ ICDR3H : 00006E$_H$	D23	D22	D21	D20	D19	D18	D17	D16	XXXXXXXX$_B$
	R	R	R	R	R	R	R	R	

- ICU lower data register 0 to 3 (ICDR0L to ICDR3L)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ICDR0L : 000061$_H$ ICDR1L : 000065$_H$ ICDR2L : 000069$_H$ ICDR3L : 00006D$_H$	D15	D14	D13	D12	D11	D10	D9	D8	XXXXXXXX$_B$
	R	R	R	R	R	R	R	R	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ICDR0L : 000060$_H$ ICDR1L : 000064$_H$ ICDR2L : 000068$_H$ ICDR3L : 00006C$_H$	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
	R	R	R	R	R	R	R	R	

R/W : Readable and writable
R : Read only
— : Unused
X : Indeterminate

(2) Block Diagram
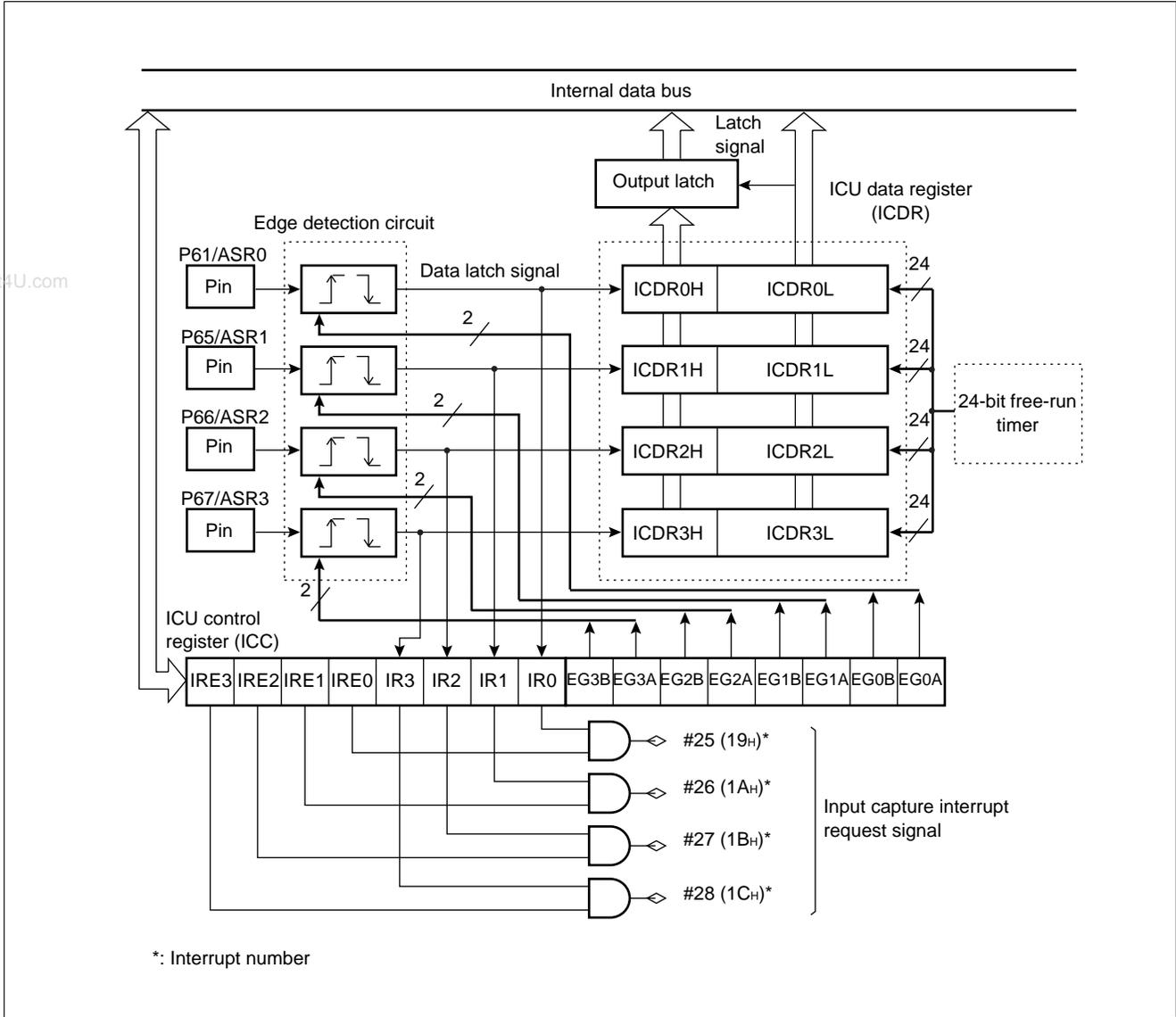
8. Output Compare (OCU)

The output compare (OCU) is two sets of compare units consisting of four-channel OCU compare data registers, a comparator and a control register.

An interrupt request can be generated for each channel upon a match detection by performing time-division comparison between the OCU compare data register setting value and the counter value of the 24-bit free-run timer.

The DOT pin can be used as a waveform output pin for reversing output upon a match detection or a general-purpose output port for directly outputting the setting value of the DOT bit.

(1) Register Configuration

- OCU control register 00 upper digits (CCR00 : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
000059$_H$	—	—	—	—	MD3	MD2	MD1	MD0	(CCR00 : L)	- - - - 0000$_B$
	—	—	—	—	R/W	R/W	R/W	R/W		

- OCU control register 00 lower digits (CCR00 : L)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000058$_H$	(CCR00 : H)	RESV	RESV	RESV	RESV	CPE3	CPE2	CPE1	CPE0	11110000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- OCU control register 01 upper digits (CCR01 : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
00005B$_H$	ICE3	ICE2	ICE1	ICE0	IC3	IC2	IC1	IC0	(CCR01 : L)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- OCU control register 01 lower digits (CCR01 : L)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00005A$_H$	(CCR01 : H)	—	—	—	—	DOT3	DOT2	DOT1	DOT0	- - - - 0000$_B$
		—	—	—	—	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Unused

(Continued)

(Continued)

• OCU compare upper data register 0 to 7 (CPR00H to CPR07H)

Address										
CPR00H : 000073H	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8		Initial value
CPR01H : 000077H	—	—	—	—	—	—	—	—		00000000B
CPR02H : 00007BH	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
CPR03H : 00007FH										
CPR04H : 000083H										
CPR05H : 000087H										
CPR06H : 00008BH										
CPR07H : 00008FH										

Address										
CPR00H : 000072H	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		Initial value
CPR01H : 000076H	D23	D22	D21	D20	D19	D18	D17	D16		00000000B
CPR02H : 00007AH	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
CPR03H : 00007EH										
CPR04H : 000082H										
CPR05H : 000086H										
CPR06H : 00008AH										
CPR07H : 00008EH										

• OCU compare lower data register 0 to 7 (CPR00L to CPR07L)

Address										
CPR00L : 000071H	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8		Initial value
CPR01L : 000075H	D15	D14	D13	D12	D11	D10	D9	D8		00000000B
CPR02L : 000079H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
CPR03L : 00007DH										
CPR04L : 000081H										
CPR05L : 000085H										
CPR06L : 000089H										
CPR07L : 00008DH										

Address										
CPR00L : 000070H	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		Initial value
CPR01L : 000074H	D7	D6	D5	D4	D3	D2	D1	D0		00000000B
CPR02L : 000078H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
CPR03L : 00007CH										
CPR04L : 000080H										
CPR05L : 000084H										
CPR06L : 000088H										
CPR07L : 00008CH										

R/W : Readable and writable
— : Unused

(2) Block Diagram of Output Compare (OCU)
- Overall block diagram
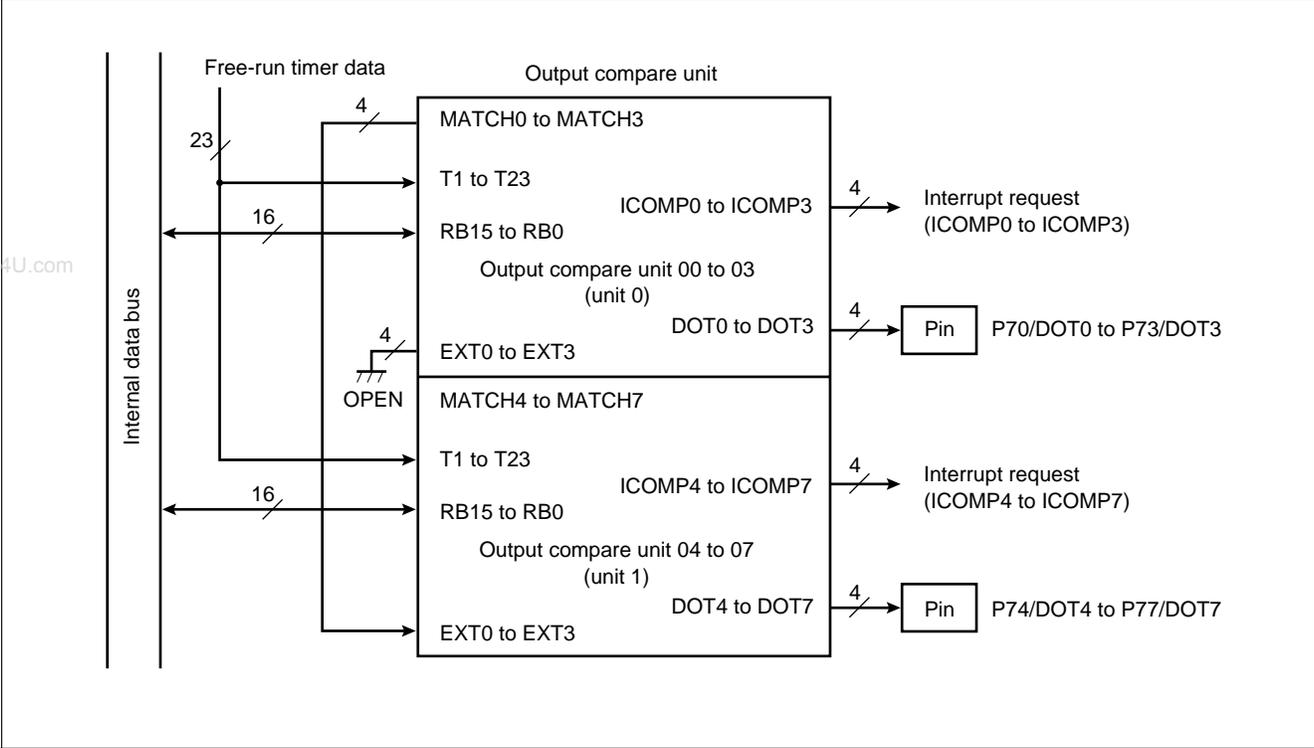
• **Block diagram of unit 0**
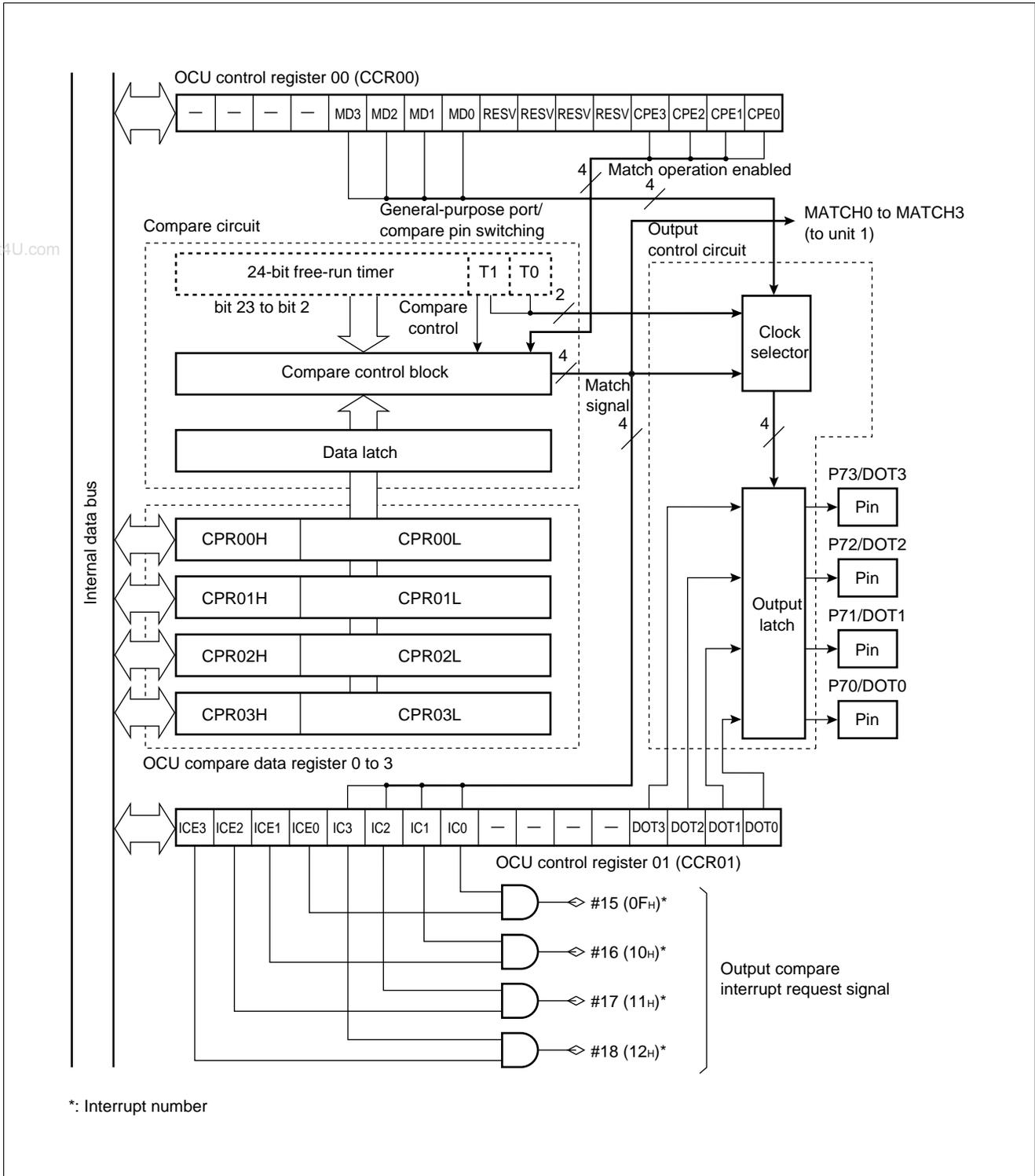
- **Block diagram of unit 1**
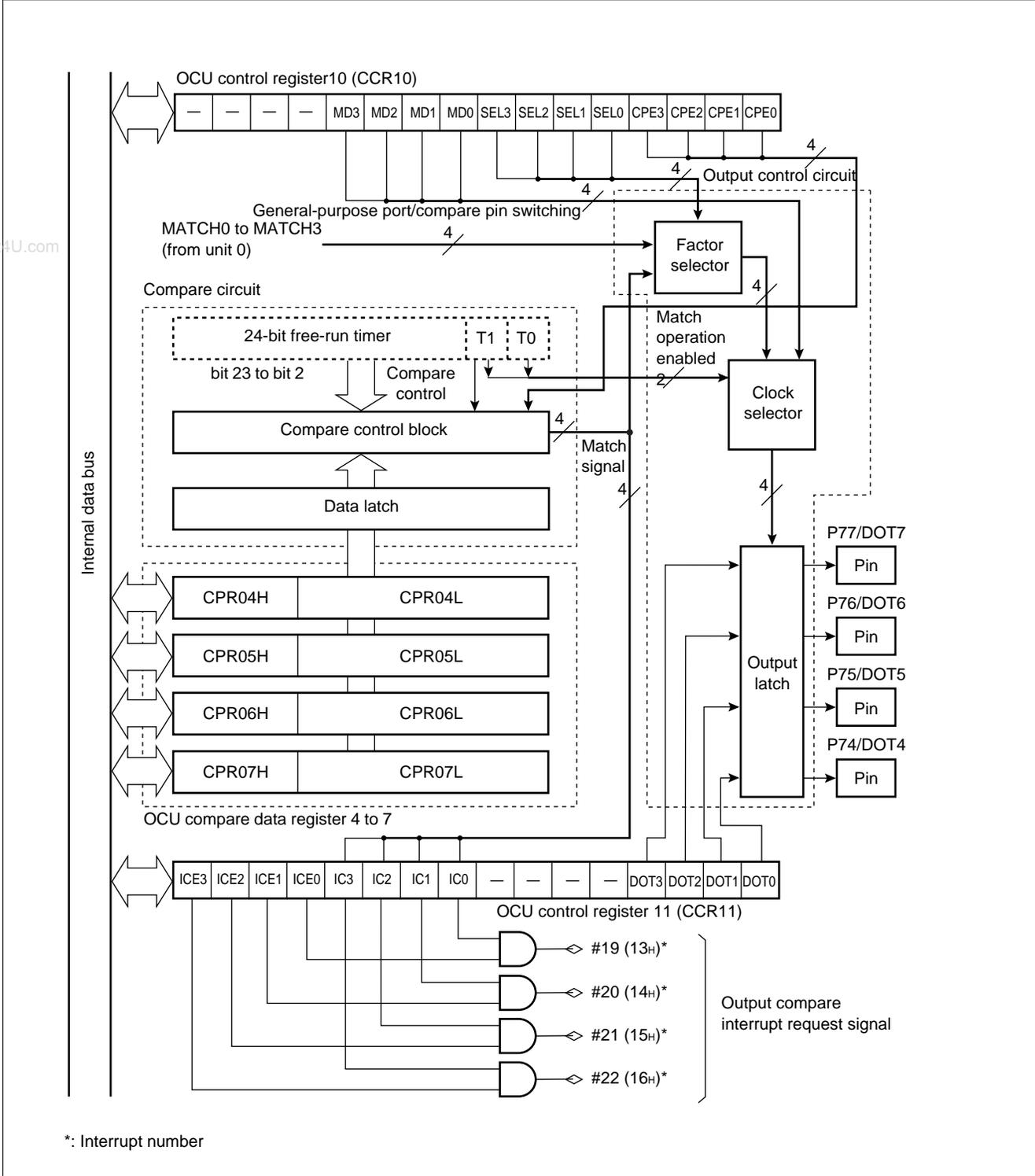
*: Interrupt number

9. I²C Interface (Included Only in MB90675 Series)

The I²C interface is a serial I/O port supporting Inter IC BUS operating as master/slave devices on I²C bus and has the following features.
- Master/slave transmission/reception
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transmission direction detection function
- Repeated generation function start condition and detection function
- Bus error detection function

(1) Register Configuration

- I²C bus status register (IBSR)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000040H	(IBCR)	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	00000000B
		R	R	R	R	R	R	R	R	

- I²C bus control register (IBCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
000041H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	(IBSR)	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- I²C bus clock control register (ICCR)

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000042H	(IADR)	—	—	EN	CS4	CS3	CS2	CS1	CS0	--0XXXXXB
		—	—	R/W	R/W	R/W	R/W	R/W	R/W	

- I²C address register (IADR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
000043H (IADR)	—	A6	A5	A4	A3	A2	A1	A0	(ICCR)	-XXXXXXXB
	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000044H (IDAR)	(Reserved area)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
R : Read only
— : Unused
X : Indeterminate

(2) Block Diagram
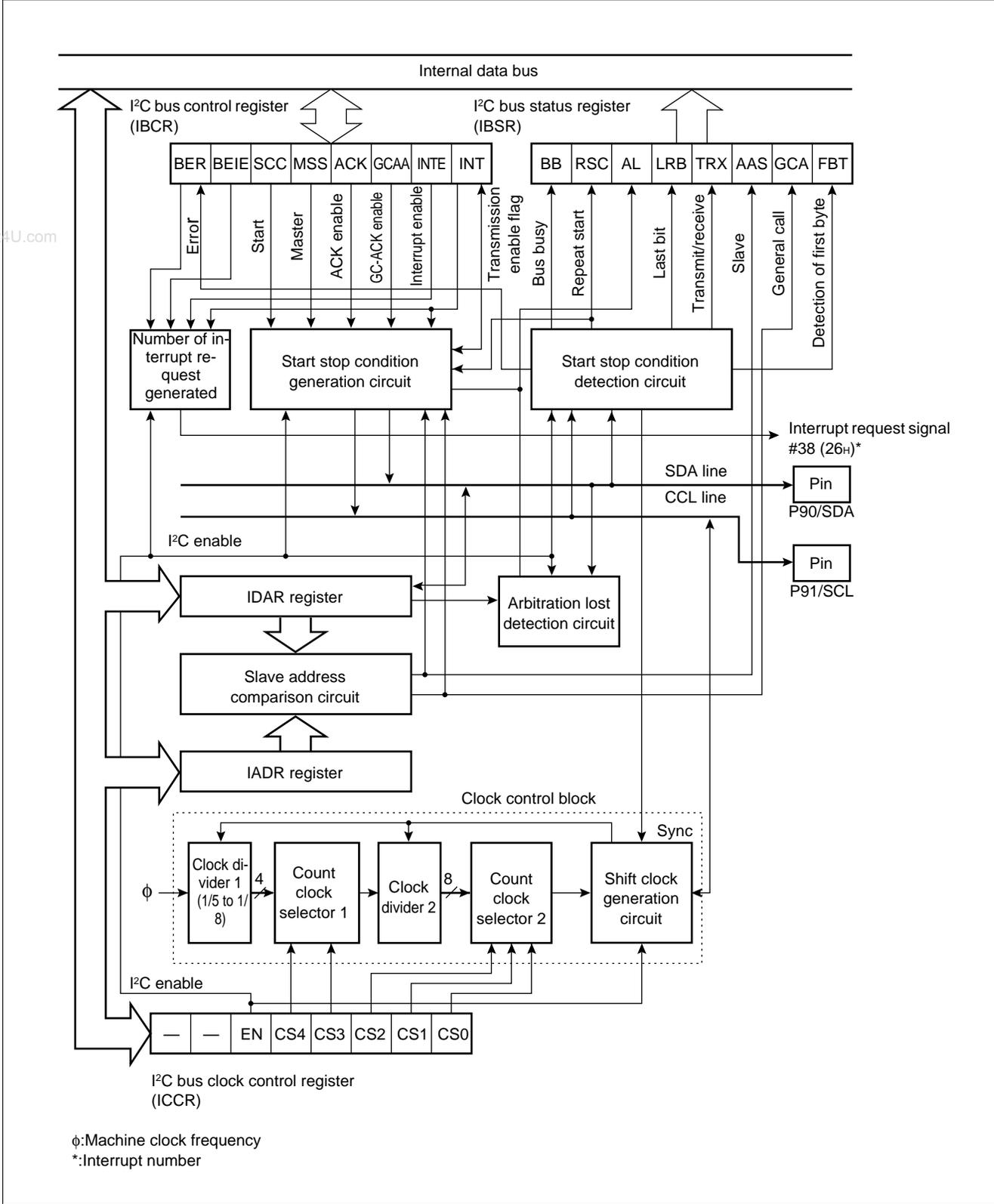
10. UART0

UART0 is a general-purpose serial data communication interface for performing synchronous or asynchronous communication (start-stop synchronization system). In addition to the normal duplex communication function (normal mode), UART0 has a master/slave type communication function (multi-processor mode).
- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (with start and stop bit)
  Clock asynchronized (start-stop synchronization system)
- Baud rate: With dedicated baud rate generator, selectable from 12 types
  External clock input possible
  Internal clock (a clock supplied from 16-bit reload timer can be used.)
- Data length: 7 bits to 9 bits selective (with a parity bit)
  6 bits to 8 bits selective (without a parity bit)
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
  Overrun error
  Parity error (not available in multi-processor mode)
- Interrupt request: Receive interrupt (reception complete, receive error detection)
  Receive interrupt (transmission complete)
  Transmit/receive conforms to extended intelligent I/O service (EI^{2}OS)
- Master/slave type communication function (multi-processor mode): 1 (master) to n (slave) communication possible

(1) Register Configuration

- Status register 0 (USR0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7·············bit 0	Initial value
000021$_H$	RDRF	ORFE	PE	TDRE	RIE	TIE	RBF	TBF	(UMC0)	00100000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Mode control register 0 (UMC0)

Address	bit 15···········bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000020$_H$	(USR0)	PEN	SBL	MC1	MC0	SMDE	RFC	SCKE	SOE	00000100$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Rate and data register 0 (URD0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7·············bit 0	Initial value
000023$_H$	BCH	RC3	RC2	RC1	RC0	BCH0	P	D8	(UIDR0/UODR0)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Input data register 0 (UIDR0)

Address	bit 15···· bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022$_H$	(URD0)	D8	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
		R	R	R	R	R	R	R	R	R	

- Output data register 0 (UODR)

Address	bit 15···· bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022$_H$	(URD0)	D8	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
		W	W	W	W	W	W	W	W	W	

R/W : Readable and writable
R : Read only
W: Write only
X : Indeterminate

(2) Block Diagram

*: Interrupt number
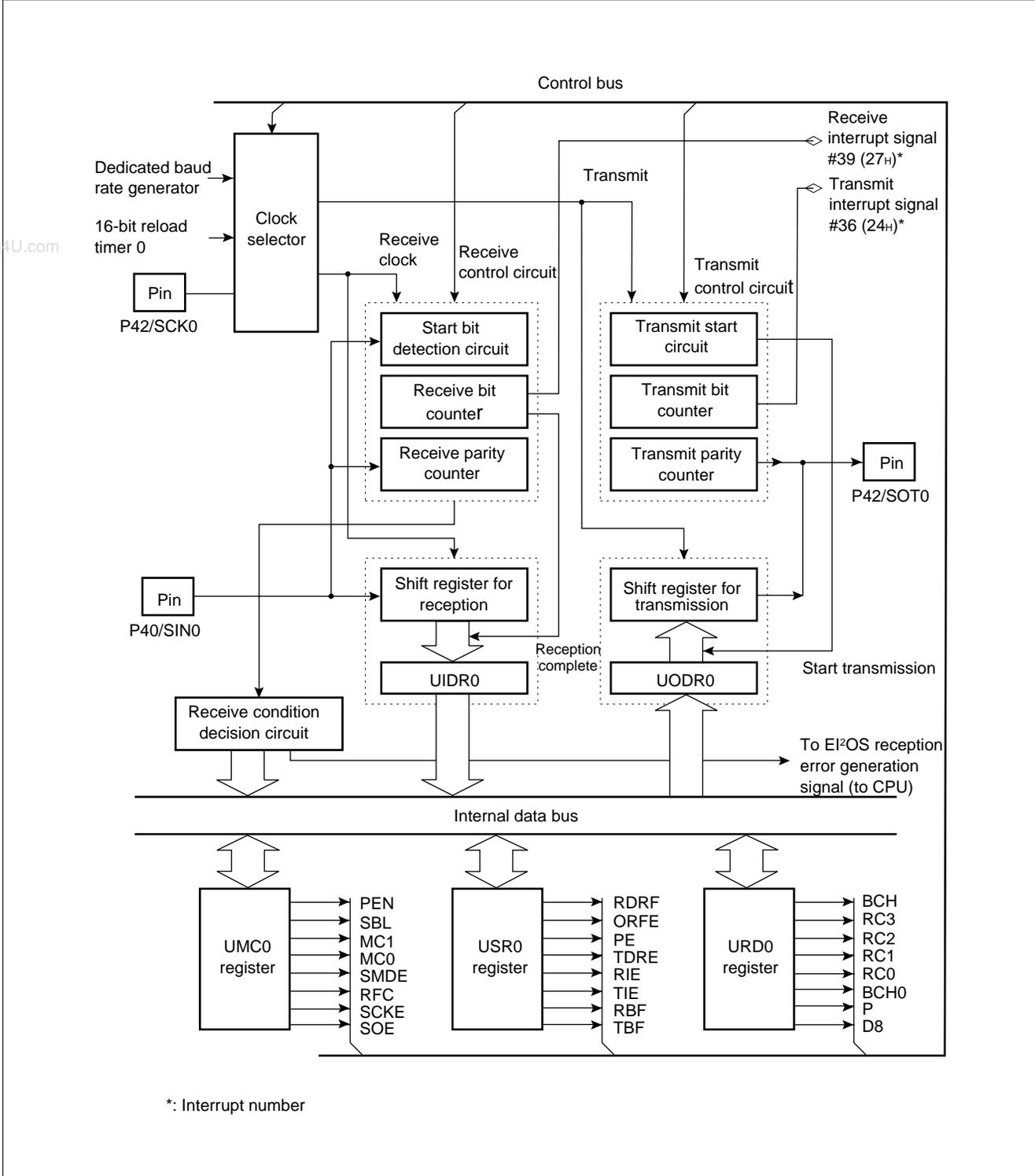
11. UART1 (SCI)

UART1 (SCI) is a general-purpose serial data communication interface for performing synchronous or asynchronous communication (start-stop synchronization system). In addition to the normal duplex communication function (normal mode), UART1 has a master-slave type communication function (multi-processor mode).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (no start or stop bit)
  - Clock asynchronized (start-stop synchronization system)
- Baud rate: With dedicated baud rate generator, selectable from 8 types
  - External clock input possible
  - Internal clock (a internal clock supplied from 16-bit reload timer can be used.)
- Data length: 7 bits (for asynchronous normal mode only)
  - 8 bits
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection:Framing error
  - Overrun error
  - Parity error (not available in multi-processor mode)
- Interrupt request: Receive interrupt (reception complete, receive error detection)
  - Receive interrupt (transmission complete)
  - Transmit/receive conforms to extended intelligent I/O service (EI^{2}OS)
- Master/slave type communication function (multi-processor mode):1 (master) to n (slave) communication possible (supported only for master station)

(1) Register Configuration

- **Control register 1 (SCR1)**

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	Initial value
000025H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	(SMR1)	00000100B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- **Mode register 1 (SMR1)**

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000024H	(SCR1)	MD1	MD0	CS2	CS1	CS0	BCH	SCKE	SOE	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Status register 1 (SSR1)**

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	Initial value
000027H	PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	(SIDR1/SODR1)	00001-00B
	R	R	R	R	R	—	R/W	R/W		

- **Input data register 1 (SIDR1)**

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000026H	(SSR1)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		R	R	R	R	R	R	R	R	

- **Output data register 1 (SODR1)**

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000026H	(SSR1)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		W	W	W	W	W	W	W	W	

R/W : Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

(2) Block Diagram
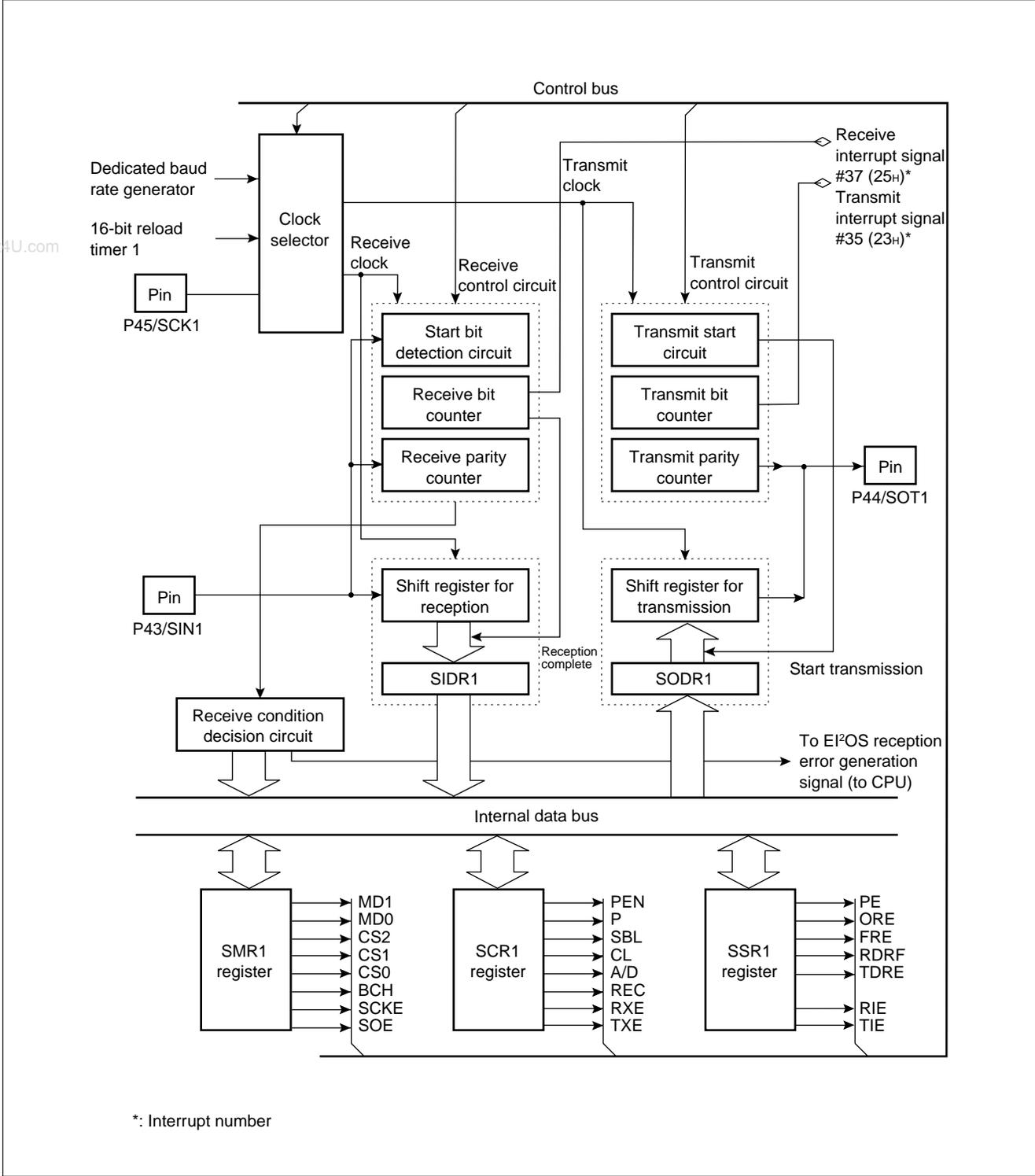
12. DTP/External Interrupt Circuit

The DTP (Data Transfer Peripheral)/external interrupt circuit is located between peripheral equipment connected externally and the F^{2}MC-16L CPU and transmits interrupt requests or data transfer requests generated by peripheral equipment to the CPU, generates external interrupt request and starts the extended intelligent I/O service (EI^{2}OS).

(1) Register Configuration

- DTP/interrupt factor register (EIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ············ bit 0	Initial value
000029H	—	—	—	—	ER3	ER2	ER1	ER0	(ENIR)	- - - - 0000 B
	—	—	—	—	R/W	R/W	R/W	R/W		

- DTP/interrupt enable register (ENIR)

Address	bit 15 ············ bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000028H	(EIRR)	—	—	—	—	EN3	EN2	EN1	EN0	- - - - 0000 B
		—	—	—	—	R/W	R/W	R/W	R/W	

- Request level setting register (ELVR)

Address	bit 15 ············ bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00002AH	(Vacancy)	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Unused

(2) Block Diagram

Request level setting register (ELVR)

| LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LA0 |

2   2   2

Internal data bus

Pin
P60/INT0

Level edge
selector 3

Level edge
selector 1

2

Pin
P61/INT1

Level edge
selector 2

Level edge
selector 0

DTP/external interrupt input
detection circuit

Pin
P62/INT2

Pin
P63/INT3

DTP/interrupt factor register
(EIRR)

| — | — | — | — | ER3 | ER2 | ER1 | ER0 |

Interrupt request signal

#14 (0E$_H$)*

#13 (0D$_H$)*

#14 (0C$_H$)*

#11 (0B$_H$)*

DTP/interrupt enable register
(ENIR)

| — | — | — | — | EN3 | EN2 | EN1 | EN0 |

*: Interrupt signal
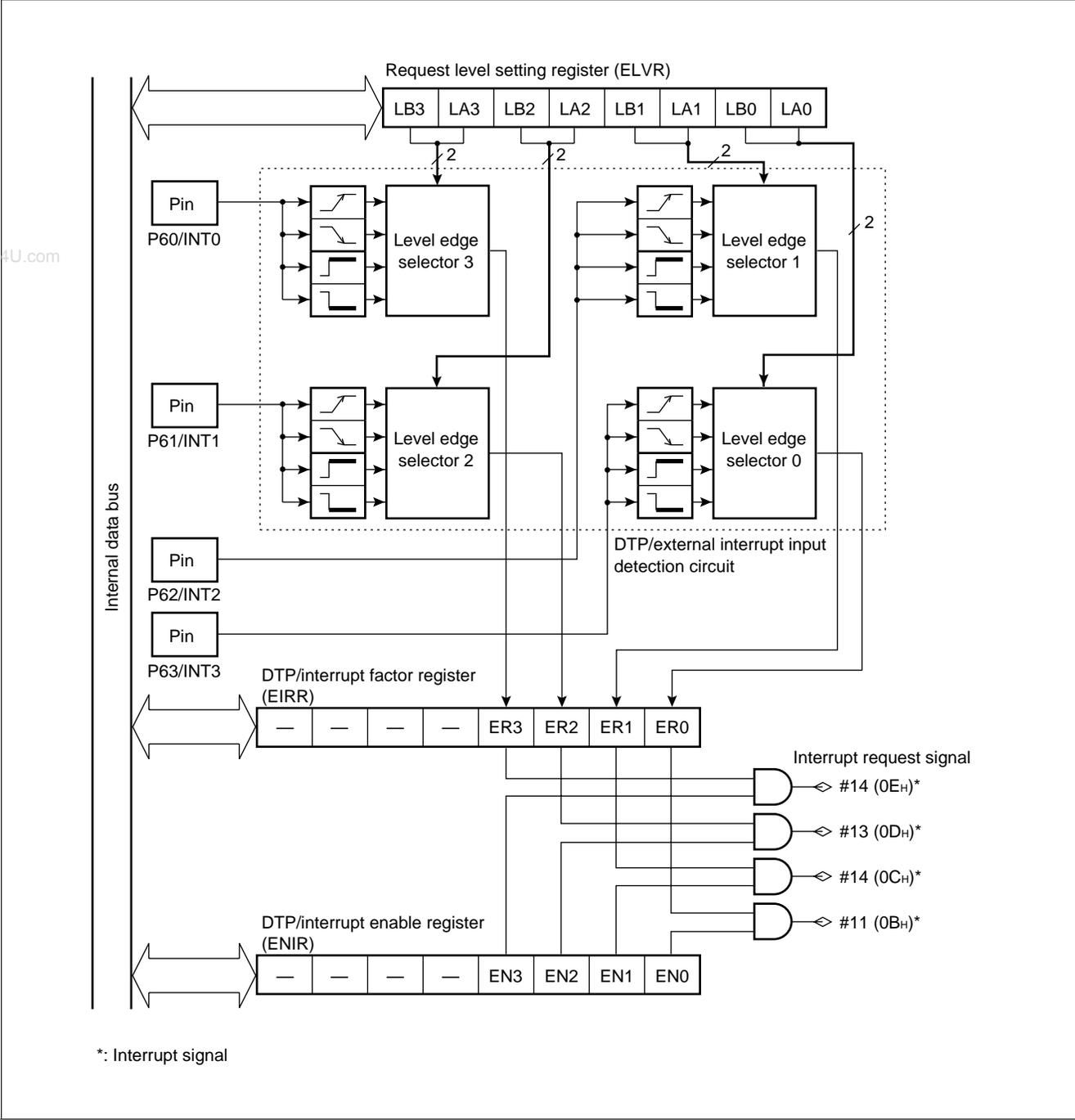
13. Wake-up Interrupt

Wake-up interrupts transmits interrupt request ("L" level) generated by peripheral device located between exter-nal peripheral devices and the F^{2}MC-16L CPU to the CPU and invokes interrupt processing.

The interrupt does not conform to the extended intelligent I/O service (EI^{2}OS).

(1) Register Configuration

- Wake-up interrupt flag register (EIFR)
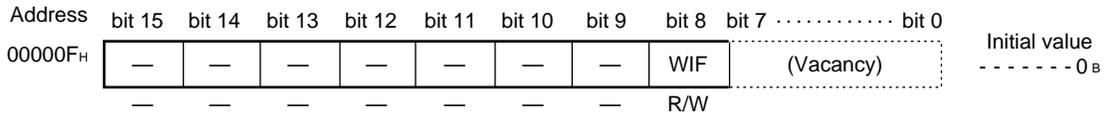
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
00000F$_H$	—	—	—	—	—	—	—	WIF	(Vacancy)	- - - - - - - 0 $_B$
	—	—	—	—	—	—	—	R/W		

- Wake-up interrupt enable register (EICR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
00001F$_H$	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	(Vacancy)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
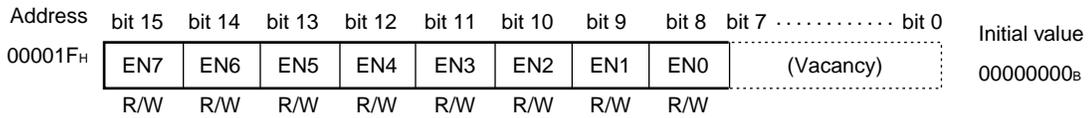
R/W : Readable and writable
— : Unused

(2) Block Diagram
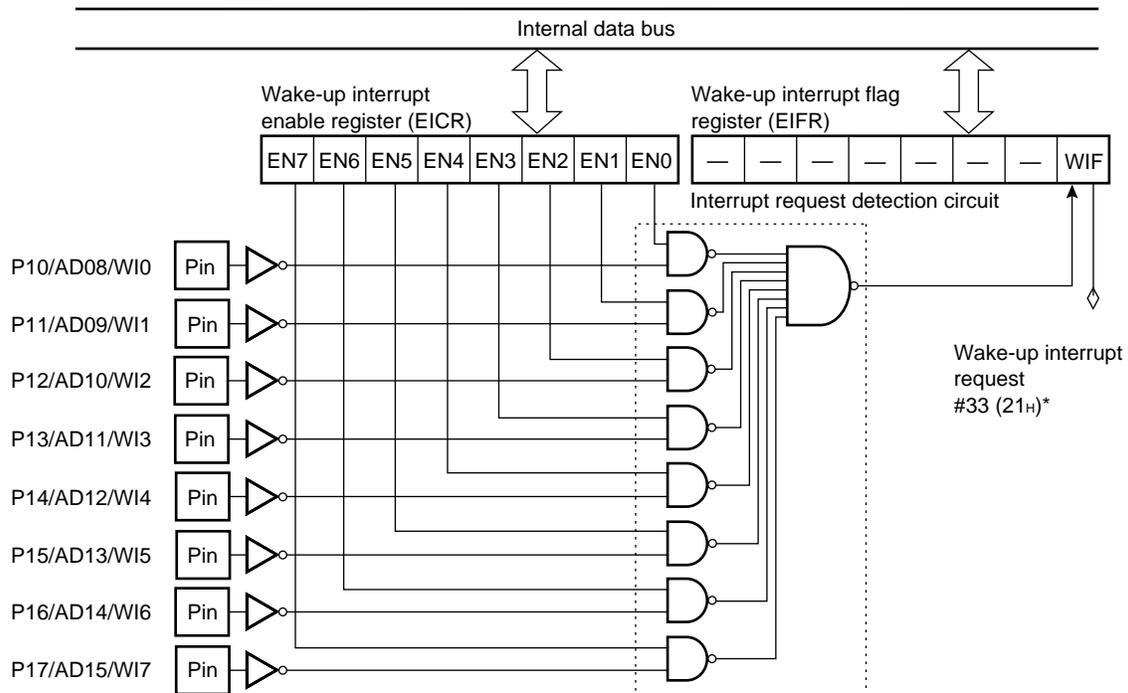
14. Delayed Interrupt Generation Module

The delayed interrupt generation module generates interrupts for switching tasks for development on a realtime operating system (REALOS software). The module can be used to generate hardware interrupt requests to the CPU with software and cancel the interrupt requests.

This module does not conform to the extended intelligent I/O service (EI^{2}OS).

(1) Register Configuration

- Delayed interrupt factor generation/cancellation register (DIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · bit 0	Initial value
00009F$_H$	—	—	—	—	—	—	—	R0	(Reserved area)	- - - - - - - 0 $_B$
	—	—	—	—	—	—	—	R/W		

R/W : Readable and writable
— : Unused

(2) Block Diagram

Internal data bus

| — | — | — | — | — | — | — | R0 |

Delayed interrupt factor generation/
cancellation register (DIRR)

S factor
R latch

Interrupt request signal
#42 (2A$_H$)*

*: Interrupt signal
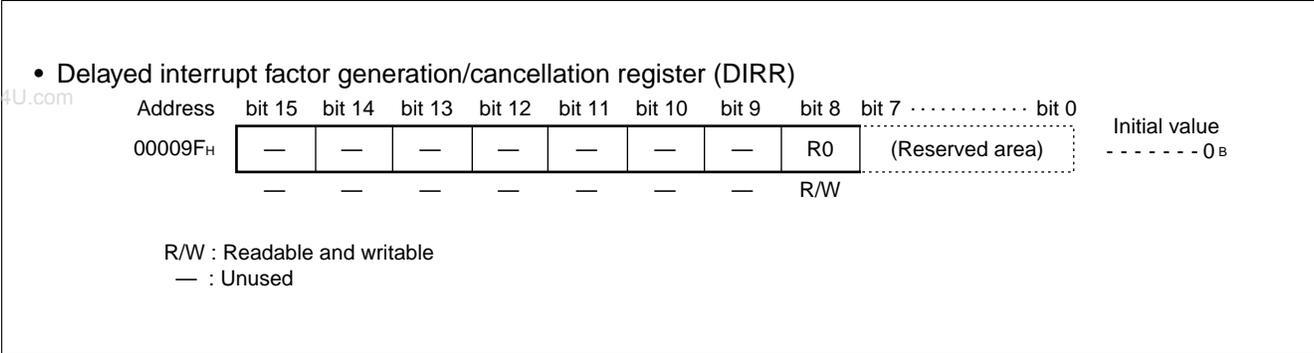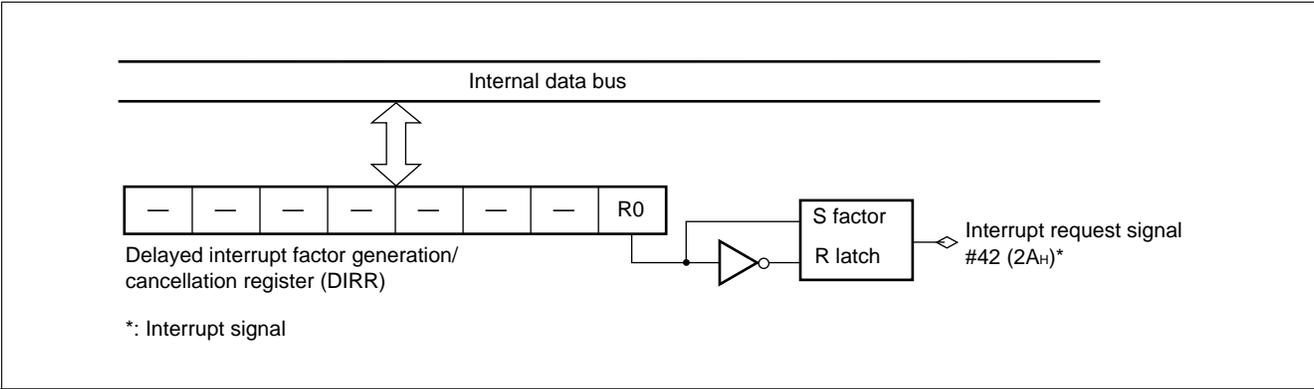
15. 8/10-bit A/D Converter

The 8/10-bit A/D converter has a function of converting analog voltage input to the analog input pins (input voltage) to digital values (A/D conversion) and has the following features.

• Minimum conversion time: 6.13 μs (at machine clock of 16 MHz, including sampling time)
• Minimum sampling time: 3.75 μs (at machine clock of 16 MHz)
• Conversion method: RC successive approximation method with a sample and hold circuit.
• Resolution: 10-bit or 8-bit selective
• Analog input pins: Selectable from eight channels by software
    One-shot conversion mode: Stops conversion after completing a conversion for a stopped channel (one channel only) or for successive channels (maximum of eight channels can be specified)
    Continuous conversion mode: Continues conversions for a specified channel (one channel only) or for successive channels (maximum of eight channels can be specified)
    Stop conversion mode: Stops conversion after completing a conversion for one channel and wait for the next activation.
• Interrupt requests can be generated and the extended intelligent I/O service (EI^{2}OS) can be started after the end of A/D conversion.
• When interrupts are enabled, there is no loss of data even in continuous operations because the conversion data protection function is in effect.
• Starting factors for conversion: Selected from software activation, 16-bit reload timer 1 output (rising edge), and external trigger (falling edge).

(1) Register Configuration

• A/D control status register upper digits (ADCS: H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··········· bit 0	Initial value
00002D$_H$	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	RESV	(ADCS: L)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	W	R/W		

• A/D control status register lower digits (ADCS: L)

Address	bit 15 ··········· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00002C$_H$	(ADCS: H)	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

• A/D data register (ADCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00002E$_H$	S10	—	—	—	—	—	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$ 0000000X$_B$
	R/W	—	—	—	—	—	R	R	R	R	R	R	R	R	R	R	

R/W : Readable and writable
R : Read only
W: Write only
—: Unused
X : Indeterminate

(2) Block Diagram

A/D control status register (ADCS)

Interrupt request signal #31 (1F$_H$)*

| BUSY | INT | INTE | PAUS | STS1 | STS0 | STRT | RESV | MD1 | MD0 | ANS2 | ANS1 | ANS0 | ANE2 | ANE1 | ANE0 |

6

P47/ATG TO

Clock selector

2

Decoder

Internal data bus

φ

Comparator

P57/AN7
P56/AN6
P55/AN5
P54/AN4
P53/AN3
P52/AN2
P51/AN1
P50/AN0

Analog channel selector

Sample hold circuit

Control circuit

AVR
AV$_{CC}$
AV$_{SS}$

D/A converter

A/D data register (ADCR)

| S10 | — | — | — | — | — | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

φ : Machine clock frequency
TO : 16-bit reload timer channel 1 output
  * : Interrupt number

16. Low-power Consumption (Standby) Mode

The F^{2}MC-16L has the following CPU operating mode configured by selection of an operating clock and clock operation control.

* **Clock mode**
  PLL clock mode: A mode in which the CPU and peripheral equipment are driven by PLL-multiplied oscillation clock (HCLK).
  Main clock mode: A mode in which the CPU and peripheral equipment are driven by divided-by-2 of the oscillation clock (HCLK).
  The PLL multiplication circuits stops in the main clock mode.
* **CPU intermittent operation mode**
  The CPU intermittent operation mode is a mode for reducing power consumption by operating the CPU intermittently while external bus and peripheral functions are operated at a high-speed.
* **Hardware stand-by mode**
  The hardware standby mode is a mode for reducing power consumption by stopping clock supply (sleep mode) to the CPU by the low-power consumption control circuit, stopping clock supplies to the CPU and peripheral functions (timebase timer mode), and stopping oscillation clock (stop mode, hardware standby mode).
  Of these modes, modes other than the PLL clock mode are power consumption modes.

(1) Register Configuration

* Clock select register (CKSCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 · · · · · · · · · · · · bit 0	Initial value
0000A1$_H$	RESV	MCM	WS1	WS0	RESV	MCS	CS1	CS0	(LPMCR)	1 1 1 1 1 1 0 0 $_B$
	R/W	R	R/W	R/W	R/W	R/W	W	R/W		

* Low-power consumption mode control register (LPMCR)

Address	bit 15 · · · · · · · · · · · · bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A0$_H$	(CKSCR)	STP	SLP	SPL	RST	RESV	CG1	CG0	RESV	0 0 0 1 1 0 0 0 $_B$
		W	W	R/W	W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
R : Read only
W : Write only

(2) Block Diagram

Low-power consumption mode control register (LPMCR)

| STP | SLP | SPL | RST | RESV | CG1 | CG0 | RESV |

Pin high-impedance control circuit → Pin Hi-z control

Internal reset generation circuit → Internal reset

CPU intermittent operation selector

RST Pin

Select intermittent cycle

CPU clock control circuit → CPU clock

Cancellation of reset

Stop and sleep signal

RST Standby control circuit

Cancellation of interrupt

HST Pin

Stop signal

Machine clock
Cancellation of oscillation stabilization time

Peripheral clock control circuit → Peripheral clock

Clock generation block

Clock selector

Oscillation stabilization time selector

PLL multiplication circuit

| RESV | MCM | WS1 | WS0 | RESV | MCS | CS1 | CS0 |

System clock generation circuit

Clock selection register (CKSCR)

X0 Pin

| Divided -by-2 | Divided -by-2048 | Divided -by-4 | Divided -by-4 | Divided -by-8 |

Main clock

X1 Pin

Timebase timer

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

$(AV_{SS} = V_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	*2
"L" level maximum output current	I_{OL}	—	15	mA	*3
"L" level average output current	I_{OLAV}	—	4	mA	*4
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	*5
"H" level maximum output current	I_{OH}	—	−15	mA	*3
"H" level average output current	I_{OHAV}	—	−4	mA	*4
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	*5
Power consumption	P_D	—	400	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

*1:AV_{CC} shall never exceed V_{CC}. AVRH shall never exceed V_{CC} and AV_{CC}. Also, AVRL shall never exceed V_{CC}, AV_{CC} and AVRH.

*2:V_I and V_O shall never exceed $V_{CC} + 0.3$ V.

*3:The maximum output current is a peak value for a corresponding pin.

*4:Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5:Total average current is an average current value observed for a 100 ms period for all corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV$_{SS}$ = V$_{SS}$ = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V$_{CC}$	2.7	5.5	V	Normal operation
	V$_{CC}$	2.0	5.5	V	Retains status at the time of operation stop
Operating temperature	T$_A$	–40	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value Min.	Value Typ.	Value Max.	Unit	Remarks
"H" level input voltage	V_{IH}	Pins other than V_{IHS} and V_{IHM}	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80, $\overline{HST}$, $\overline{RST}$		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	MB90670 series
	V_{IHS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80 to P86, $\overline{HST}$, $\overline{RST}$, P90, P91, PA0 to PA7, PB0 to PB2		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	MB90675 series
	V_{IHM}	MD pin input		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
"L" level input voltage	V_{IL}	Pins other than V_{ILS} and V_{ILM}		$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	V_{ILS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80, $\overline{HST}$, $\overline{RST}$		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	MB90670 series
	V_{ILS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80 to P86, $\overline{HST}$, $\overline{RST}$, P90, P91, PA0 to PA7, PB0 to PB2		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	MB90675 series
	V_{ILM}	MD pin input		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
"H" level output voltage	V_{OH}	Other than P50 to P57	$V_{CC} = 4.5$ V $I_{OH} = -4.0$ mA	$V_{CC} - 0.5$	—	—	V	
	V_{OH}	Other than P50 to P57	$V_{CC} = 2.7$ V $I_{OH} = -1.6$ mA	$V_{CC} - 0.3$	—	—	V	
"L" level output voltage	V_{OL}	All output pins	$V_{CC} = 4.5$ V $I_{OL} = 4.0$ mA	—	—	0.4	V	
	V_{OL}	All output pins	$V_{CC} = 2.7$ V $I_{OL} = 2.0$ mA	—	—	0.4	V	
Open-drain output leakage current	I_{leak}	P50 to P57, P90, P91[*1]	—	—	0.1	10	μA	

(Continued)

(Continued)

(AV$_{CC}$ = V$_{CC}$ = 2.7 V to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input leakage current	I$_{IL}$	Other than P50 to P57, P90 and P91	V$_{CC}$ = 5.5 V V$_{SS}$ < V$_I$ < V$_{CC}$	–10	—	10	μA	
Pull-up resistance	R	—	V$_{CC}$ = 5.0 V	25	45	100	kΩ	
	R	—	V$_{CC}$ = 3.0 V	40	95	200	kΩ	
Pull-down resistance	R	—	V$_{CC}$ = 5.0 V	25	50	200	kΩ	
	R	—	V$_{CC}$ = 3.0 V	40	100	400	kΩ	
Power supply current	I$_{CC}$	—	Internal operation at 16 MHz V$_{CC}$ at 5.0 V	—	50	70	mA	Normal operation*2
	I$_{CCS}$	—	Internal operation at 16 MHz V$_{CC}$ at 5.0 V	—	10	30	mA	In sleep mode*2
	I$_{CC}$	—	Internal operation at 8 MHz V$_{CC}$ at 3.0 V	—	12	20	mA	Normal operation*2
	I$_{CCS}$	—	Internal operation at 8 MHz V$_{CC}$ at 3.0 V	—	2.5	10	mA	In sleep mode*2
	I$_{CCH}$	—	T$_A$ = +25°C	—	0.1	10	μA	In stop mode and hardware standby mode*2
Input capacitance	C$_{IN}$	Other than AV$_{CC}$, AV$_{SS}$, V$_{CC}$, V$_{SS}$	—	—	10	—	pF	

*1: Only MB90675 series has P90 and P91 pins.

*2: The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice.

4. AC Characteristics

(1) Reset Input Timing, Hardware Standby Input Timing

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value Min.	Value Max.	Unit	Remarks
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}*	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$	—	16 t_{CP}*	—	ns	

*: For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timings."
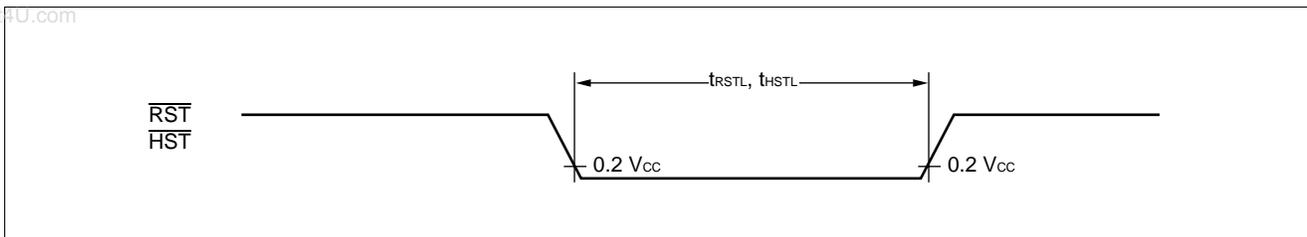
• Measurement conditions for AC ratings
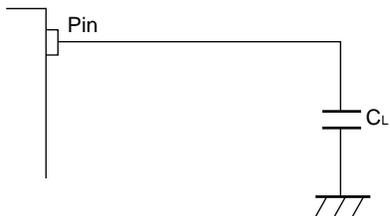
C_L is a load capacitance connected to a pin under test.

CLK, ALE: $C_L = 30$ pF
Address data bus (AD15 to AD00), $\overline{RD}$, $\overline{WR}$: $C_L = 80$ pF

(2)Specification for Power-on Reset

$(AV_{SS} = V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin name	Condi-tion	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	—	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}		1	—	ms	Due to repeated operations

*: V_{CC} must be kept lower than 0.2 V before power-on.

Notes : • The above ratings are values for causing a power-on reset.

• When $\overline{HST}$ is set to "L" level, apply power according to this table to cause a power-on reset irrespective of whether or not a power-on reset is required.

• For built-in resources in the device, re-apply power to the resources to cause a power-on reset.

• There are internal registers which can be initialized only by a power-on reset. Apply power according to this rating to ensure initialization of the registers.

t_R

V_{CC} 2.7 V   0.2 V   0.2 V   0.2 V

t_{OFF}
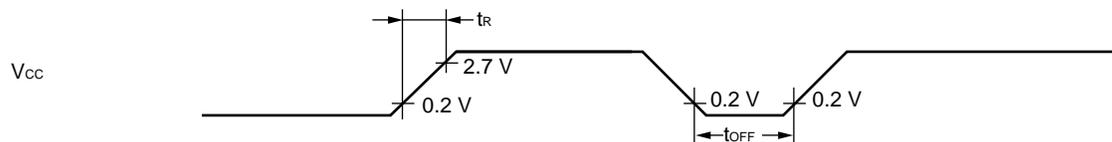
Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.

Main power supply voltage V_{CC}

Sub power supply voltage V_{SS}

RAM data retained

It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.
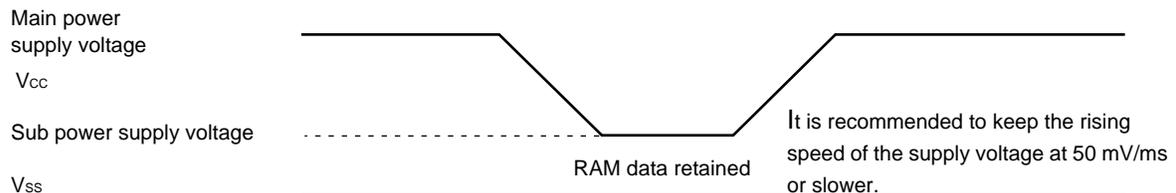
(3) Clock Timing
- **Operation at 5.0 V ± 10%**

(AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F$_C$	X0, X1		3	—	32	MHz	
Clock cycle time	t$_C$	X0, X1		31.25	—	333	ns	
Input clock pulse width	P$_{WH}$, P$_{WL}$	X0		10	—	—	ns	Recommended duty ratio of 30% to 70%
Input clock rising/falling time	t$_{CR}$, t$_{CF}$	X0	—	—	—	5	ns	
Internal operating clock frequency	f$_{CP}$	—		1.5	—	16	MHz	
Internal operating clock cycle time	t$_{CP}$	—		62.5	—	666	ns	
Frequency fluctuation rate locked	Δf	P37/CLK		—	—	3	%	*

*: The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{f_O} \times 100 \, (\%)$$
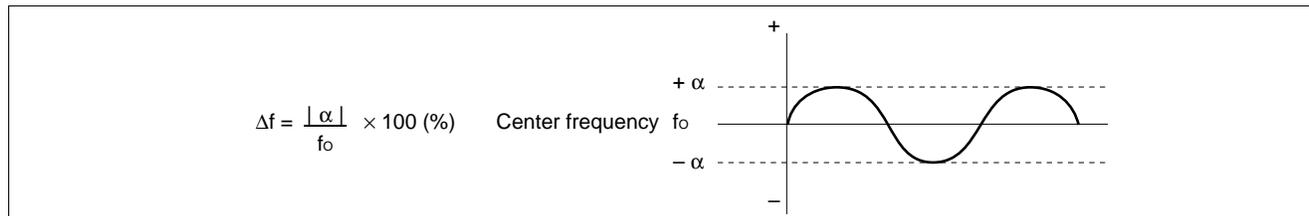
The PLL frequency deviation changes periodically from the preset frequency "(about CLK × (1CYC to 50 CYC)）", thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

- **Operation at V$_{CC}$ = 2.7 V (minimum value)**

(AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40°C to +85°C)

Parameter	Symbol	Pin name	Condi-tion	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F$_C$	X0, X1	—	3	—	16	MHz	
Clock cycle time	t$_C$	X0, X1		62.5	—	333	ns	
Input clock pulse width	P$_{WH}$, P$_{WL}$	X0		20	—	—	ns	Recommended duty ratio of 30% to 70%
Input clock rising/falling time	t$_{CR}$, t$_{CF}$	X0		—	—	5	ns	
Internal operating clock fre-quency	f$_{CP}$	—		1.5	—	8	MHz	
Internal operating clock cycle time	t$_{CP}$	—		125	—	666	ns	
Frequency fluctuation rate locked	Δf	P37/CLK		—	—	3	%	*

*: The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{f_O} \times 100\ (\%) \qquad \text{Center frequency}\ \ f_O$$
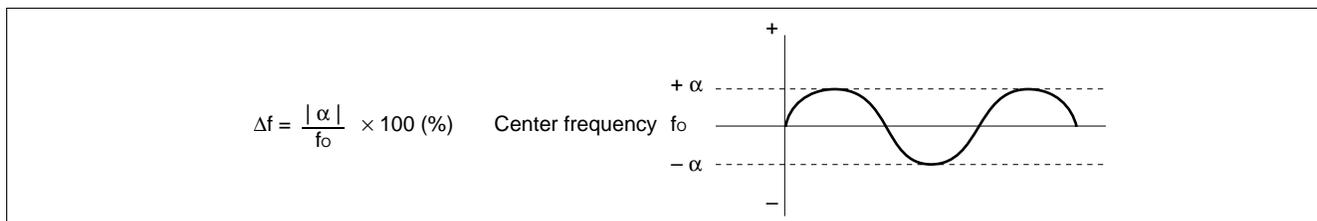
The PLL frequency deviation changes periodically from the preset frequency "(about CLK × (1CYC to 50 CYC)", thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

• **Clock timing**

• **PLL operation guarantee range**

Relationship between internal operating clock frequency and power supply voltage

Relationship between clock frequency and internal operating clock frequency
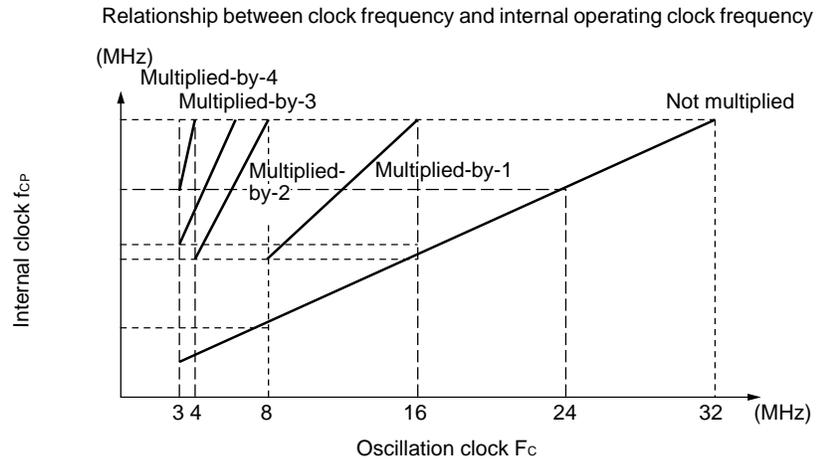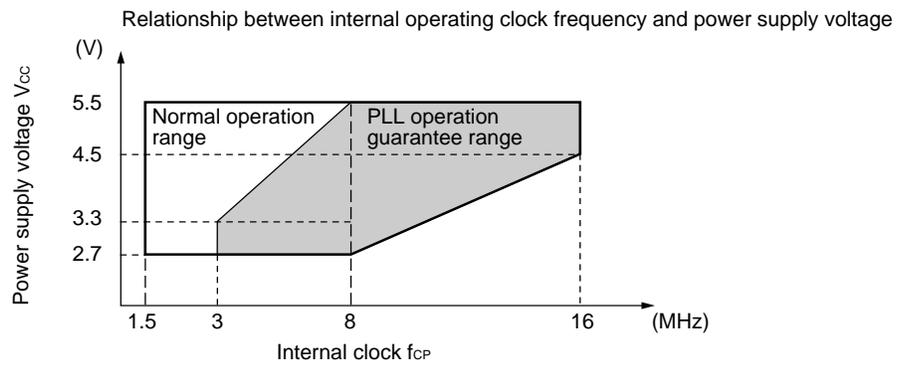
Note : The operation guarantee range on the lower voltage is 2.7 V for the evaluation chips.

The AC ratings are measured for the following measurement reference voltages.

• **Input signal waveform**

Hystheresis input pin
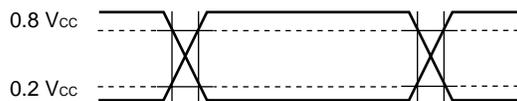
Pins other than hystheresis input/MD input
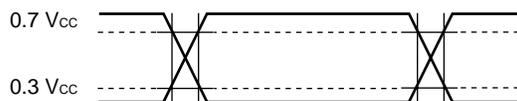
• **Output signal waveform**

Output pin
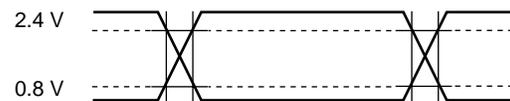
(4) Recommended Resonator Manufacturers

• **Sample application of piezoelectric resonator (FAR family)**
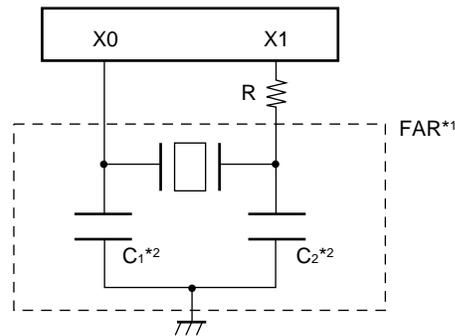
*1: FUJITSU MEDIA DEVICES Acoustic Resonator

FAR part number (built-in capacitor type)	Frequency (MHz)	Dumping resistor	Initial deviation of FAR frequen-cy ($T_A = +25°C$)	Temperature characteristics of FAR frequency ($T_A = −20°C$ to $+60°C$)	Loading capacitors[2]
FAR-C4☐C-2000-☐20	2.00	510 Ω	±0.5%	±0.5%	Built-in
FAR-C4☐A-4000-☐01	4.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-4000-☐02	4.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-4000-☐00	4.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-8000-☐02	8.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-12000-☐02	12.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-16000-☐02	16.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-20000-L14B	20.00	—	±0.5%	±0.5%	Built-in
FAR-C4☐B-24000-L14A	24.00	—	±0.5%	±0.5%	Built-in

Inquiry: FUJITSU MEDIA DEVICES LIMITED

- **Sample application of ceramic resonator**
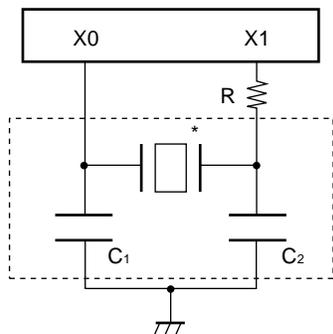
- **Mask ROM product**

Resonator manufacturer	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Kyocera Corporation	KBR-2.0MS	2.00	150	150	Not required
	PBRC-2.00A	2.00	150	150	Not required
	KBR-4.0MSA	4.00	33	33	680 Ω
	KBR-4.0MKS	4.00	Built-in	Built-in	680 Ω
	PBRC4.00A	4.00	33	33	680 Ω
	PBRC4.00B	4.00	Built-in	Built-in	680 Ω
	KBR-6.0MSA	6.00	33	33	Not required
	KBR-6.0MKS	6.00	Built-in	Built-in	Not required
	PBRC6.00A	6.00	33	33	Not required
	PBRC6.00B	6.00	Built-in	Built-in	Not required
	KBR-8.0M	8.00	33	33	560 Ω
	PBRC8.00A	8.00	33	33	Not required
	PBRC8.00B	8.00	Built-in	Built-in	Not required
	KBR-10.0M	10.00	33	33	330 Ω
	PBRC10.00B	10.00	Built-in	Built-in	680 Ω
	KBR-12.0M	12.00	33	33	330 Ω
	PBRC-12.00B	12.00	Built-in	Built-in	680 Ω
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CST2.00MG040	2.00	Built-in	Built-in	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CST4.00MGW040	4.00	Built-in	Built-in	Not required
	CSA6.00MG	6.00	30	30	Not required
	CST6.00MGW	6.00	Built-in	Built-in	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CST8.00MTW	8.00	Built-in	Built-in	Not required

(Continued)

(Continued)

Resonator manufacturer	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Murata Mfg. Co., Ltd.	CSA10.0MTZ	10.00	30	30	Not required
	CST10.0MTW	10.00	Built-in	Built-in	Not required
	CSA12.0MTZ	12.00	30	30	Not required
	CST12.0MTW	12.00	Built-in	Built-in	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CST16.00MXW0C3	16.00	Built-in	Built-in	Not required
	CSA20.00MXZ040	20.00	10	10	Not required
	CSA24.00MXZ040	24.00	5	5	Not required
	CST24.00MXW0H1	24.00	Built-in	Built-in	Not required
	CSA32.00MXZ040	32.00	5	5	Not required
	CST32.00MXW040	32.00	Built-in	Built-in	Not required
TDK Corporation	FCR4.0MC5	4.00	Built-in	Built-in	Not required

• **One-time product**

Resonator manufacturer	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Murata Mfg. Co., Ltd.	CSTCS4.00MG0C5	4.0	Built-in	Built-in	Not required
	CST8.00MTW	8.00	Built-in	Built-in	Not required
	CSACS8.00MT	8.00	30	30	Not required
	CSA10.0MTZ	10.00	30	30	Not required
	CST10.0MTW	10.00	Built-in	Built-in	Not required
TDK Corporation	FCR4.0MC5	4.00	Built-in	Built-in	Not required

Inquiry:Kyocera Corporation
 •AVX Corporation
  North American Sales Headquarters: TEL 1-803-448-9411
 •AVX Limited
  European Sales Headquarters: TEL 44-1252-770000
 •AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters: TEL 852-363-3303
 Murata Mfg. Co., Ltd.
 •Murata Electronics North America, Inc.: TEL 1-404-436-1300
 •Murata Europe Management GmbH: TEL 49-911-66870
 •Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233
 TDK Corporation
 •TDK Corporation of America
  Chicago Regional Office: TEL 1-708-803-6100
 •TDK Electronics Europe GmbH
  Components Division: TEL 49-2102-9450
 •TDK Singapore (PTE) Ltd.: TEL 65-273-5022
 •TDK Hongkong Co., Ltd.: TEL 852-736-2238
 •Korea Branch, TDK Corporation: TEL 82-2-554-6633

(5) Clock Output Timing

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5\text{V}, \ AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	$1 \ t_{CP}$*	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}	CLK	$V_{CC} = 5.0 \text{ V} \pm 10\%$	$1 \ t_{CP}$*$/2 - 20$	$1 \ t_{CP}$*$/2 + 20$	ns	5.0 V ± 10 % is ± 20
	t_{CHCL}	CLK	$V_{CC} = 3.0 \text{ V} \pm 10\%$	$1 \ t_{CP}$*$/2 - 35$	$1 \ t_{CP}$*$/2 + 35$	ns	3.0 V ± 10 % is ± 35

*: For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timing".

(6) Bus Read Timing

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value Min.	Value Max.	Unit	Remarks
ALE pulse width	t_{LHLL}	ALE	$V_{CC} = 5.0 \text{ V} \pm10\%$	1 t_{CP}*/2 – 20	—	ns	
	t_{LHLL}	ALE	$V_{CC} = 3.0 \text{ V} \pm10\%$	1 t_{CP}*/2 – 35	—	ns	
Effective address → ALE ↓ time	t_{AVLL}	AD15 to AD00	$V_{CC} = 5.0 \text{ V} \pm10\%$	1 t_{CP}*/2 – 25	—	ns	
	t_{AVLL}	AD15 to AD00	$V_{CC} = 3.0 \text{ V} \pm10\%$	1 t_{CP}*/2 – 40	—	ns	
ALE ↓ → address effective time	t_{LLAX}	AD15 to AD00	—	1 t_{CP}*/2 – 15	—	ns	
Effective address → $\overline{RD}$ ↓ time	t_{AVRL}	AD15 to AD00		1 t_{CP}* – 15	—	ns	
Effective address → read data time	t_{AVDV}	AD15 to AD00	$V_{CC} = 5.0 \text{ V} \pm10\%$	—	5 t_{CP}*/2 – 60	ns	
	t_{AVDV}	AD15 to AD00	$V_{CC} = 3.0 \text{ V} \pm10\%$	—	5 t_{CP}*/2 – 80	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 t_{CP}*/2 – 20	—	ns	
$\overline{RD}$ ↓ → read data time	t_{RLDV}	AD15 to AD00	$V_{CC} = 5.0 \text{ V} \pm10\%$	—	3 t_{CP}*/2 – 60	ns	
	t_{RLDV}	AD15 to AD00	$V_{CC} = 3.0 \text{ V} \pm10\%$	—	3 t_{CP}*/2 – 80	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD15 to AD00		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1 t_{CP}*/2 – 15	—	ns	
$\overline{RD}$ ↑ → address disappear time	t_{RHAX}	$\overline{RD}$, A19 to A16	—	1 t_{CP}*/2 – 10	—	ns	
Effective address → CLK ↑ time	t_{AVCH}	CLK, A19 to A16		1 t_{CP}*/2 – 20	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1 t_{CP}*/2 – 20	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timing".

(7) Bus Write Timing

(AV$_{CC}$ = V$_{CC}$ = 2.7 V to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value Min.	Value Max.	Unit	Remarks
Effective address → $\overline{WR}$ ↓ time	t$_{AVWL}$	A19 to A00	—	1 t$_{CP}$ – 15	—	ns	
$\overline{WR}$ pulse width	t$_{WLWH}$	$\overline{WR}$		3 t$_{CP}$*/2 – 20	—	ns	
Write data → $\overline{WR}$ ↑ time	t$_{DVWH}$	AD15 to AD00		3 t$_{CP}$*/2 – 20	—	ns	
$\overline{WR}$ ↑ → data hold time	t$_{WHDX}$	AD15 to AD00	V$_{CC}$ = 5.0 V ±10%	20	—	ns	
	t$_{WHDX}$	AD15 to AD00	V$_{CC}$ = 3.0 V ±10%	30	—	ns	
$\overline{WR}$ ↑ → address disappear time	t$_{WHAX}$	A19 to A00	—	1 t$_{CP}$*/2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t$_{WHLH}$	$\overline{WRL}$, ALE		1 t$_{CP}$*/2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t$_{WLCH}$	$\overline{WRH}$, CLK		1 t$_{CP}$*/2 – 20	—	ns	

*: For t$_{CP}$ (internal operating clock cycle time), refer to "(3) Clock Timing".
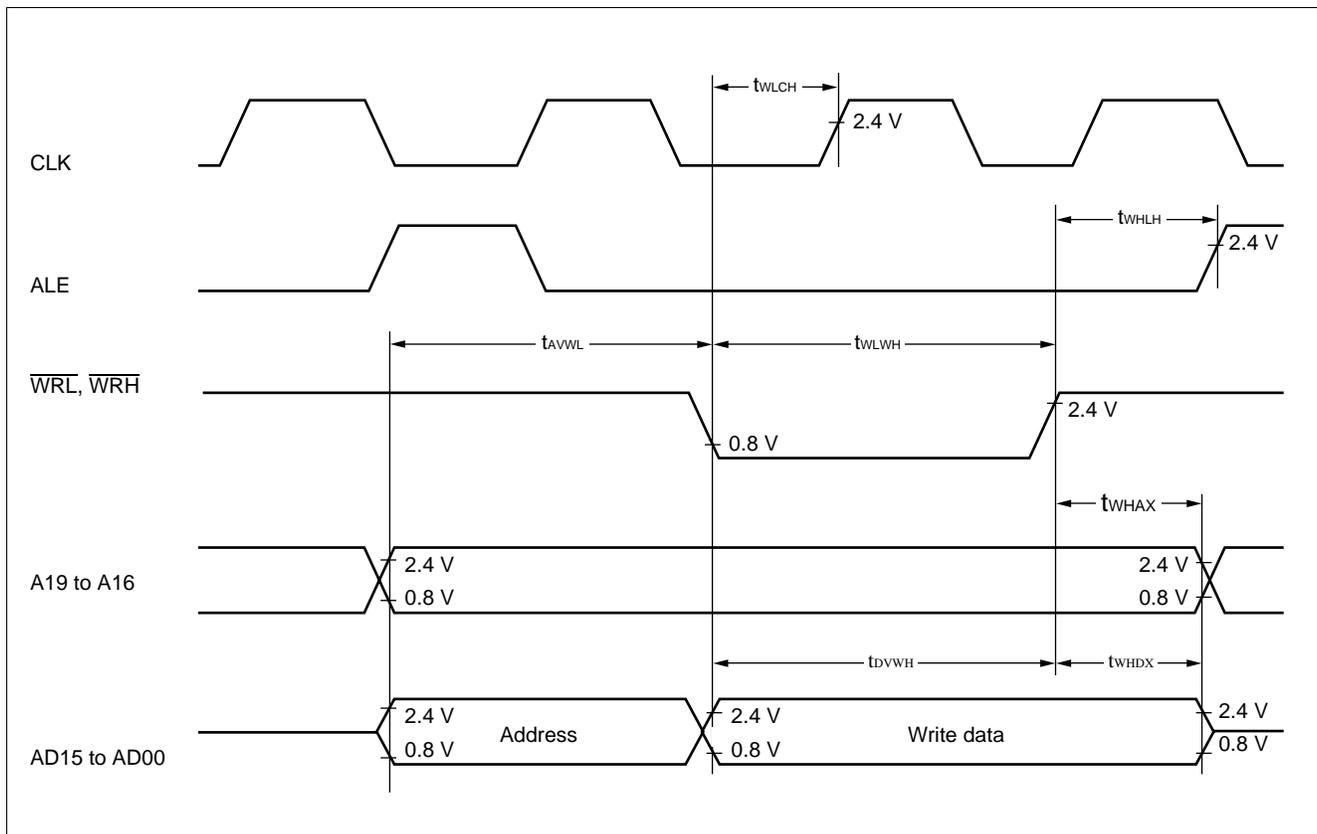
(8) Ready Input Timing

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	$V_{CC} = 5.0 \text{ V} \pm 10\%$	45	—	ns	
	t_{RYHS}	RDY	$V_{CC} = 3.0 \text{ V} \pm 10\%$	70	—	ns	
RDY hold time	t_{RYHH}	RDY	—	0	—	ns	

Note : Use the auto-ready function when the setup time for the rising of the RDY signal is not sufficient.
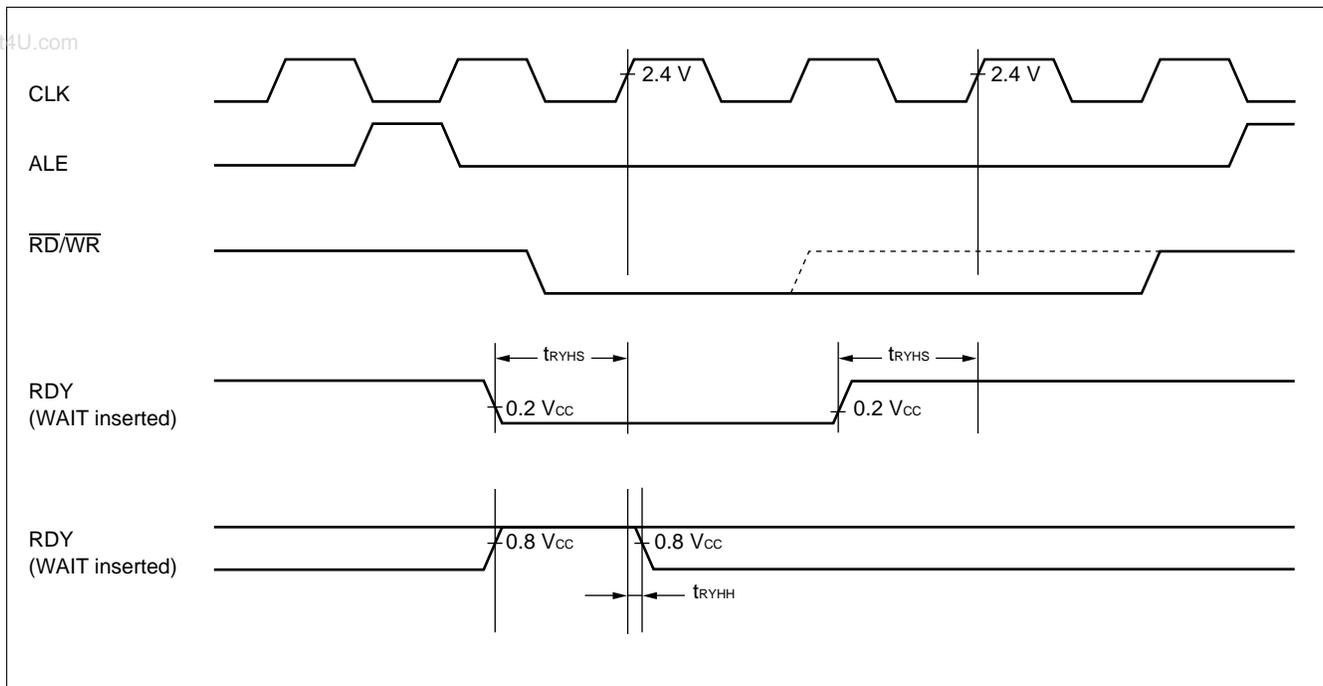
(9) Hold Timing

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pins in floating status → $\overline{HAK} \downarrow$ time	t_{XHAL}	$\overline{HAK}$	—	30	1 t_{CP}*	ns	
$\overline{HAK} \uparrow$ → pin valid time	t_{HAHV}	$\overline{HAK}$		1 t_{CP}*	2 t_{CP}*	ns	

* : For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timing".

Note : More than 1 machine cycle is needed before $\overline{HAK}$ changes after HRQ pin is fetched.

(10) UART0 Timing

$(AV_{CC} = V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin name	Condition	Value Min.	Value Max.	Unit	Remarks
Serial clock cycle time	t_{SCYC}	—	—	8 t_{CP}*	—	ns	Internal shift clock mode C_L = 80 pF + 1 TTL for an output pin
SCK ↓ → SOT delay time	t_{SLOV}	—	V_{CC} = 5.0 V ±10%	– 80	80	ns	
	t_{SLOV}	—	V_{CC} = 3.0 V ±10%	– 120	120	ns	
Valid SIN → SCK ↑	t_{IVSH}	—	V_{CC} = 5.0 V ±10%	100	—	ns	
	t_{IVSH}	—	V_{CC} = 3.0 V ±10%	200	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	—		1 t_{CP}*	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	—	4 t_{CP}*	—	ns	External shift clock mode C_L = 80 pF + 1 TTL for an output pin
Serial clock "L" pulse width	t_{SLSH}	—		4 t_{CP}*	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—	V_{CC} = 5.0 V ±10%	—	150	ns	
	t_{SLOV}	—	V_{CC} = 3.0 V ±10%	—	200	ns	
Valid SIN → SCK ↑	t_{IVSH}	—	V_{CC} = 5.0 V ±10%	60	—	ns	
	t_{IVSH}	—	V_{CC} = 3.0 V ±10%	120	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	—	V_{CC} = 5.0 V ±10%	60	—	ns	
	t_{SHIX}	—	V_{CC} = 3.0 V ±10%	120	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timing".

Notes : • These are AC ratings in the CLK synchronous mode.

  • C_L is the load capacitor connected to pins while testing.

• **Internal shift clock mode**

SCK

t_{SCYC}

0.8 V   2.4 V   0.8 V

t_{SLOV}

SOT

2.4 V
0.8 V

t_{IVSH} t_{SHIX}

SIN

2.4 V_{CC} 2.4 V_{CC}
0.8 V_{CC} 0.8 V_{CC}

• **External shift clock mode**

SCK

t_{SLSH} t_{SHSL}

0.2 V_{CC} 0.2 V_{CC} 0.8 V_{CC} 0.8 V_{CC}

t_{IVSH}

SOT

2.4 V
0.2 V

t_{IVSH} t_{SHIX}

SIN

0.8 V_{CC} 0.8 V_{CC}
0.2 V_{CC} 0.2 V_{CC}

(11) UART1 Timing

(AV$_{CC}$ = V$_{CC}$ = 2.7 V to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t$_{SCYC}$	—	—	8 t$_{CP}$*	—	ns	Internal shift clock mode C$_L$ = 80 pF + 1 TTL for an output pin
SCK ↓ → SOT delay time	t$_{SLOV}$	—	V$_{CC}$ = 5.0 V ±10%	– 80	80	ns	
	t$_{SLOV}$	—	V$_{CC}$ = 3.0 V ±10%	– 120	120	ns	
Valid SIN → SCK ↑	t$_{IVSH}$	—	V$_{CC}$ = 5.0 V ±10%	100	—	ns	
	t$_{IVSH}$	—	V$_{CC}$ = 3.0 V ±10%	200	—	ns	
SCK ↑ → valid SIN hold time	t$_{SHIX}$	—		1 t$_{CP}$*	—	ns	
Serial clock "H" pulse width	t$_{SHSL}$	—	—	4 t$_{CP}$*	—	ns	External shift clock mode C$_L$ = 80 pF + 1 TTL for an output pin
Serial clock "L" pulse width	t$_{SLSH}$	—		4 t$_{CP}$*	—	ns	
SCK ↓ → SOT delay time	t$_{SLOV}$	—	V$_{CC}$ = 5.0 V ±10%	—	150	ns	
	t$_{SLOV}$	—	V$_{CC}$ = 3.0 V ±10%	—	200	ns	
Valid SIN → SCK ↑	t$_{IVSH}$	—	V$_{CC}$ = 5.0 V ±10%	60	—	ns	
	t$_{IVSH}$	—	V$_{CC}$ = 3.0 V ±10%	120	—	ns	
SCK ↑ → valid SIN hold time	t$_{SHIX}$	—	V$_{CC}$ = 5.0 V ±10%	60	—	ns	
	t$_{SHIX}$	—	V$_{CC}$ = 3.0 V ±10%	120	—	ns	

* : For t$_{CP}$ (internal operating clock cycle time), refer to "(3) Clock Timing".

Notes : • These are AC ratings in the CLK synchronous mode.

• C$_L$ is the load capacitor connected to pins while testing.

• **Internal shift clock mode**

• **External shift clock mode**
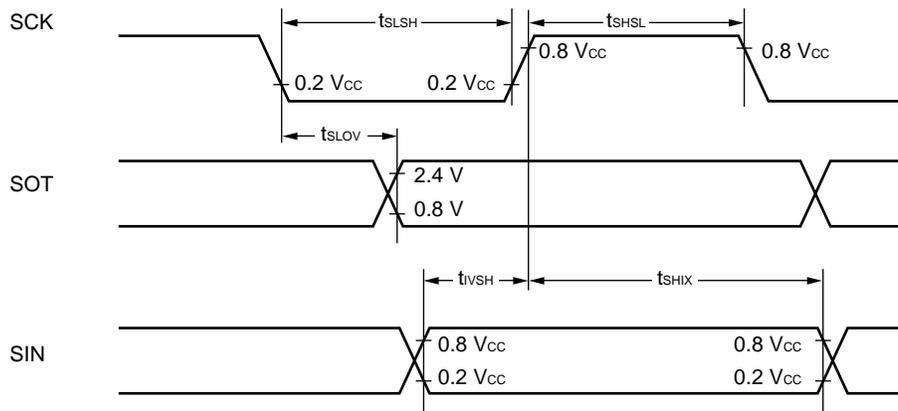
(12) Timer Input Timing

(AV$_{CC}$ = V$_{CC}$ = 2.7 V to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t$_{TIWH}$, t$_{TIWL}$	TIN0, TON1	—	4 t$_{CP}$*	—	ns	

* : For t$_{CP}$ (internal operating clock cycle time), refer to "(3) Clock Timing".
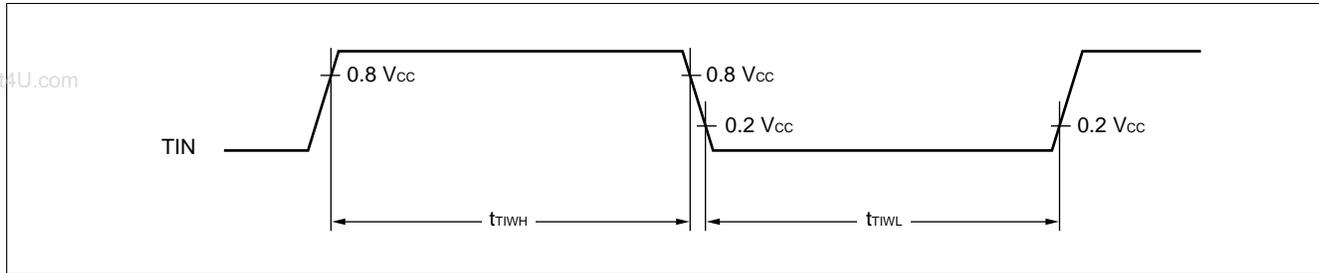
(13) Timer Output Timing

(AV$_{CC}$ = V$_{CC}$ = 2.7 V to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T$_{OUT}$ transition time	t$_{TO}$	TOT0, TOT1	V$_{CC}$ = 5.0 V ±10%	30	—	ns	
	t$_{TO}$	TOT0, TOT1	V$_{CC}$ = 3.0 V ±10%	80	—	ns	

(14) I²C Timing

(AV$_{CC}$ = V$_{CC}$ = 5.0 V ±10%, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value Min.	Value Max.	Unit	Remarks
SCL clock frequency	f$_{SCL}$	—		0	100	kHz	
Bus free time between stop and start conditions	t$_{BUS}$	—		4.7	—	µs	
Hold time (re-transmission) start	t$_{HDSTA}$	—		4.0	—	µs	The first clock pulse is gener-ated after this period.
LOW status hold time of SCL clock	t$_{LOW}$	—		4.7	—	µs	
HIGH status hold time of SCL clock	t$_{HIGH}$	—		4.0	—	µs	
Setup time for conditions for starting re-transmis-sion	t$_{SUSTA}$	—		4.7	—	µs	
Data hold time	t$_{HDDAT}$	—	—	0	—	µs	
Data setup time	t$_{SUDAT}$	—		250	—	ns	
Rising time of SDA and SCL signals	t$_R$	—		—	1000	ns	
Falling time of SDA and SCL signals	t$_F$	—		—	300	ns	
Setup time for stop con-ditions	t$_{SUSTO}$	—		4.0	—	µs	

Note : Only MB90675 series has I²C.
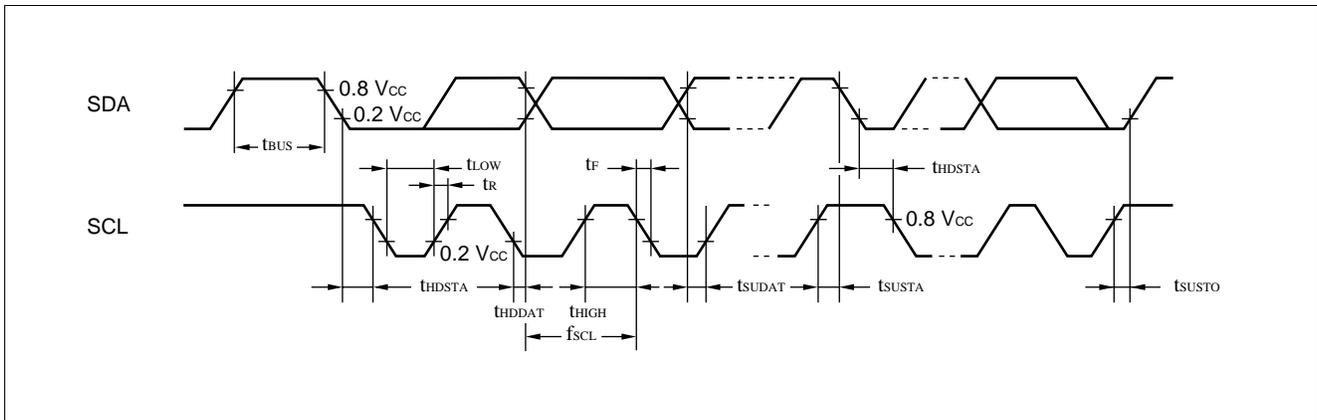
5. A/D Converter Electrical Characteristics

(AV$_{CC}$ = V$_{CC}$ = 2.7 V to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0.0 V, 2.7 V ≦ AVRH − AVRL, T$_A$ = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Min.	Typ.	Max.	Unit
				Value			
Resolution	—	—	—	—	—	10	bit
Total error	—	—		—	—	±3.0	LSB
Linearity error	—	—		—	—	±2.0	LSB
Differential linearity error	—	—		—	—	±1.5	LSB
Zero transition voltage	V$_{OT}$	AN0 to AN7		AVRL − 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	mV
Full-scale transition voltage	V$_{FST}$	AN0 to AN7		AVRH − 4.5 LSB	AVRH − 1.5 LSB	AVRH + 0.5 LSB	mV
Conversion time	—	—	V$_{CC}$ = 5.0 V ±10% at machine clock of 16 MHz	6.125	—	—	μs
	—	—	V$_{CC}$ = 3.0 V ±10% at machine clock of 8 MHz	12.25	—	—	μs
Analog port input current	I$_{AIN}$	AN0 to AN7		—	0.1	10	μA
Analog input voltage	V$_{AIN}$	AN0 to AN7		AVRL	—	AVRH	V
Reference voltage	—	AVRH	—	AVRL − 2.7	—	AV$_{CC}$	V
	—	AVRL		0	—	AVRH − 2.7	V
Power supply current	I$_A$	AV$_{CC}$		—	3	—	mA
	I$_{AH}$	AV$_{CC}$	Supply current when CPU stopped and A/D converter not in operation (V$_{CC}$ = AV$_{CC}$ = AVRH = 5.0 V)	—	—	5	μA
Reference voltage supply current	I$_R$	AVRH	—	—	200	—	μA
	I$_{RH}$	AVRH	Supply current when CPU stopped and A/D converter not in operation (V$_{CC}$ = AV$_{CC}$ = AVRH = 5.0 V)	—	—	5	μA
Offset between channels	—	AN0 to AN7	—	—	—	4	LSB

6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error:The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error:The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error:The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.

Total error

3FF

3FE

3FD

Actual conversion characteristics

0.5 LSB'

$\{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}$

Digital output

004

003

002

001

V_{NT} (Measured value)

Actual conversion characteristics

Theoretical characteristics

0.5 LSB'

AVRL   AVRH

Analog input
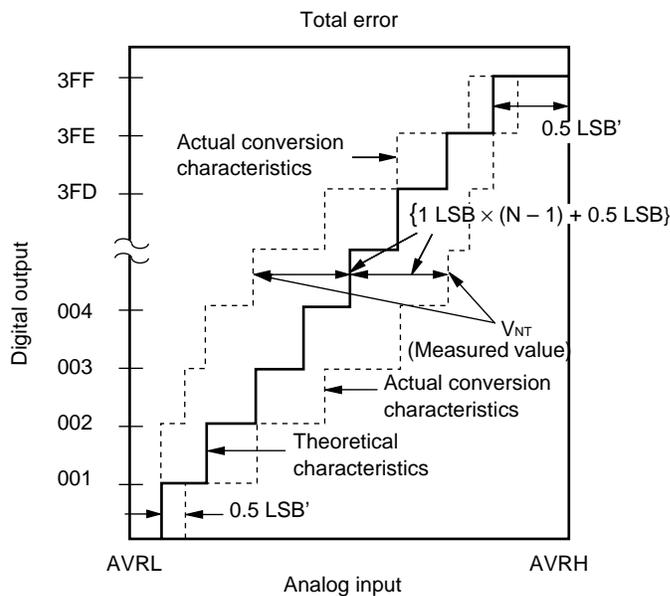
$1\ \text{LSB}' = (\text{Theoretical value})\ \dfrac{\text{AVRH} - \text{AVRL}}{1024}\ \text{[V]}$

$\text{Total error for digital output N} = \dfrac{V_{NT} - \{1\ \text{LSB}' \times (N - 1) + 0.5\ \text{LSB}'\}}{1\ \text{LSB}'}\ \text{[LSB]}$

$V_{OT}'\ (\text{Theoretical value}) = \text{AVRL} + 0.5\ \text{LSB}'\ \text{[V]}$

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

$V_{FST}'\ (\text{Theoretical value}) = \text{AVRH} - 1.5\ \text{LSB}'\ \text{[V]}$

(Continued)

(Continued)

Linearity error

Differential linearity error

Linearity error of digital output N $= \dfrac{V_{NT} - \{1\ LSB \times (N-1) + V_{OT}\}}{1\ LSB'}$ [LSB]

$1\ LSB = \dfrac{AVRH - AVRL}{1022}$ [V]

Differential linearity error of digital output N $= \dfrac{V_{(N+1)T} - V_{NT}}{1\ LSB'} - 1\ LSB$ [LSB]

V_{OT}: Voltage at transition of digital output from "000$_H$" to "001$_H$"
V_{FST}: Voltage at transition of digital output from "3FE$_H$" to "3FF$_H$"
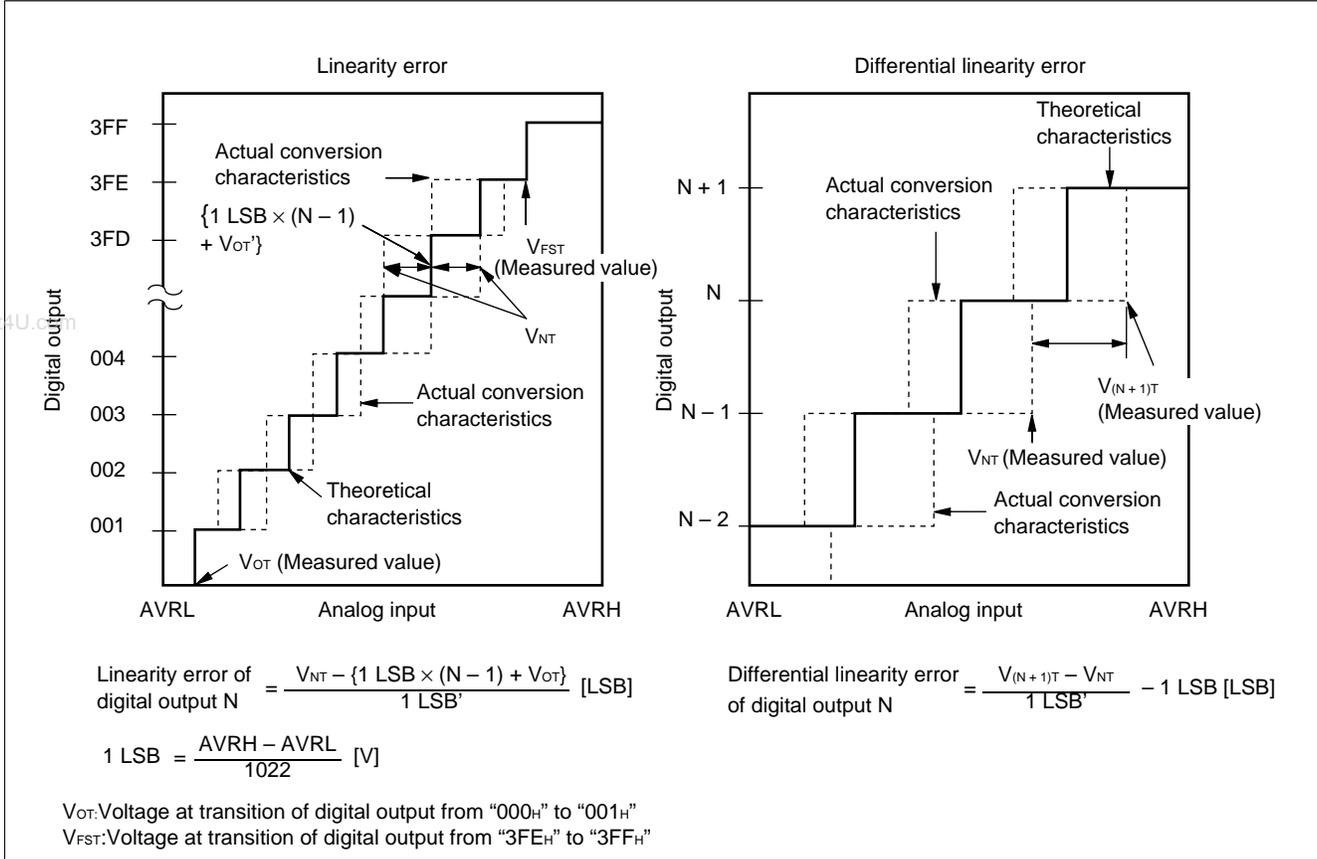
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions. Output impedance values of the external circuit of 7 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling time for analog voltages may not be sufficient (sampling time = 3.75 μs @machine clock of 16 MHz).

• Block diagram of analog input circuit model

R_{ON1}: Approx. 1.5 kΩ (V_{CC} = 5.0 V)
R_{ON2}: Approx. 0.5 kΩ (V_{CC} = 5.0 V)
R_{ON3}: Approx. 0.5 kΩ (V_{CC} = 5.0 V) C_0: Approx. 60 pF
R_{ON4}: Approx. 0.5 kΩ (V_{CC} = 5.0 V) C_1: Approx. 4 pF
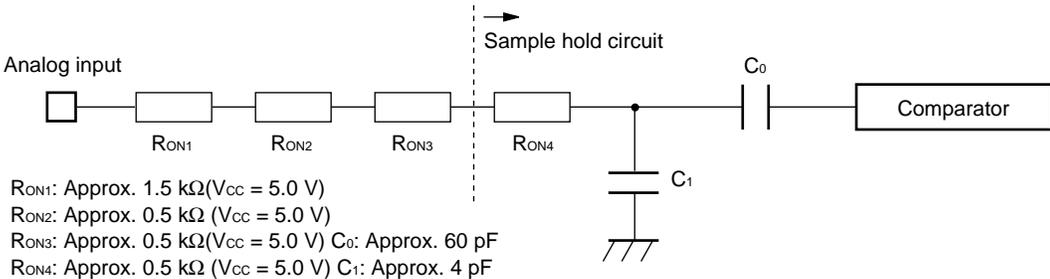
Note : Listed values must be considered as standards.

• Error

The smaller the | AVRH – AVRL |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

(1) "H" Level Output Voltage
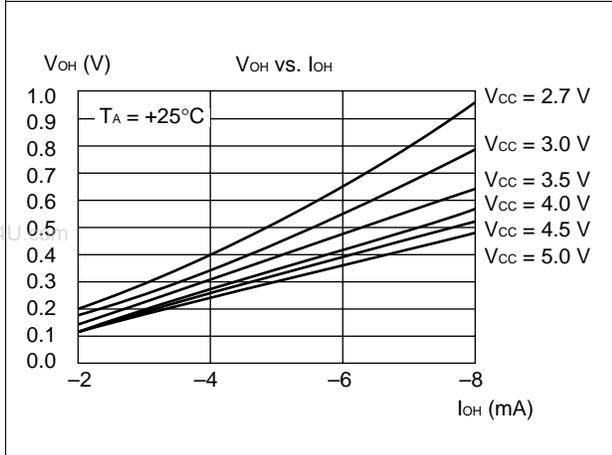
(2) "L" Level Output Voltage
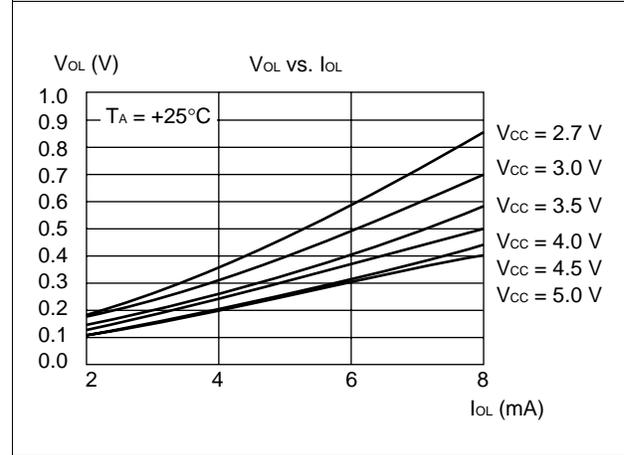
### (3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)
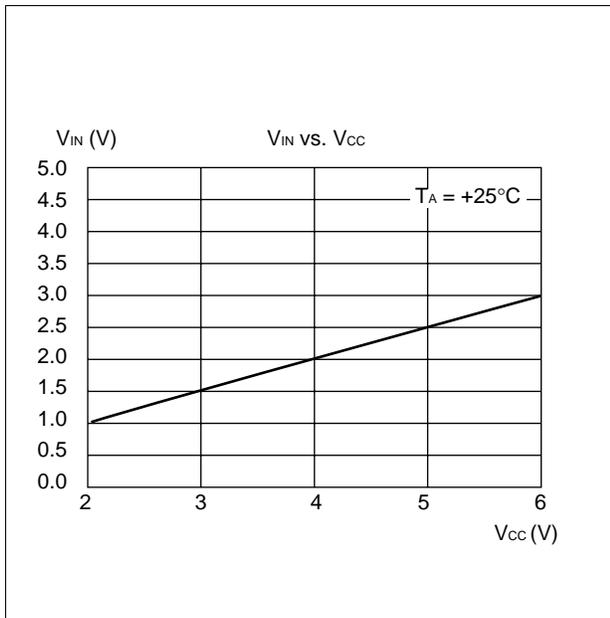
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

V_{IHS}:Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}:Threshold when input voltage in hysteresis characteristics is set to "L" level
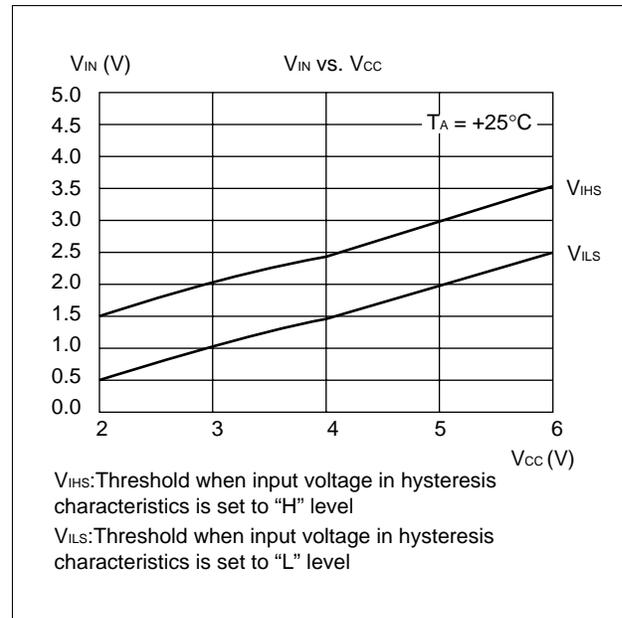
(5) Power Supply Current (f$_{CP}$ = Internal Operating Clock Frequency)
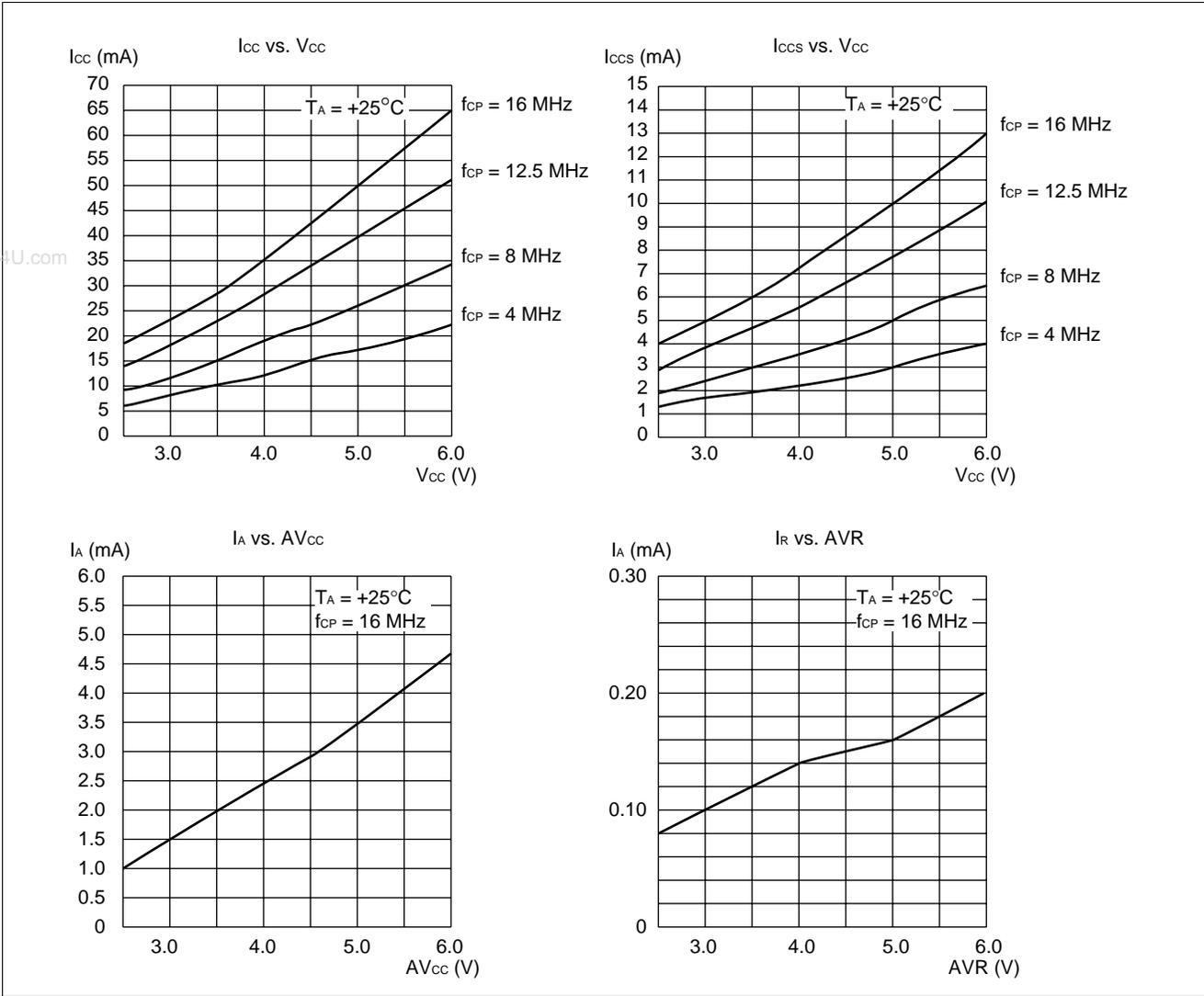
(6) Pull-up Resistance
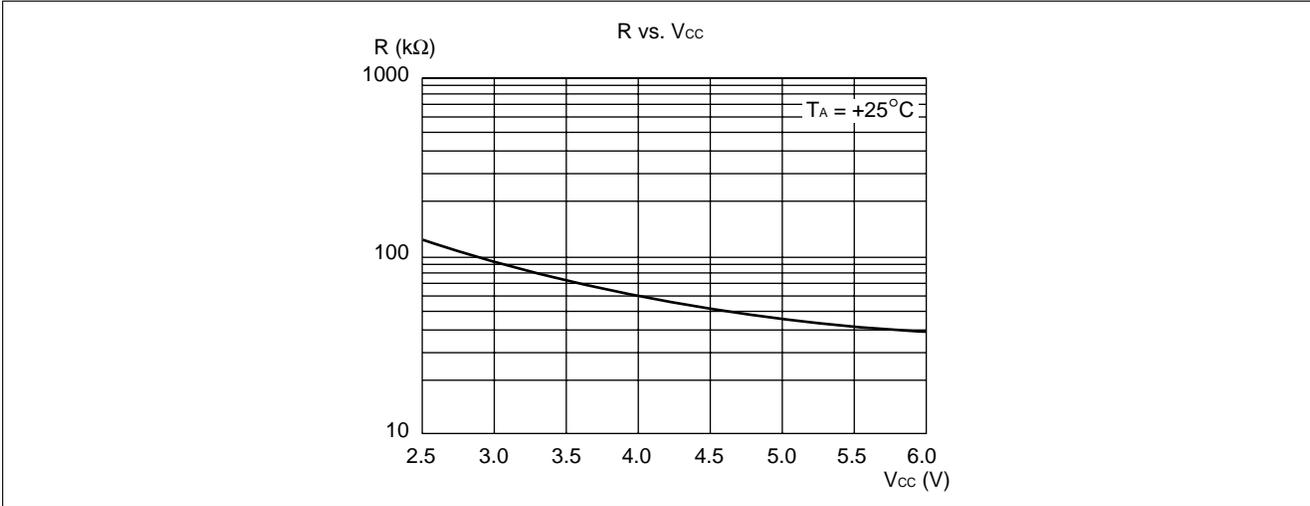
■ MASK OPTIONS

• MB90670 series

No.	Part number	MB90671 MB90672 MB90673	MB90P673	MB90V670
	Specifying procedure	Specify when ordering masking	Set with EPROM pro-grammer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P67, P70 to P77, P80, $\overline{RST}$, MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor
2	Pull-down resistors MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor

• MB90675 series

No.	Part number	MB90676 MB90677 MB90678	MB90P678	MB90V670
	Specifying procedure	Specify when ordering masking	Set with EPROM pro-grammer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P67, P70 to P77, P80 to P86, P90, P91, PA0 to PA7, PB0 to PB2, $\overline{RST}$, MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor
2	Pull-down resistors MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor

Notes : • The pull-up register configured as a port pin is switched-off in the stop mode and during the hardware standby.

• In turning on power, option settings can not be made until clocks are supplied because 8 machine cycles are needed for option settings for the MB90P670/P675.

■ **ORDERING INFORMATION**

Part number	Package	Remarks
MB90671PFV MB90672PFV MB90673PFV MB90T673PFV MB90P673PFV	80-pin Plastic LQFP (FPT-80P-M05)	
MB90671PF MB90672PF MB90673PF MB90T673PF MB90P673PF	80-pin Plastic QFP (FPT-80P-M06)	
MB90676PFV MB90677PFV MB90678PFV MB90T678PFV MB90P678PFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90676PF MB90677PF MB90678PF MB90T678PF MB90P678PF	100-pin Plastic QFP (FPT-100P-M06)	

■ PACKAGE DIMENSIONS

80-pin Plastic LQFP
(FPT-80P-M05)

Note: pins width and pins thickness include plating thickness.

14.00±0.20(.551±.008)SQ
12.00±0.10(.472±.004)SQ

0.145±0.055
(.006±.002)

(Mounting height)

0.08(.003)

INDEX

LEAD No. ①

0.50(.020)

0.20±0.05
(.008±.002)

0.08(.003) Ⓜ

Details of "A" part

$1.50^{+0.20}_{-0.10}$ (Mounting height)
$(.059^{+.008}_{-.004})$

0.10±0.10
(.004±.004)
(Stand off)

0°~8°

0.25(.010)

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

"A"
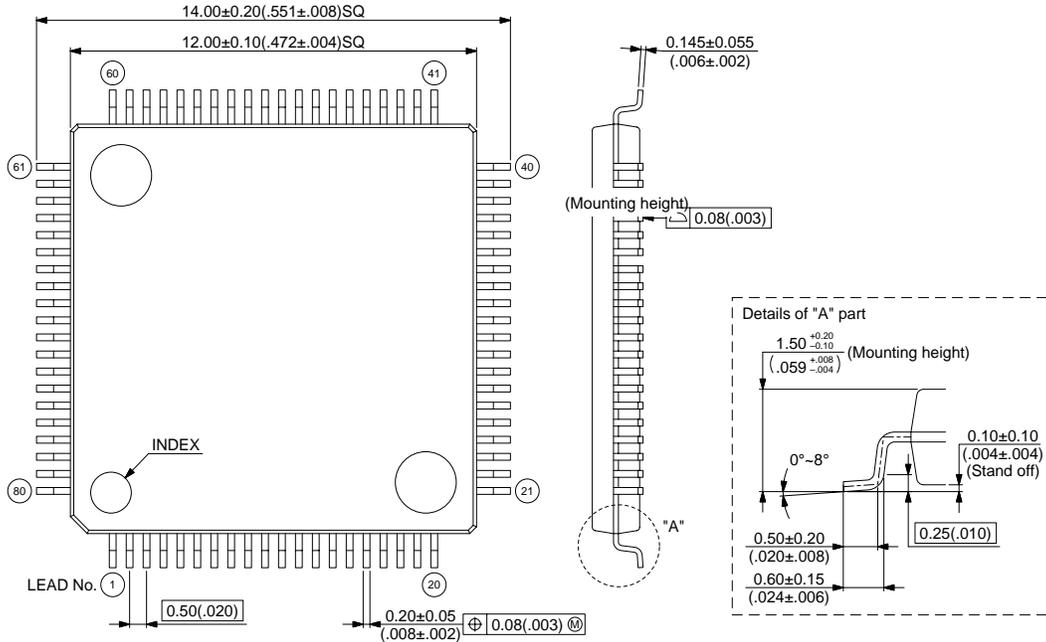
© 2000 FUJITSU LIMITED F80008S-c-3-7

Dimensions in mm (inches)

80-pin Plastic QFP
(FPT-80P-M06)

Note: pins width and pins thickness include plating thickness.

23.90±0.40(.941±.016)
20.00±0.20(.787±.008)

0.10(.004)

17.90±0.40
(.705±.016)
14.00±0.20
(.551±.008)

INDEX

0.80(.031)

0.37±0.05
(.015±.002)

0.20(.008) Ⓜ

0.17±0.06
(.007±.002)

Details of "A" part

$3.05^{+0.30}_{-0.20}$
$(.120^{+.012}_{-.008})$
(Mounting height)

0.25(.010)

0°~8°

0.80±0.20
(.031±.008)

0.88±0.15
(.035±.006)

$0.30^{+0.10}_{-0.25}$
$(.012^{+.004}_{-.010})$
(Stand off)

"A"
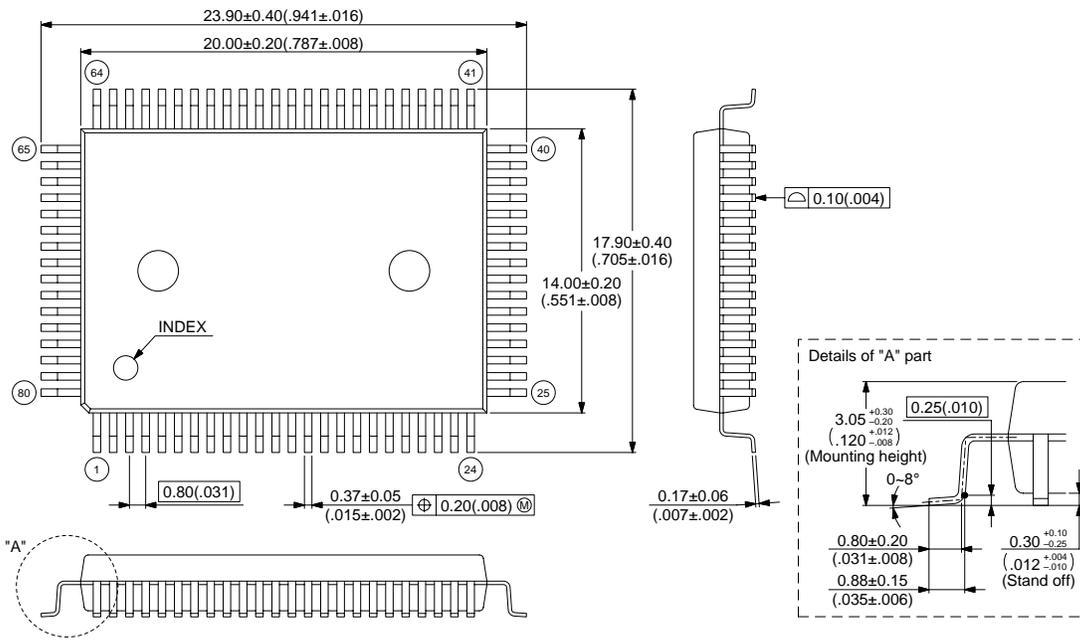
© 2001 FUJITSU LIMITED F80010S-c-4-4

Dimensions in mm (inches)

(Continued)

100-pin Plastic LQFP (FPT-100P-M05)

Note: pins width and pins thickness include plating thickness.

16.00±0.20(.630±.008)SQ
14.00±0.10(.551±.004)SQ

75   51
76   50
INDEX
100   26
1   25
0.50(.020)
0.20±0.05 (.008±.002)   ⊕ 0.08(.003) Ⓜ
0.145±0.055 (.0057±.0022)
0.08(.003)
"A"

Details of "A" part
1.50 $^{+0.20}_{-0.10}$ (.059 $^{+.008}_{-.004}$) (Mounting height)
0.10±0.10 (.004±.004) (Stand off)
0°~8°
0.50±0.20 (.020±.008)
0.60±0.15 (.024±.006)
0.25(.010)
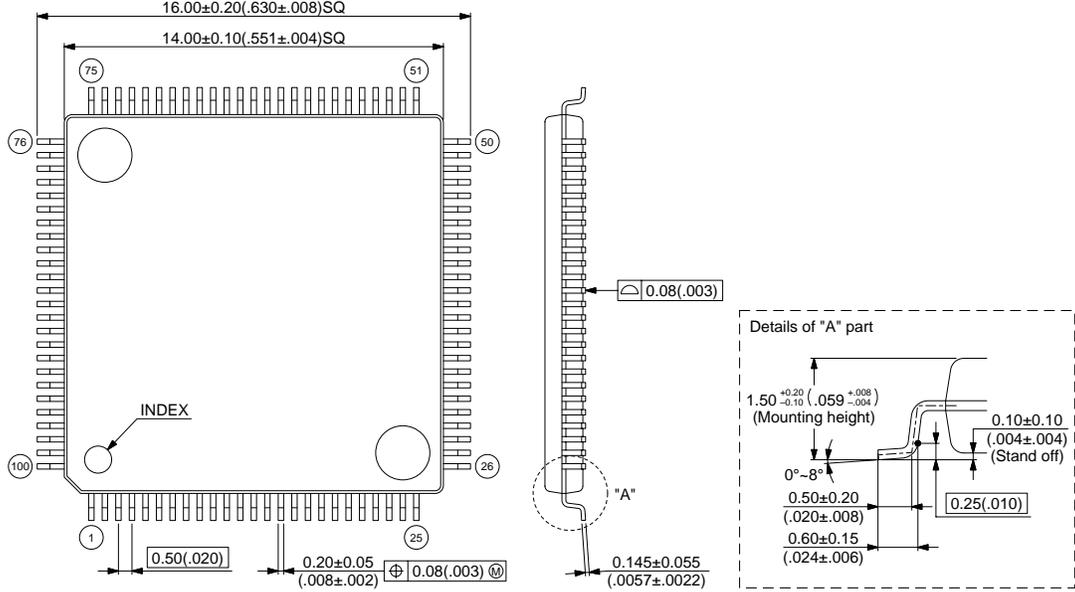
© 2000 FUJITSU LIMITED F100007S-3c-5

Dimensions in mm (inches)

100-pin Plastic QFP (FPT-100P-M06)

Note: pins width and pins thickness include plating thickness.

23.90±0.40(.941±.016)
20.00±0.20(.787±.008)

80   51
81   50
INDEX
100   31
1   30
0.65(.026)
0.32±0.05 (.013±.002)   ⊕ 0.13(.005) Ⓜ
17.90±0.40 (.705±.016)
14.00±0.20 (.551±.008)
0.10(.004)
0.17±0.06 (.007±.002)
"A"

Details of "A" part
3.00 $^{+0.35}_{-0.20}$ (.118 $^{+.014}_{-.008}$) (Mounting height)
0.25(.010)
0~8°
0.80±0.20 (.031±.008)
0.88±0.15 (.035±.006)
0.25±0.20 (.010±.008) (Stand off)
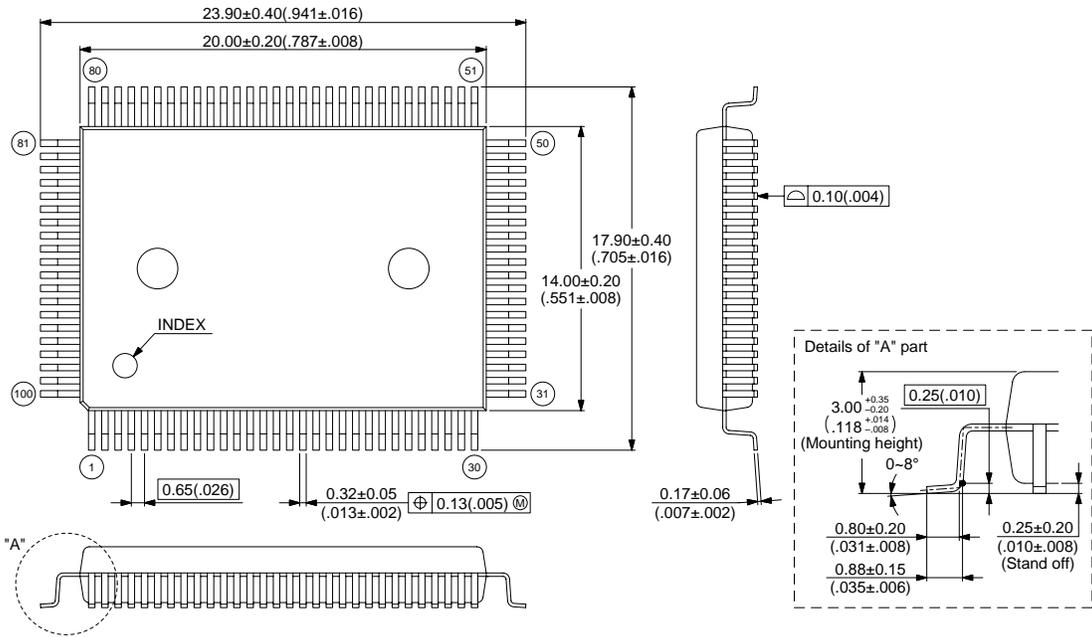
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Dimensions in mm (inches)

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