M5L8251AP-5

PROGRAMMABLE COMMUNICATION INTERFACE

T-75-37-07

DESCRIPTION

The M5L8251AP-5 is a universal synchronous/asynchronous receiver/transmitter (USART) IC chip designed for data communications use. It is produced using the N-channel silicon-gate ED-MOS process and is mainly used in combination with 8-bit microprocessors.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Synchronous and asynchronous operation
  - Synchronous:
    - 5~8-bit characters
    - Internal or external synchronization
    - Automatic SYNC character insertion
  - Asynchronous system:
    - 5~8-bit characters
    - Clock rate—1, 16or 64 times the baud rate
    - 1, 1½, or 2 stop bits
    - False-start-bit detection
    - Automatic break-state detection
- Baud rate: DC~64k-baud
- Full duplex, double-buffered transmitter/receiver
- Error detection: parity, overrun, and framing

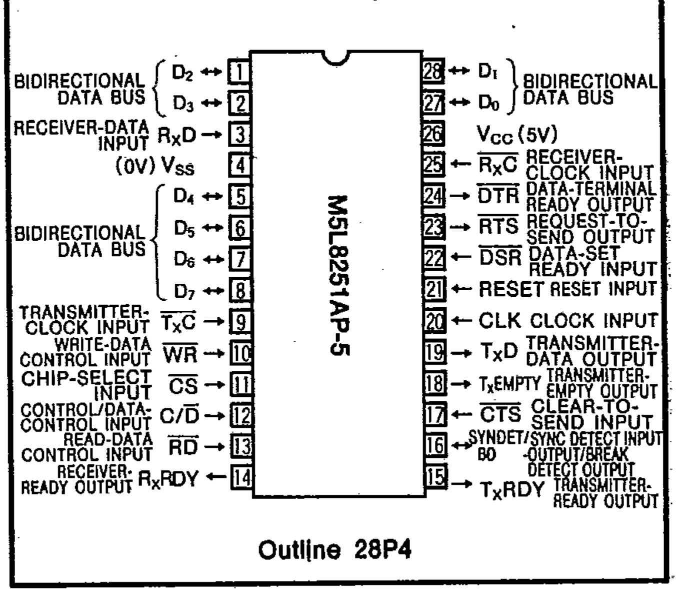
APPLICATION

Modem control of data communications using microcomputers. Control of CRT, TTY and other terminal equipment

FUNCTION

The M5L8251AP-5 is used in the peripheral circuits of a CPU. It permits assignments, by means of software, of operations in all the currently used serial-data transfer systems. The M5L8251AP-5 receives parallel-format data from the CPU, converts it into a serial format, and then transmits via the T_XD pin. It also receives data sent in via the R_XD pin from the external circuit, and converts it into a parallel format for sending to the CPU. On receipt of parallel-format data for transmission from the CPU or serial data for the CPU from external devices, the M5L8251AP-5 informs the CPU using the T_XRDY or R_XRDY pin. In addition, the CPU can read the M5L8251AP-5 status at any time. The M5L8251AP-5 can detect the data received for errors and inform the CPU of the presence of errors as status information. Errors include parity, overrun and frame errors.

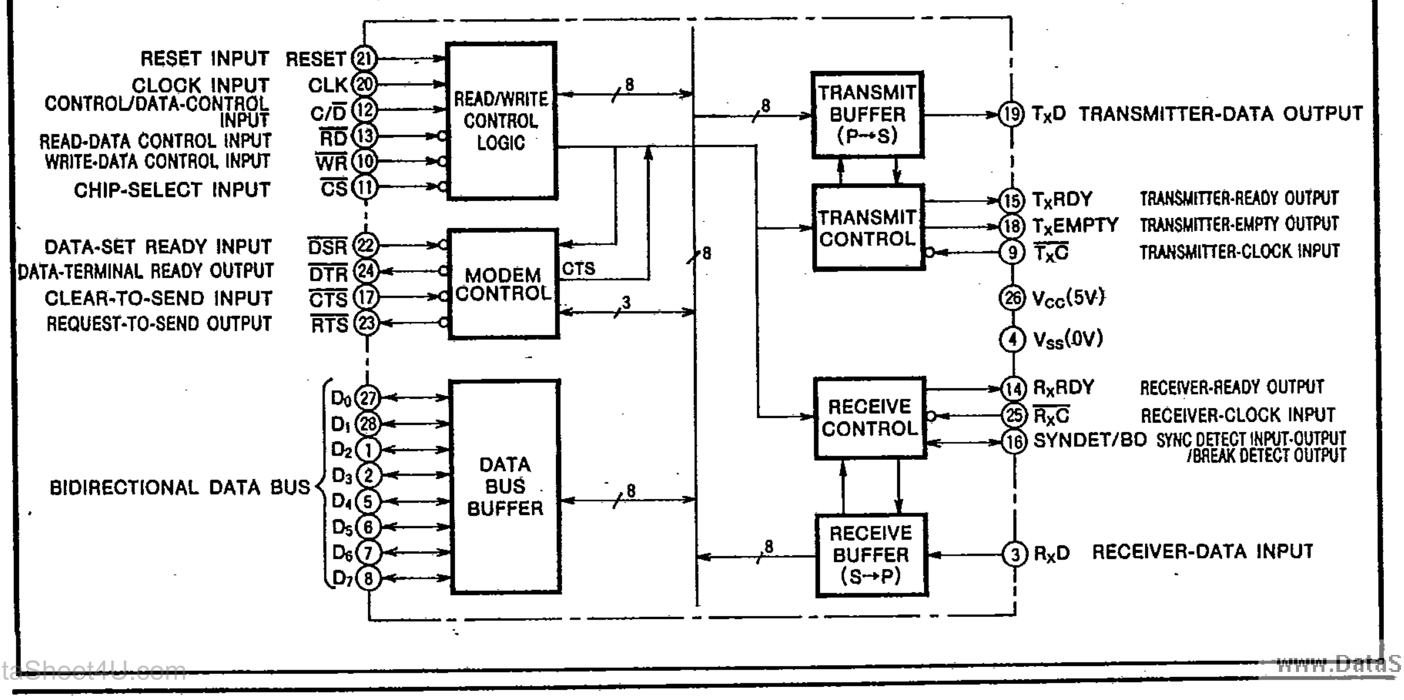
PIN CONFIGURATION (TOP VIEW)



BIDIRECTIONAL DATA BUS
D2 1
D3 2
RECEIVER-DATA INPUT RxD 3
(0V) Vss 4
BIDIRECTIONAL DATA BUS
D4 5
D5 6
D6 7
D7 8
TRANSMITTER-CLOCK INPUT TxC 9
WRITE-DATA CONTROL INPUT WR 10
CHIP-SELECT INPUT CS 11
CONTROL/DATA-CONTROL INPUT C/D 12
READ-DATA CONTROL INPUT RD 13
RECEIVER-READY OUTPUT RxRDY 14
M5L8251AP-5
28 D1 BIDIRECTIONAL DATA BUS
27 D0
26 Vcc (5V)
25 RxC RECEIVER-CLOCK INPUT
24 DTR DATA-TERMINAL READY OUTPUT
23 RTS REQUEST-TO-SEND OUTPUT
22 DSR DATA-SET READY INPUT
21 RESET RESET INPUT
20 CLK CLOCK INPUT
19 TxD TRANSMITTER-DATA OUTPUT
18 TxEMPTY TRANSMITTER-EMPTY OUTPUT
17 CTS CLEAR-TO-SEND INPUT
16 SYNDET/BD SYNC DETECT INPUT-OUTPUT/BREAK DETECT OUTPUT
15 TxRDY TRANSMITTER-READY OUTPUT

Outline 28P4

BLOCK DIAGRAM



RESET INPUT RESET 21
CLOCK INPUT CLK 20
CONTROL/DATA-CONTROL INPUT C/D 12
READ-DATA CONTROL INPUT RD 13
WRITE-DATA CONTROL INPUT WR 10
CHIP-SELECT INPUT CS 11
READ/WRITE CONTROL LOGIC
8
DATA-SET READY INPUT DSR 22
DATA-TERMINAL READY OUTPUT DTR 24
CLEAR-TO-SEND INPUT CTS 17
REQUEST-TO-SEND OUTPUT RTS 23
MODEM CONTROL
CTS
3
BIDIRECTIONAL DATA BUS
D0 27
D1 28
D2 1
D3 2
D4 5
D5 6
D6 7
D7 8
DATA BUS BUFFER
TRANSMIT BUFFER (P→S)
TRANSMIT CONTROL
RECEIVE CONTROL
RECEIVE BUFFER (S→P)
19 TxD TRANSMITTER-DATA OUTPUT
15 TxRDY TRANSMITTER-READY OUTPUT
18 TxEMPTY TRANSMITTER-EMPTY OUTPUT
9 TxC TRANSMITTER-CLOCK INPUT
26 Vcc(5V)
4 Vss(0V)
14 RxRDY RECEIVER-READY OUTPUT
25 RxC RECEIVER-CLOCK INPUT
16 SYNDET/BD SYNC DETECT INPUT-OUTPUT /BREAK DETECT OUTPUT
3 RxD RECEIVER-DATA INPUT

OPERATION

The M5L8251AP-5 interfaces with the system bus as shown in Fig.1, positioned between the CPU and the modem or terminal equipment, and offers all the functions required for data communication.

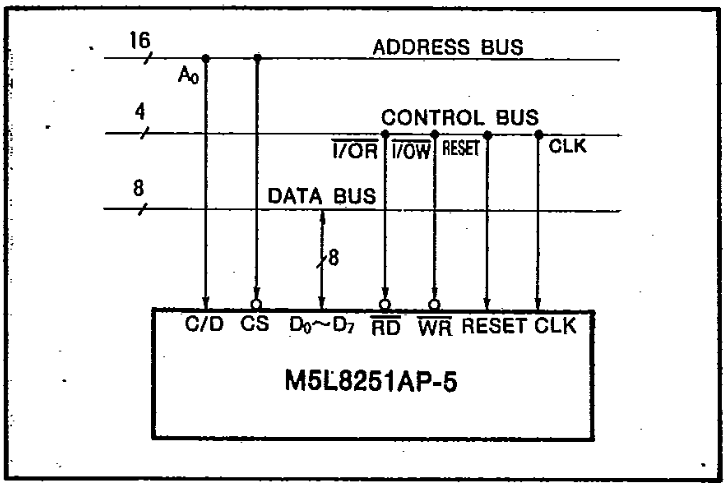


Fig. 1 M5L8251AP-5 interface to CPU system bus

When using the M5L8251AP-5, it is necessary to program, as the initial setting, assignments for synchronous/asynchronous mode selection, baud rate, character length, parity check, and even/odd parity selection in accordance with the communication system used. Once programming is completed, functions appropriate to the communication system can be carried out continuously.

When initial setting of the USART is completed, data communication becomes possible. Though the receiver is always in the enable state, the transmitter is placed in the transmitter-enable state (T_XEN) by a command instruction, and the application of a low-level signal to the $\overline{CTS}$ pin prompts data-transfer start-up. Until this condition is satisfied, transmission is not executed. On receiving data, the receiver informs the CPU that reading for the receiver data in the USART by the CPU has become possible (the R_XRDY terminal has turned to high-level). Since data reception and the entry of the CPU into the data-readable state are output as status information, the CPU can access USART status without accessing the R_XRDY terminal.

During receiving operation, the USART checks errors and gives out status information. There are three types of errors: parity, overrun, and frame. Even though an error occurs, the USART continues its operations, and the error state is retained until error reset (ER) is effected by a command instruction. The M5L8251AP-5 access methods are listed in Table 1.

Table 1 M5L8251AP-5 Access Methods

$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
L	L	H	L	Data bus ← Data in USART
L	H	L	L	USART ← Data bus
H	L	H	L	Data bus ← Status
H	H	L	L	Control ← Data bus
X	H	H	L	3-State ← Data bus
X	X	X	H	3-State ← Data bus

Read/Write Control Logic

This logic consists of a control word register and command word register. It receives signals from the CPU control bus and generates internal-control signals for the elements.

Modem Control Circuit

This is a general-purpose control-signal circuit designed to simplify the interface to the modem. Four types of control signal are available: output signals $\overline{DTR}$ and $\overline{RTS}$ are controlled by command instructions, input signal $\overline{DSR}$ is given to the CPU as status information and input signal $\overline{CTS}$ controls direct transmission.

Data-Bus Buffer

This is an 8-bit 3-state bidirectional bus through which control words, command words, status information, and transfer data are transferred. Fig. 2 shows the structure of the data-bus buffer.

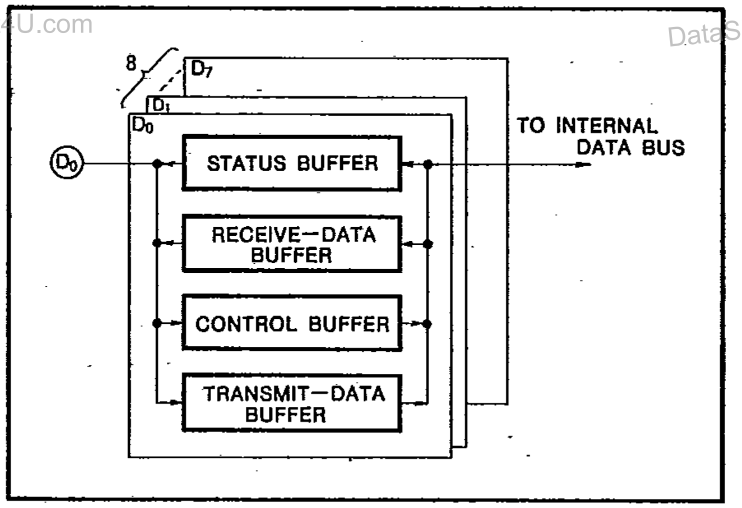


Fig. 2 Data-bus-buffer structure

Transmit Buffer

This buffer converts parallel-format data given to the data-bus buffer in to serial data with addition of a start bit, stop bits and a parity bit, and sends out the converted data through the T_XD pin based on the control signal.

Transmit-Control Circuit

This circuit carries out all the controls required for serial data transmission. It controls transmitter data and outputs the signals required by external devices in accordance with the instructions of the read/write control logic.

Receive Control Circuit

This circuit offers all the controls required for normal reception of the input serial data. It controls receiver data and outputs signals for the external devices in accordace with the instructions of the read/write control logic.

Receive Buffer

This buffer converts serial data given via the R_XD pin into a parallel format, checks the bits and characters in accordance with the communication format designated by mode setting, and transfers the assembled characters to the CPU via the data-bus buffer.

Receiver-Data Input (R_XD)

Serial characters sent from another device are input to this pin and converted to a parallel-character format to serve as data for the CPU. Unless the high-level state is detected after a chip-master reset procedure (this resetting is carried out to prevent spurious operation such as that due to faulty connection of the R_XD to the line in a break state), the serial characters are not received. This applies to only the asynchronous mode. When the R_XD line enters the low-level state instantaneously because of noise, etc, the mis-start prevention function starts working. That is, the start bit is detected by its falling edge but in order to make sure that it is the correct start bit, the R_XD line is strobed at the middle of the start bit to reconfirm the low-level state. If it is found to be high-level a faulty-start judgment is made.

Transmitter-Clock Input ($\overline{T_XC}$)

This clock controls the baud rate for character transmission from the T_XD pin. Serial data is shifted by the falling edge of the $\overline{T_XC}$ signal. In the synchronous mode, the $\overline{T_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by the mode setting.

Example When the baud rate is 110 bauds:

$\overline{T_XC}$=110Hz(1X)
$\overline{T_XC}$=1.76kHz(16X)
$\overline{T_XC}$=7.04kHz(64X)

Write-Data Control Input ($\overline{WR}$)

Data and control words output from the CPU by the low-level input are written in the M5L8251AP-5. This terminal is usually used in a form connected with the control bus $\overline{I/OW}$ of the CPU.

Chip-Select Input ($\overline{CS}$)

This is a device-select signal that enables the USART by a low-level input. Usually, it is connected to the address bus directly or via the decoder. When this signal is in the high-level state, the M5L8251AP-5 is disabled.

Control/Data Control Input (C/$\overline{D}$)

This signal shows whether the information on the USART data bus is in the form of data characters or control words, or in the form of status information, in accordance with the $\overline{RD}$ and $\overline{WR}$ inputs while the CPU is accessing the M5L8251AP-5. The high-level identifies control words or status information, and the low-level, data characters.

Read-Data Control Input ($\overline{RD}$)

Receiver data and status information are output from the CPU by a low-level input for the CPU data bus.

Receiver-Ready Output (R_XRDY)

This signal indicates that the received characters have entered the receiver buffer, and further, the receiver-data buffer in the data-bus buffer shown in Fig. 2. It is possible to confirm the R_XRDY status by using this signal as an interruption signal for the CPU or by allowing the CPU to read the D_1 bit of the status information by polling. The R_XRDY is automatically reset when a character is read by the CPU. Even in the break state in which the R_XD line is held at low-level, the R_XRDY remains active. It can be masked by making the $R_XE(D_2)$ of the command instruction 0.

Transmitter-Ready Output (T_XRDY)

This signal shows that the data is ready for transmission. It is possible to confirm the status of serial-data transmission by using it as an interruption signal for the CPU or by allowing the CPU to read the D_0 bit of the status information by polling. Since the T_XRDY signal shows that the data buffer is empty, it is automatically reset when a transmission character is loaded by the CPU. The T_XRDY bit of the status information means that the transmit-data buffer shown in Fig. 2 has become empty, while the T_XRDY pin enters the high-level state only when the transmit-data buffer is empty, T_XEN equals 1, and a low-level input has been applied to the $\overline{CTS}$ pin.

Status (D_0): When transmit-data buffer (TDB) is empty, it becomes 1.

T_XRDY terminal: When (TDB is empty)·(T_XEN=1)·($\overline{CTS}$ = "L") = "H" or resetting, it becomes active.

Sync Detect/Break Detect Output-Input (SYNDET/BD)

In the synchronous mode this pin is used for input and output operations. When it is specified for the internal synchronous mode by mode setting, this pin works as an output terminal. It enters the high-level state when a SYNC character is received through the R_XD pin. If the M5L8251AP-5 has been programmed for double SYNC characters (bi-sync), a high-level is entered in the middle of the last bit of the second SYNC character. This signal is automatically reset by reading the status information.

On designation of the M5L8251AP-5 to the external synchronous mode, this pin begins to serve for input operations. Applying a high-level signal to this pin prompts the M5L8251AP-5 to begin assembling data characters at the next rising edge of the $\overline{R_XC}$. For the width of a high-level signal to be input, a minimum $\overline{R_XC}$ period is required.

Designation of the asynchronous mode causes this pin to function as a BD (output) pin. When the start, data, and parity bits and stop bits are all 0 for two characters period, a high-level is entered. The BD (break detect) signal can also be read as the D_6 bit of the status information. This signal is reset by resetting the chip master or by the R_XD line's recovering the high-level state.

Clear-To-Send Input ($\overline{CTS}$)

When the T_XEN bit (D_0) of the command instruction has been set to 1 and the $\overline{CTS}$ input is low-level serial data is sent out from the T_XD pin. Usually this is used as a clear-to-send signal for the modem.

Note: CTS indicates the modem status as follows:
ON means data transmission is possible;
OFF means data transmission is impossible.

Transmitter-Empty Output (T_XEMPTY)

When no transmisison characters are left in the transmit buffer, this pin enters the high-level state. In the asynchronous mode, the following transmission character is shifted to the transmit buffer when it is loaded from the CPU. Thus, it is automatically reset. In the synchronous mode, a SYNC character is loaded automatically on the transmit buffer when no transfer-data characters are left. In this case, however, the T_XEMPTY does not enter the low-level state when a SYNC character has been sent out, since T_XEMPTY="H" denotes the state in which there is no transfer character and one or two SYNC characters are being transferred or the state in which a SYNC character is being transferred as a filler. T_XEMPTY is unrelated to the T_XEN bit of the command instruction.

Transmission-Data Output (T_XD)

Parallel-format transmission characters loaded on the M5L8251AP-5 by the CPU are assembled into the format designated by the mode instruction and sent in serial-data form via the T_XD pin. Data is output, however, only in cases where the D_0 bit (T_XEN) of the command instruction is 1 and the $\overline{CTS}$ terminal is in the low-level state. Once reset, this pin is kept at the mark status (high level) until the first character is sent.

Clock Input (CLK)

This system-clock input is required for internal-timing generation and is usually connected to the clock-output (CLK) pin of the M5L8085AP. Although there is no direct relation with the data-transfer baud rate, the clock-input (CLK) frequency is more than 30 times the $\overline{T_XC}$ or $\overline{R_XC}$ input frequency in the case of the synchronous system and more than 4.5 times in the case of the asynchronous system.

Reset Input (RESET)

Once the USART is shifted to the idle mode by a high-level input, this state continues until a new control word is set. Since this is a master reset, it is always necessary to load a control word following the reset process. The reset input requires a minimum 6-clock pulse width.

Data-Set Ready Input ($\overline{DSR}$)

This is a general-purpose input signal, but is usually used as a data-set ready signal to test modem status. Its status can be known from the status reading process. The D_7 bit of the status information equals 1 when the $\overline{DSR}$ pin is in the low-level state, and 0 when in the high-level state.

$\overline{DSR}$="L"→D_7 bit of status information=1
$\overline{DSR}$="H"→D_7 bit of status information=0

Note: DSR indicates modem status as follows:
ON means the modem can transmit and receive;
OFF means it cannot.

Request-To-Send Output ($\overline{RTS}$)

This is a general-purpose output signal but is used as a request-to-send signal for the modem. The $\overline{RTS}$ terminal is controlled by the D_5 bit of the command instruction. When D_5 is equal to 1, $\overline{RTS}$="L", and when D_5 is 0, $\overline{RTS}$="H".

Command register D_5=1→$\overline{RTS}$="L"
Command register D_5=0→$\overline{RTS}$="H"

Note: RTS controls the modem transmission carrier as follows:
ON means carrier dispatch;
OFF means carrier stop.

Data-Terminal Ready Output ($\overline{DTR}$)

This is a general-purpose output signal, but is usually used as a data-terminal ready or rate-select signal to the modem. The $\overline{DTR}$ pin is controlled by the D_1 bit of the command instruction; if D_1=1, $\overline{DTR}$="L", and if D_1=0, $\overline{DTR}$="H".

D_1 of the command register=1→$\overline{DTR}$="L"
D_1 of the command register=0→$\overline{DTR}$="H"

Receiver-Clock Input ($\overline{R_XC}$)

This clock signal controls the baud rate for the sending in of characters via the $\overline{R_XD}$ pin. The data is shifted in by the rising edge of the $\overline{R_XC}$ signal. In the synchronous mode, the $\overline{R_XC}$ frequency is equal to the actual baud rate. In the asynchronous mode, the frequency is specified as 1, 16, or 64 times the baud rate by mode setting. This relationship is parallel to that of $\overline{T_XC}$, and in usual communication-line systems the transmission and reception baud rates are equal. The $\overline{T_XC}$ and $\overline{R_XC}$ terminals are, therefore, used connected to the same baud-rate generator.

PROGRAMMING

It is necessary for the M5L8251AP-5 to have the control word loaded by the CPU prior to data transfer. This must always be done following any resetting operation (by external RESET pin or command instruction IR). There are two types of control words: mode instructions specifying general operations required for communications and command instructions to control the M5L8251AP-5 actual operations.

Following the resetting operation, a mode instruction must be set first. This instruction sets the synchronous or asynchronous system to be used. In the sysnchronous system, a SYNC character is loaded from the CPU. In the case of the bi-sync system, however, a second SYNC character must be loaded in succession.

Loading a command instruction makes data transfer possible. This operation after resetting must be carried out for initializing the M5L8251AP-5. The USART command instruction contains an internal-reset IR instruction (D_6bit) that makes it possible to return the M5L8251AP-5 to its reset state. The initialization flowchart is shown in Fig. 3 and the mode-instruction and command-instruction formats are shown in Figs. 4 and 5.

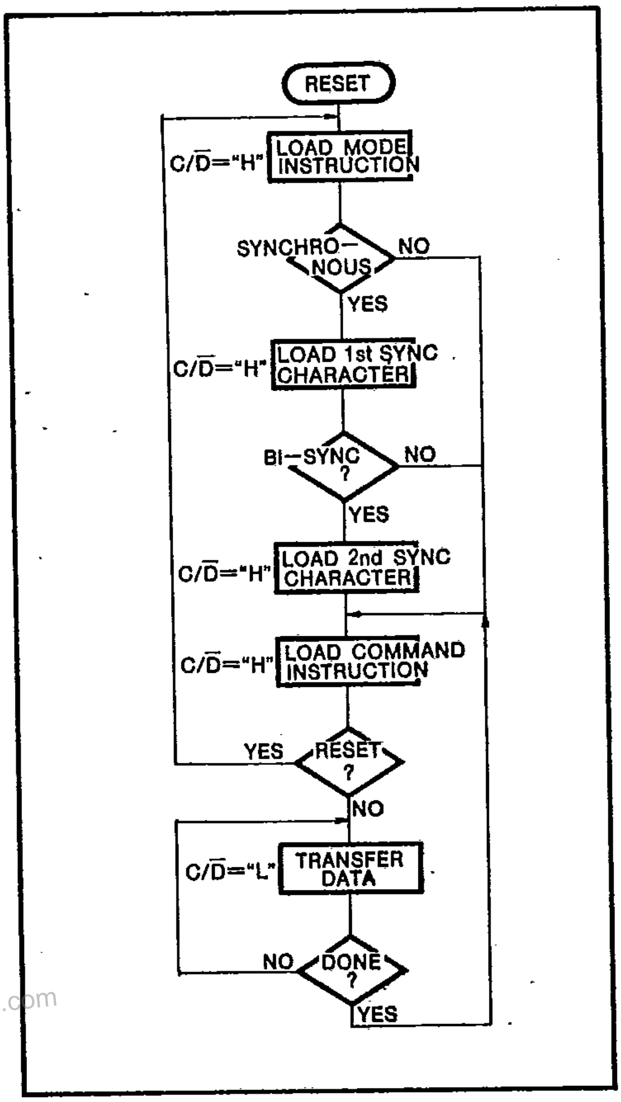


Fig. 3 Initialization flow chart

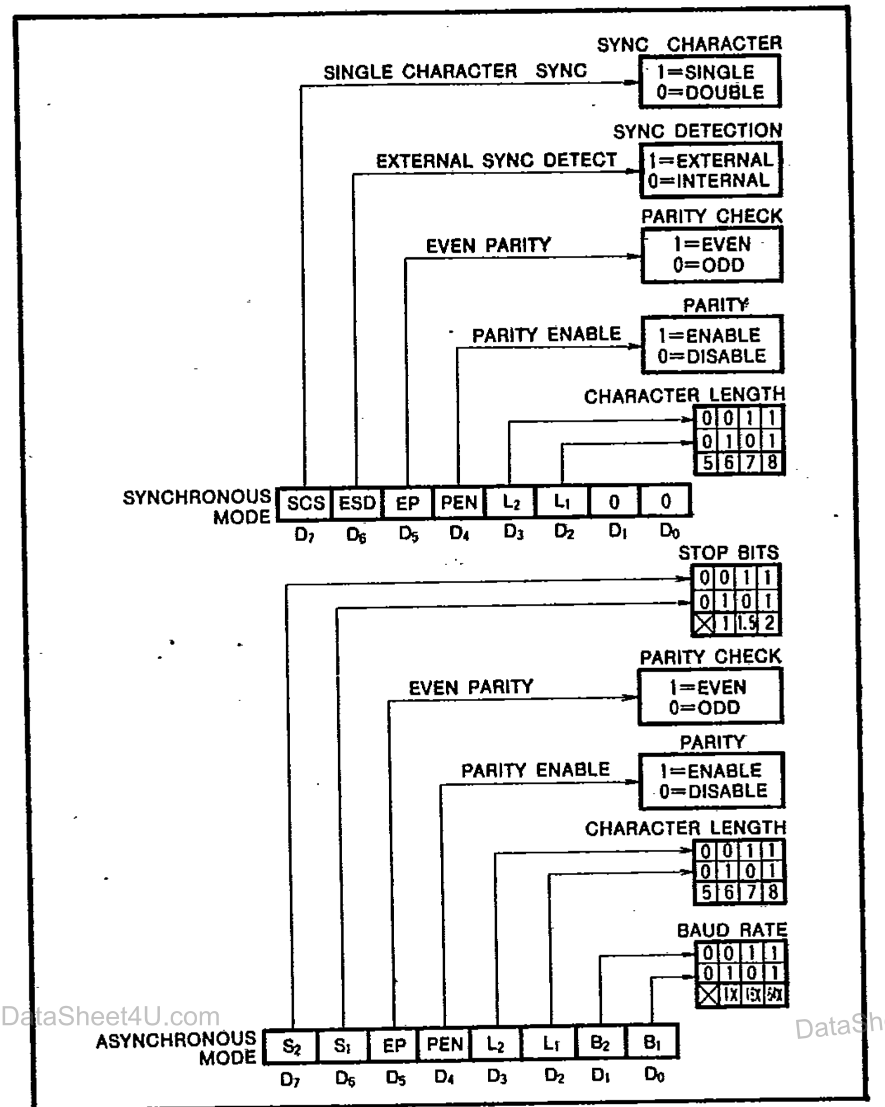


Fig. 4 Mode-instruction format (C/D̄="H", W̄R̄="L")

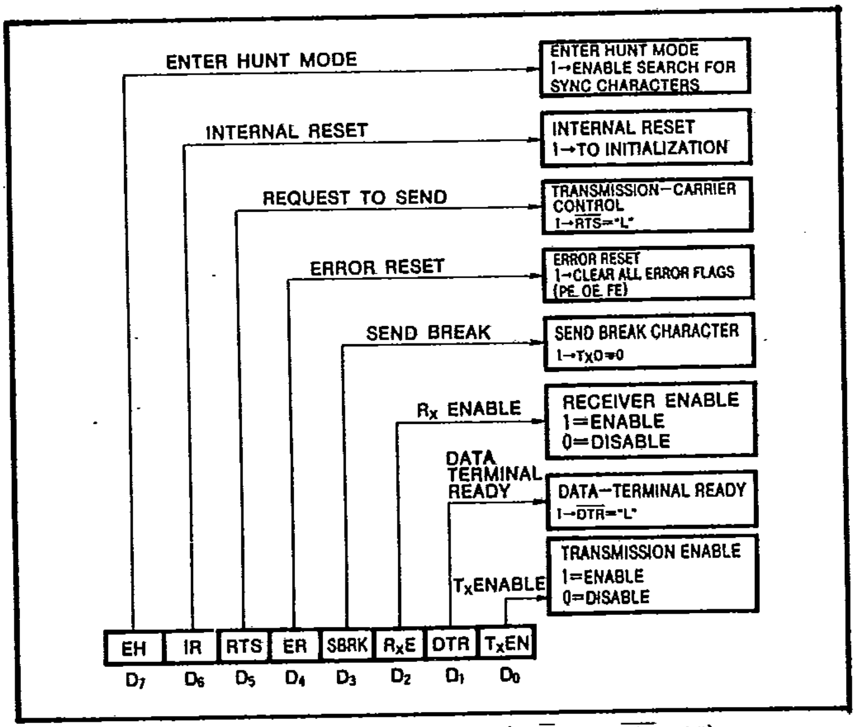

ENTER HUNT MODE
ENTER HUNT MODE 1→ENABLE SEARCH FOR SYNC CHARACTERS
INTERNAL RESET
INTERNAL RESET 1→TO INITIALIZATION
REQUEST TO SEND
TRANSMISSION-CARRIER CONTROL 1→R̄T̄S̄="L"
ERROR RESET
ERROR RESET 1→CLEAR ALL ERROR FLAGS (PE, OE, FE)
SEND BREAK
SEND BREAK CHARACTER 1→TxD=0
Rx ENABLE
RECEIVER ENABLE 1=ENABLE 0=DISABLE
DATA TERMINAL READY
DATA-TERMINAL READY 1→D̄T̄R̄="L"
TxENABLE
TRANSMISSION ENABLE 1=ENABLE 0=DISABLE
EH IR RTS ER SBRK RxE DTR TxEN
D7 D6 D5 D4 D3 D2 D1 D0

Fig. 5 Command-instruction format (C/D̄="H", W̄R̄="L")

Asynchronous Transmission Mode

When data characters are loaded on the M5L8251AP-5 after initial setting, the USART automatically adds a start bit (0), an odd or even parity bit specified by the mode instruction during initialization, and a specified number of stop bits (1). After that, the assembled data characters are transferred as serial data via the T_XD pin, if transfer is enabled ($T_XEN=1 \cdot \overline{CTS}=$"L"). In this case, the transfer data (baud rate) is shifted by the mode instruction at a rate of 1X, 1/16X, or 1/64X the $\overline{T_XC}$ period.

If the data characters are not loaded on the M5L8251AP-5, the T_XD pin enters a mark state ("H"). When SBRK is programmed by the command instruction, break characters (0) are output continuously through the T_XD pin.

Asynchronous Reception Mode

The R_XD line usually starts operations in a mark state ("H"), triggered by the falling edge of a low-level pulse when it comes to this line. This signal is again strobe at the middle of the bit to confirm that it is a perfect start bit. The detection of a second low-level indicates the validity of the start bit (again strobe is carried out only in the case of 16X and 64X). After that, the bit counter inside the M5L8251AP-5 starts operating; each bit of the serial information on the R_XD line is shifted in by the rising edge of $\overline{R_XC}$, and the data bit, parity bit (when necessary), and stop bit are sampled at the middle position.

The occurrence of a parity error causes the setting of a parity-error flag. If the stop bit is 0, a frame error flag is set. Attention should be paid to the fact that the receiver requires only one stop bit even though the program has designated 1/1.5 or 2 stop bits.

Reception up to the stop bit means reception of a complete character. This character is then transferred to the receiver-data buffer shown in Fig.2, and the R_XRDY becomes active. In cases where this character is not read by the CPU and where the next character is transferred to the receiver-data buffer, the preceding character is destroyed and an overrun-error flag is set.

These error flags can be read as the M5L8251AP-5 status information. The occurrence of an error does not stop USART operations. The error flags are cleared by the ER(D_4 bit) of the command instruction.

The asynchronous-system transfer formats are shown in Figs. 6 and 7.

Synchronous Transmission Mode

In this mode the T_XD pin remains in the high-level state until initial setting by the CPU is completed. After initialization, the state of $\overline{CTS}$="L" and $T_XEN=1$ enables serial transmission of characters through the T_XD pin. Then, data characters are sent out and shifted by the falling edge of the $\overline{T_XC}$ signal. The transmission rate equals the $\overline{T_XC}$ rate.

Thus, once data-character transfer starts, it must continue through the T_XD pin at the same rate as that of $\overline{T_XC}$. Unless data characters are provided from the CPU before the transmitter buffer becomes empty, one or two SYNC characters are automatically output from the T_XD pin. In this case, it should be noted that the T_XEMPTY pin enters the high-level state when there are no data characters left in the M5L8251AP-5 to be transferred, and that the low-level state is not entered until the USART is provided with the next data character from the CPU. Care should also be taken over the fact that merely setting a command instruction does not effect SYNC-character insertion, because the SYNC character insertion is enabled after sending out the first data character.

In this mode, too, break characters are sent out in succession from the T_XD pin when SBRK is designated ($D_3=1$) by a command instruction.

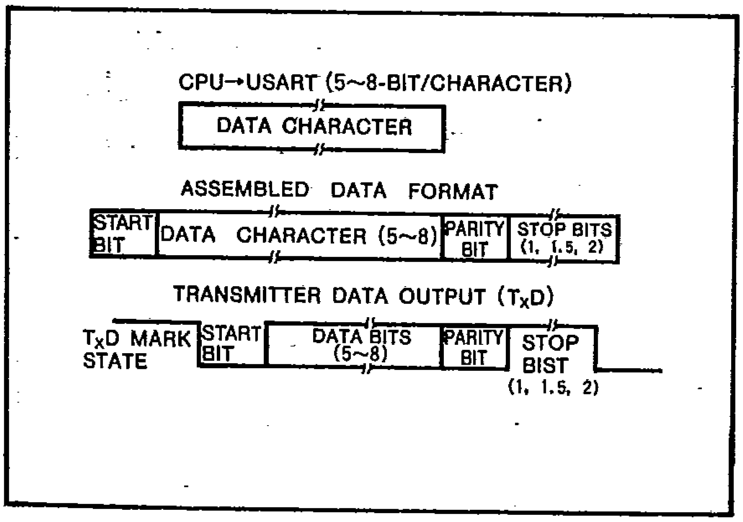
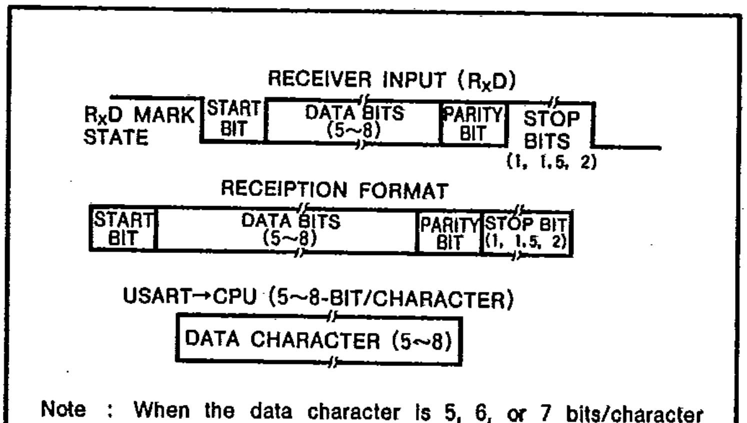


Fig. 6 Asynchronous transmission format I (transmission)



Note : When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART→CPU) are set to 0.

Fig. 7 Asynchronous transmission format II (reception)

Synchronous Reception Mode

Character synchronization in this mode is carried out internally or externally by initial-setting designation.

Programming in the internal synchronous mode requires that an EH instruction ($D_7=1$, enter hunt mode) is included in the first command instruction. Data on the R_XD pin is sampled by the rising $\overline{R_XC}$ signal, and the receiver-buffer contents are compared with the SYNC character each time a bit is input. Comparison continues until an agreement is reached. When the M5L8251AP-5 has been programmed in the bi-sync mode, data received in further succession is compared. The detection of two SYNC characters in succession makes the USART end the hunt mode, setting the SYNDET pin to the high-level state. This reset operation is prompted by the reading of the status information. When the parity has been programmed, SYNDET is not set in the middle of the last data bit but in the middle of the parity bit.

In the external synchronous mode, the M5L8251AP-5 gets out of the hunt mode when a high-level synchronization signal is given to the SYNDET pin. The high-level signal requires a minimum duration of one $\overline{R_XC}$ cycle. In the asynchronous mode, however, the EH signal does not affect the operation at all.

Parity and overrun errors are checked in the same way as in the asynchronous system. During hunt-mode operations the parity bit is not checked, but parity checking is carried out even when the receiver is disabled.

The CPU can command the receiver to enter the hunt mode, if synchronization is lost. This prevents the SYNC character from erroneously becoming equal to the received data when all the data in the receiver buffer is set to 1 Attention should be paid to the fact that the SYNDET F/F is reset each time status information is read irrespective of the synchronous mode's being internal or external. This, however, does not return the M5L8251AP-5 to the hunt mode. Synchronism detection is carried out even though it is not the hunt mode. The synchronous transfer formats are shown in Figs. 8 and 9.

Command Instruction

This instruction defines actual operations in the communication mode designated by mode setting. Command instructions include transmitter/receiver enable error-reset, internal-reset, modem-control, enter-hunt and break transmission instructions.

The mode is set following the reset operation. A SYNC character is set as required, and the writing of high-level signals on the control/data pin ($C/\overline{D}$) that follows it is regarded as a command instruction. When the mode is set all over again from the beginning, the M5L8251AP-5 can be reset by using inputting via the reset terminal or by internal resetting based on the command instruction.

Note 1: The command error reset (ER), internal reset (IR) and enter-hunt-mode (EH) operations are only effective when the command instruction is loaded, so that these bits need not be returned to 0.

2: When a break character is sent out by a command, the T_XD set to 0 immediately irrespective of whether or not the USART has sent out data.

3: Operations of the USART's receiver section which is always in the enable state cannot be inhibited. The command instruction $R_XE=0$ does not mean that data reception via the R_XD pin is inhibited; it means that the R_XRDY is masked and error flags are inhibited.

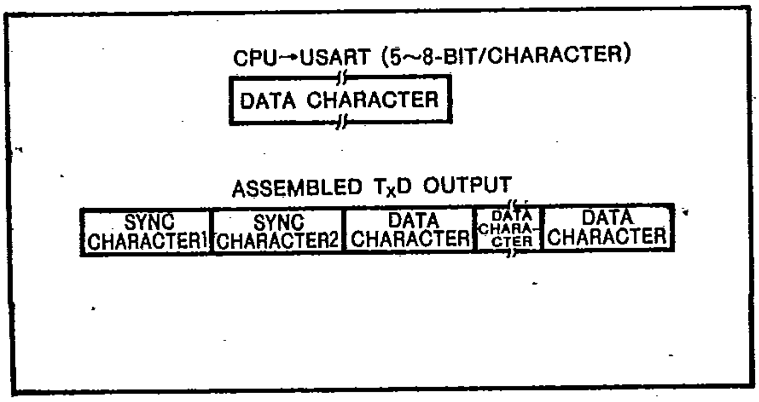


Fig. 8 Synchronous transmission format I (transmission)

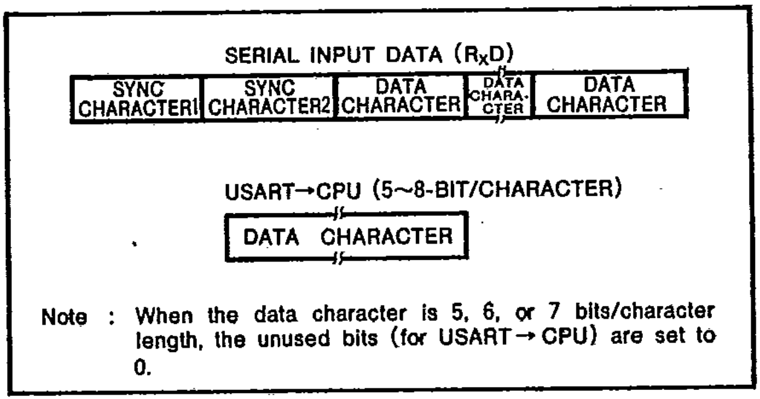

SERIAL INPUT DATA (RxD)
SYNC CHARACTER1
SYNC CHARACTER2
DATA CHARACTER
DATA CHARACTER
DATA CHARACTER
USART→CPU (5~8-BIT/CHARACTER)
DATA CHARACTER
Note : When the data character is 5, 6, or 7 bits/character length, the unused bits (for USART→CPU) are set to 0.

Fig. 9 Synchronous transmission format II (reception)

STATUS INFORMATION

The CPU can always read USART status by setting the $C/\overline{D}$ to high-level and $\overline{RD}$ to low-level.

The status information format is shown in Fig. 10. In this format R_XRDY, T_XEMPTY and SYNDET have the same definitions as those of the pins. This means that these three pieces of status information become high-level when each pin is 1. The other status information is defined as follows:

DSR: When the $\overline{DSR}$ pin is in the low-level state, status information DSR becomes 1.

FE: The occurrence of a frame error in the receiver section makes the status information FE=1.

OE: The occurrence of an overrun error in the receiver section makes the status information OE=1.

PE: The occurrence of a parity error in the receiver section makes this status information PE=1.

T_XRDY: This information becomes 1 when the transmit data buffer is empty. Be careful because this has a different meaning from the T_XRDY pin that enters the high-level state only when the transmitter buffer is empty, when the $\overline{CTS}$ pin is in the low-level state, and when T_XEN is 1.

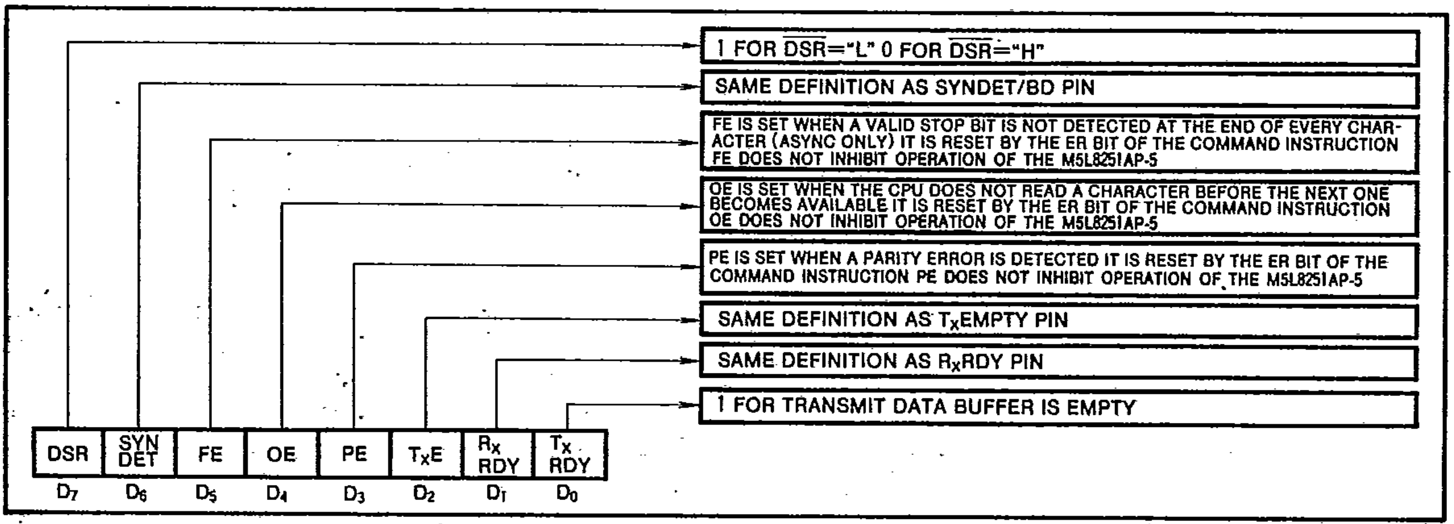

1 FOR $\overline{DSR}$="L" 0 FOR $\overline{DSR}$="H"
SAME DEFINITION AS SYNDET/BD PIN
FE IS SET WHEN A VALID STOP BIT IS NOT DETECTED AT THE END OF EVERY CHARACTER (ASYNC ONLY) IT IS RESET BY THE ER BIT OF THE COMMAND INSTRUCTION FE DOES NOT INHIBIT OPERATION OF THE M5L8251AP-5
OE IS SET WHEN THE CPU DOES NOT READ A CHARACTER BEFORE THE NEXT ONE BECOMES AVAILABLE IT IS RESET BY THE ER BIT OF THE COMMAND INSTRUCTION OE DOES NOT INHIBIT OPERATION OF THE M5L8251AP-5
PE IS SET WHEN A PARITY ERROR IS DETECTED IT IS RESET BY THE ER BIT OF THE COMMAND INSTRUCTION PE DOES NOT INHIBIT OPERATION OF THE M5L8251AP-5
SAME DEFINITION AS T_XEMPTY PIN
SAME DEFINITION AS R_XRDY PIN
1 FOR TRANSMIT DATA BUFFER IS EMPTY
DSR
SYN DET
FE
OE
PE
T_XE
R_X RDY
T_X RDY
D_7
D_6
D_5
D_4
D_3
D_2
D_1
D_0

Fig. 10 Status information ($C/\overline{D}$="H", $\overline{WR}$="L")

APPLICATION EXAMPLES

Fig. 11 shows an application example for the M5L8251AP-5 in the asynchronous mode. When the port addresses of the M5L8251AP-5 are assumed to be 00# and 01# in this figure, initial setting in the asynchronous mode is carried out in the following manner:

```
MVI   A, B6#   Mode setting
OUT   01#
MVI   A, 27#   Command instruction
OUT   01#
```

In this case, the following are set by mode setting:

Asynchronous mode
6 bits/character
Parity enable (even)
1.5 stop bits
Baud rate: 16X

Command instructions set the following

RTS=1→$\overline{RTS}$ pin="L"
R_XE=1
DTR=1→$\overline{DTR}$ pin="L"
T_XEN=1

When the initial setting is complete, transfer operations are allowed. The $\overline{RTS}$ pin is initially set to the low-level by setting RTS to 1, and this serves as a $\overline{CTS}$ input with T_XEN being equal to 1. For this reason the same definition applies to the status and pin of T_XRDY, and 1 is assigned when the transmit-data buffer is empty. Actual transfer of data is carried out in the following way:

```
IN    01#      Status read
```

The IN instruction prompts the CPU to read the USART's status. The result is; if the T_XRDY equals 1 transmitter data is sent from the CPU and written on the M5L8251AP-5. Transmitter data is written in the M5L8251AP-5 in the following manner:

```
MVI   A, 2D#   2D16 is an example of transmit-
               ter data.
OUT   00#      USART←(A)
```

Receiver data is read in the following manner:

```
IN    00#      (A)←USART
```

In the above example, the status information is read and as a result, the transmitter data is written and read. Interruption processing by using the T_XRDY and R_XRDY pins is also possible.

Fig. 12 shows the status of the T_XD pin when data written in the USART is transferred from the CPU. When the data shown in Fig.12 enters the R_XD pin, data sent from the M5L8251AP-5 to the CPU becomes $2D_{16}$ and bits D_6 and D_7 are treated as 0.

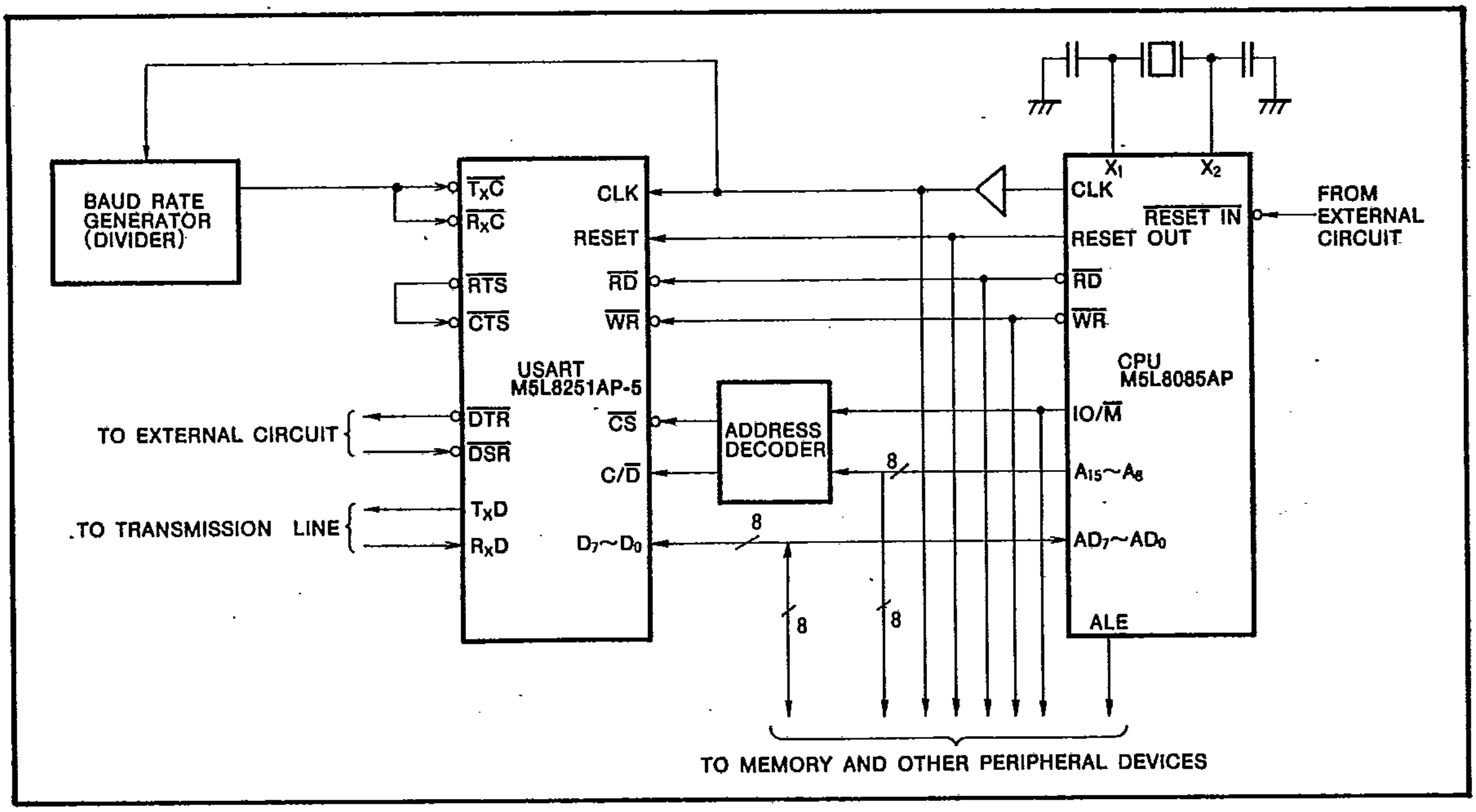


Fig. 11 Example of circuit using the asynchronous mode

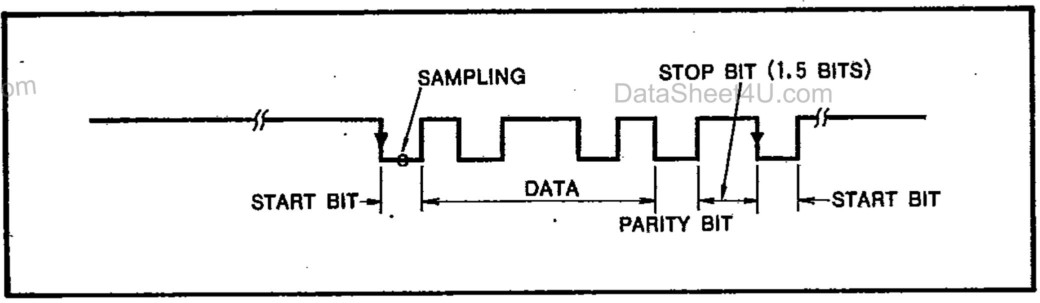


Fig. 12 Example of data transmission

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power-supply voltage	With respect to V_{SS}	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20～75	℃
T_{stg}	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2.2mA			0.45	V
I_{CC}	Supply current from V_{CC}	All outputs are high-level			100	mA
I_{IH}	High-level input current	V_I=V_{CC}	−10		10	μA
I_{IL}	Low-level input current	V_I=0.45V	−10		10	μA
I_{OZ}	Off-state input current	V_O=0.45V～V_{CC}	−10		10	μA
C_I	Input terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			10	pF
$C_{I/O}$	Input/output terminal capacitance	V_{CC}=V_{SS}, f=1MHz, 25mV_{rms}, T_a=25℃			20	pF

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Clock cycle time (Notes4, 5)			320		1350	ns
$t_{W(\phi)}$	Clock high pulse width			120		$t_{C(\phi)}-90$	ns
$t_{W(\overline{\phi})}$	Clock low pulse width			90			ns
t_r	Clock rise time					20	ns
t_f	Clock fall time					20	ns
f_{TX}	Transmitter input clock frequency	1X baud rate		DC		64	kHz
		16X baud rate		DC		310	
		64X baud rate		DC		615	
$t_{W(TPWL)}$	Transmitter input clock low pulse width	1X baud rate		12			$t_{C(\phi)}$
		16X, 64X baud rate		1			
$t_{W(TPWH)}$	Transmitter input clock high pulse width	1X baud rate		15			$t_{C(\phi)}$
		16X, 64X baud rate		3			
f_{RX}	Receiver input clock frequency	1X baud rate		DC		64	kHz
		16X baud rate		DC		310	
		64X baud rate		DC		615	
$t_{W(RPWL)}$	Receiver input clock low pulse width	1X baud rate		12			$t_{C(\phi)}$
		16X, 64X baud rate		1			
$t_{W(RPWH)}$	Receiver input clock high pulse width	1X baud rate		15			$t_{C(\phi)}$
		16X, 64X baud rate		3			
$t_{SU(A-R)}$	Address setup time before read ($\overline{CS}$, C/$\overline{D}$) (Note6)			0			ns
$t_{h(R-A)}$	Address hold time after read ($\overline{CS}$, C/$\overline{D}$) (Note6)			0			ns
$t_{W(R)}$	Read pulse width			250			ns
$t_{SU(A-W)}$	Address setup time before write			0			ns
$t_{h(W-A)}$	Address hold time after write			0			ns
$t_{W(W)}$	Write pulse width			250			ns
$t_{SU(DQ-W)}$	Data setup time before write			150			ns
$t_{h(W-DQ)}$	Data hold time after write			20			ns
$t_{SU(ESD-RxC)}$	E•SYNDET setup time before $\overline{R_XC}$			18			$t_{C(\phi)}$
$t_{SU(C-R)}$	Control setup time before read			20			$t_{C(\phi)}$
t_{RV}	Write recovery time between writes (Note7)			6			$t_{C(\phi)}$
$t_{SU(RxD-IS)}$	R_XD setup time before internal sampling pulse			2			μs
$t_{h(IS-RxD)}$	R_XD hold time after internal sampling pulse			2			μs

Note 4 : The $\overline{T_XC}$ and $\overline{R_XC}$ frequencies have the following limitations with respect to CLK.
For 1X baud rate f_{TX}, $f_{RX} \leqq 1/(30t_{C(\phi)})$. For 16X 64X baud rate f_{TX}, $f_{RX} \leqq 1/(4.5t_{C(\phi)})$

5 : Reset pulse width=$6t_{C(\phi)}$ minimum. System clock must be running during reset.

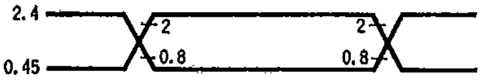
6 : $\overline{CS}$, C/$\overline{D}$ are considered as address.

7 : This recovery time is for mode initialization only. Write data is allowed only when T_XRDY=1. Recovery time between writes for asynchronous mode is $8t_{C(\phi)}$, and that for synchronous mode is $16t_{C(\phi)}$.

SWITCHING CHARACTERISTICS (T_a=−20~75°C, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

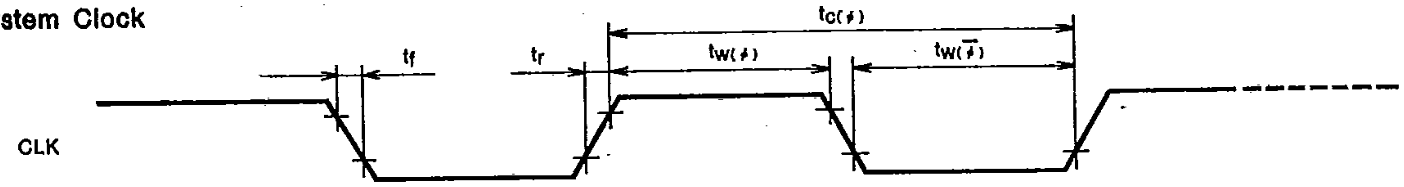
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PZV(R-DQ)}$	Output data enable time after read (Note8)	C_L=150pF			200	ns
$t_{PVZ(R-DQ)}$	Output data disable time after read		10		100	ns
$t_{PZV(T_xC-T_xD)}$	T_XD enable time after falling edge of $\overline{T_XC}$				1	μs
$t_{PLH(CLB-T_xR)}$	Propagation time from center of last bit to T_XRDY (Note9)				8	$t_{C(\phi)}$
$t_{PHL(W-T_xR)}$	Propagation time from write data to T_XRDY clear (Note9)				400	ns
$t_{PLH(CLB-R_xR)}$	Propagation time from center of last bit to R_XRDY (Note9)				26	$t_{C(\phi)}$
$t_{PHL(R-R_xR)}$	Propagation time from read data to R_XRDY clear (Note9)				400	ns
$t_{PLH(R_xC-SYD)}$	Propagation time from rising edge of $\overline{R_XC}$ to internal SYNDET (Note9)				26	$t_{C(\phi)}$
$t_{PLH(CLB-T_xE)}$	Propagation time from center of last bit to T_XEMPTY (Note9)				20	$t_{C(\phi)}$
$t_{PHL(W-C)}$	Propagation time from rising edge of $\overline{WR}$ to control (Note9)				8	$t_{C(\phi)}$

Note 8 : Assumes that address is vaild before falling edge of $\overline{RD}$
9 : Status-up date can have a maximum delay of 28 clock periods from the event affecting the status.
10 : Input pulse level 0.45~2.4V Reference level Input V_{IH}=2V, V_{IL}=0.8V
Input pulse rise time 20ns Output V_{OH}=2V, V_{OL}=0.8V
Input pulse fall time 20ns

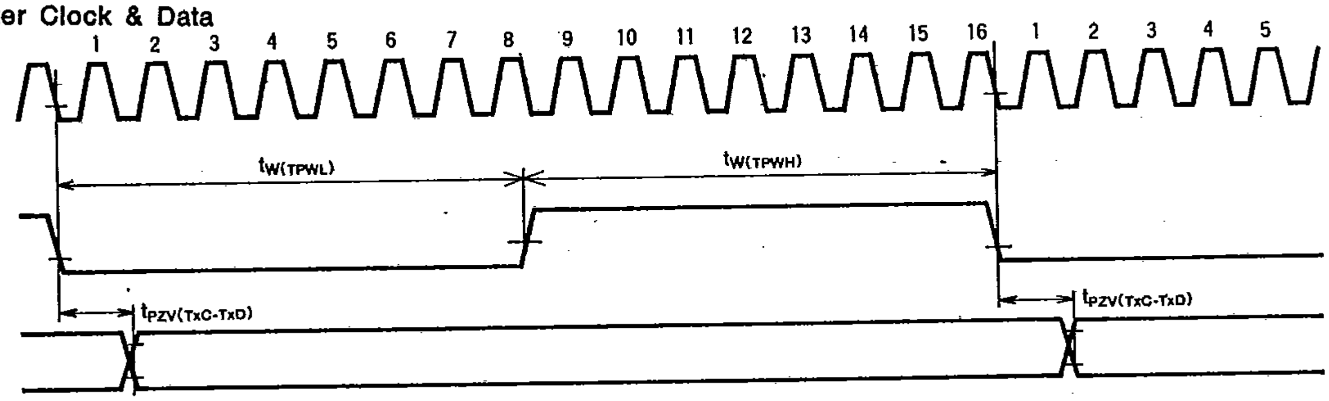


TIMING DIAGRAMS

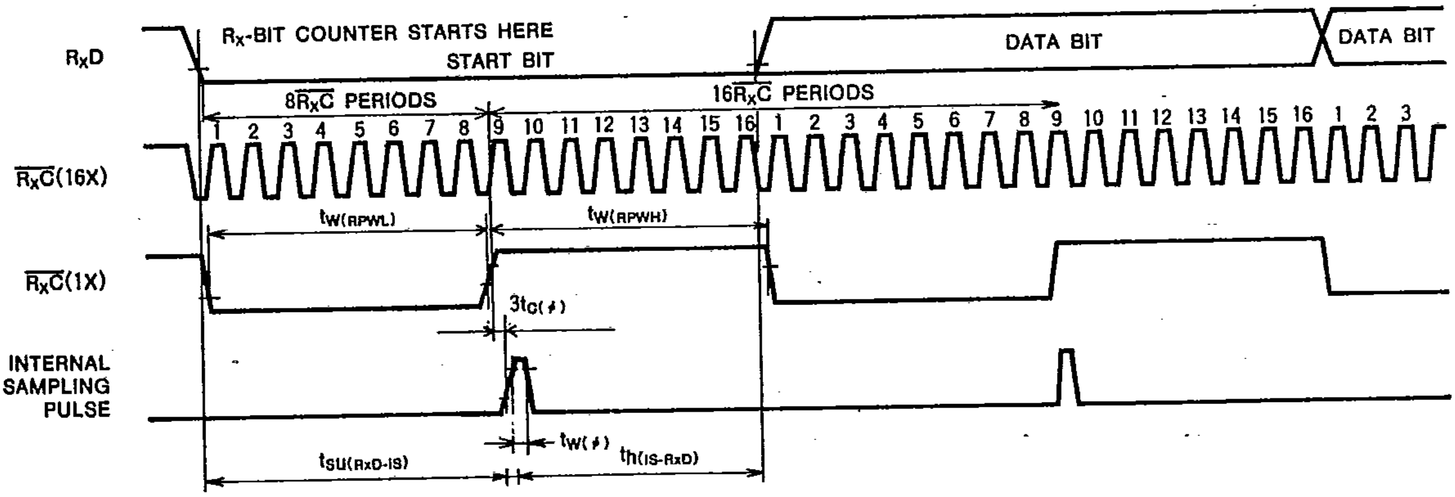
System Clock



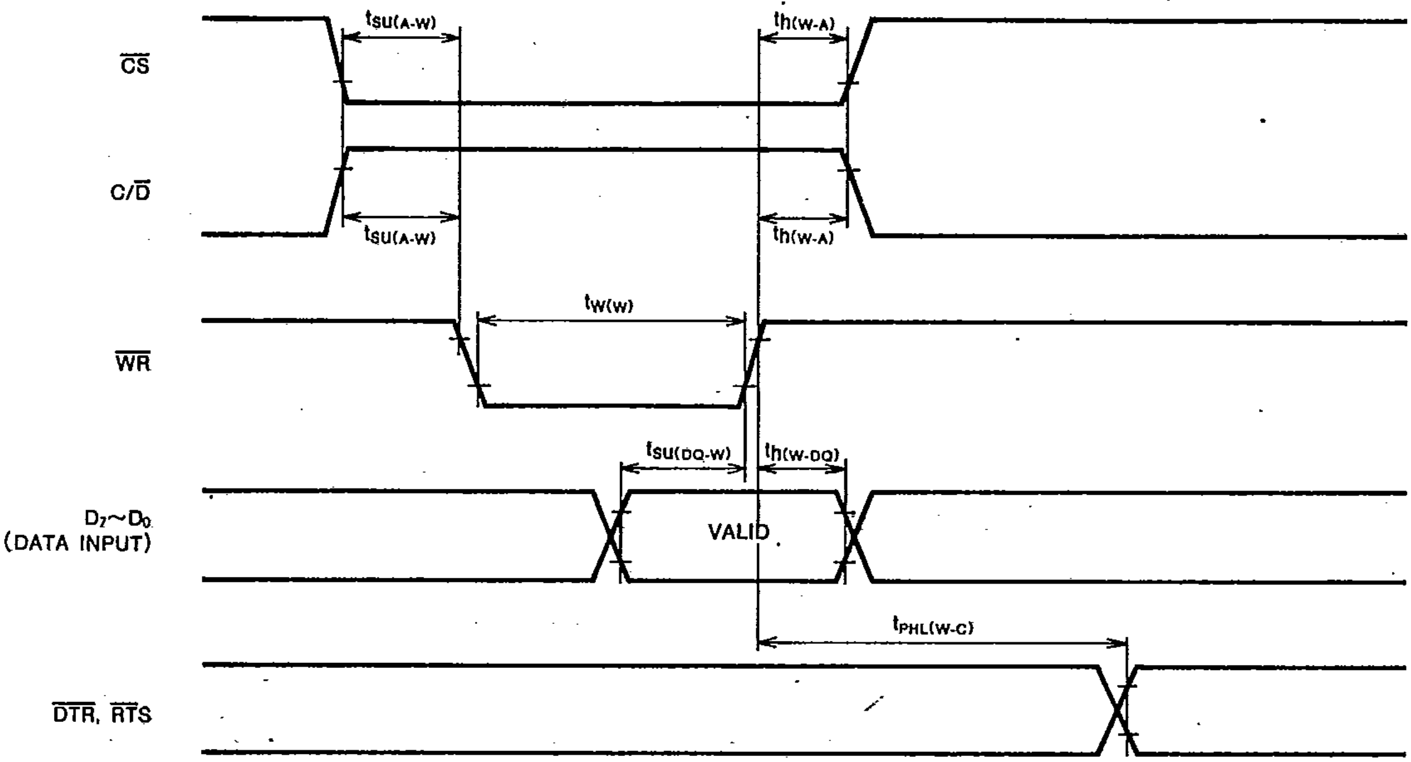
Transmitter Clock & Data



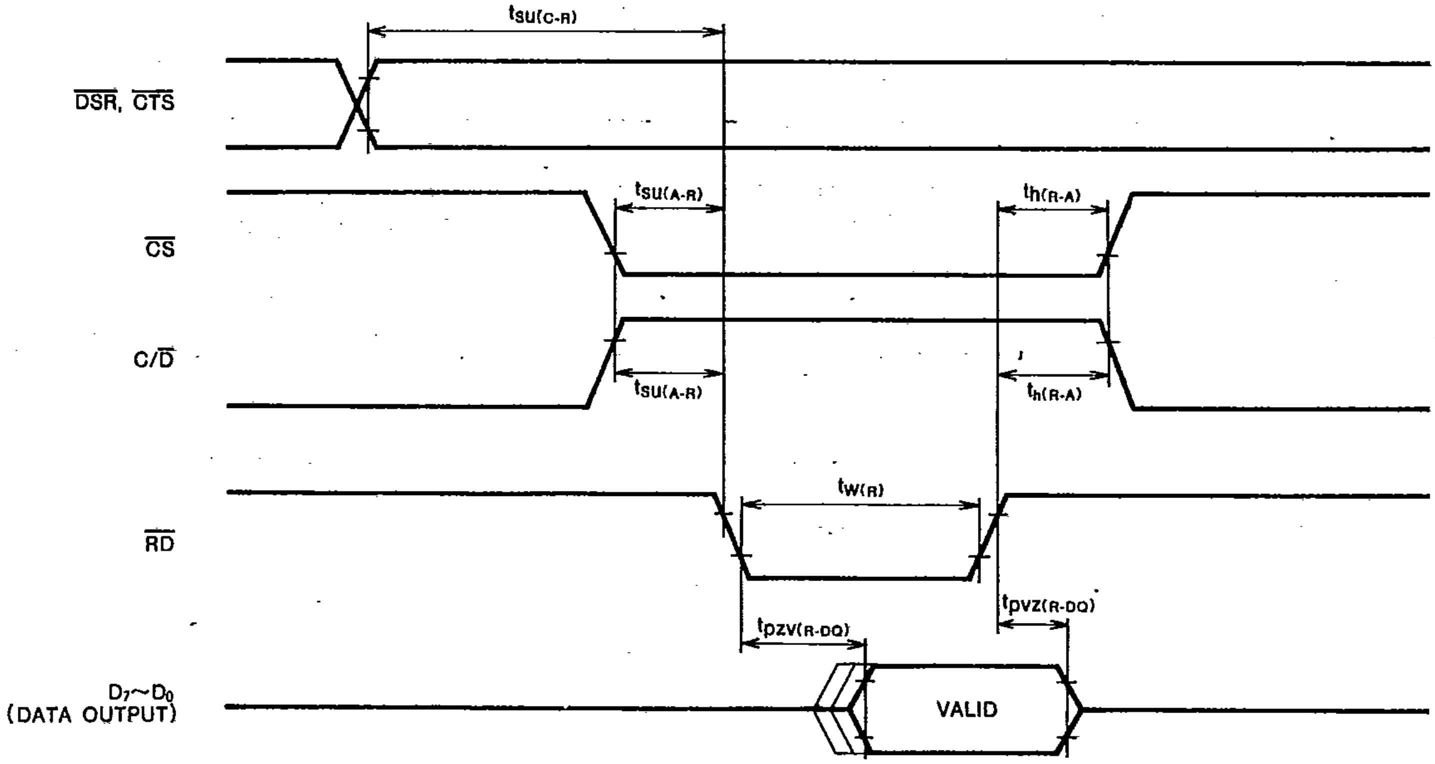
Receiver Clock & Data



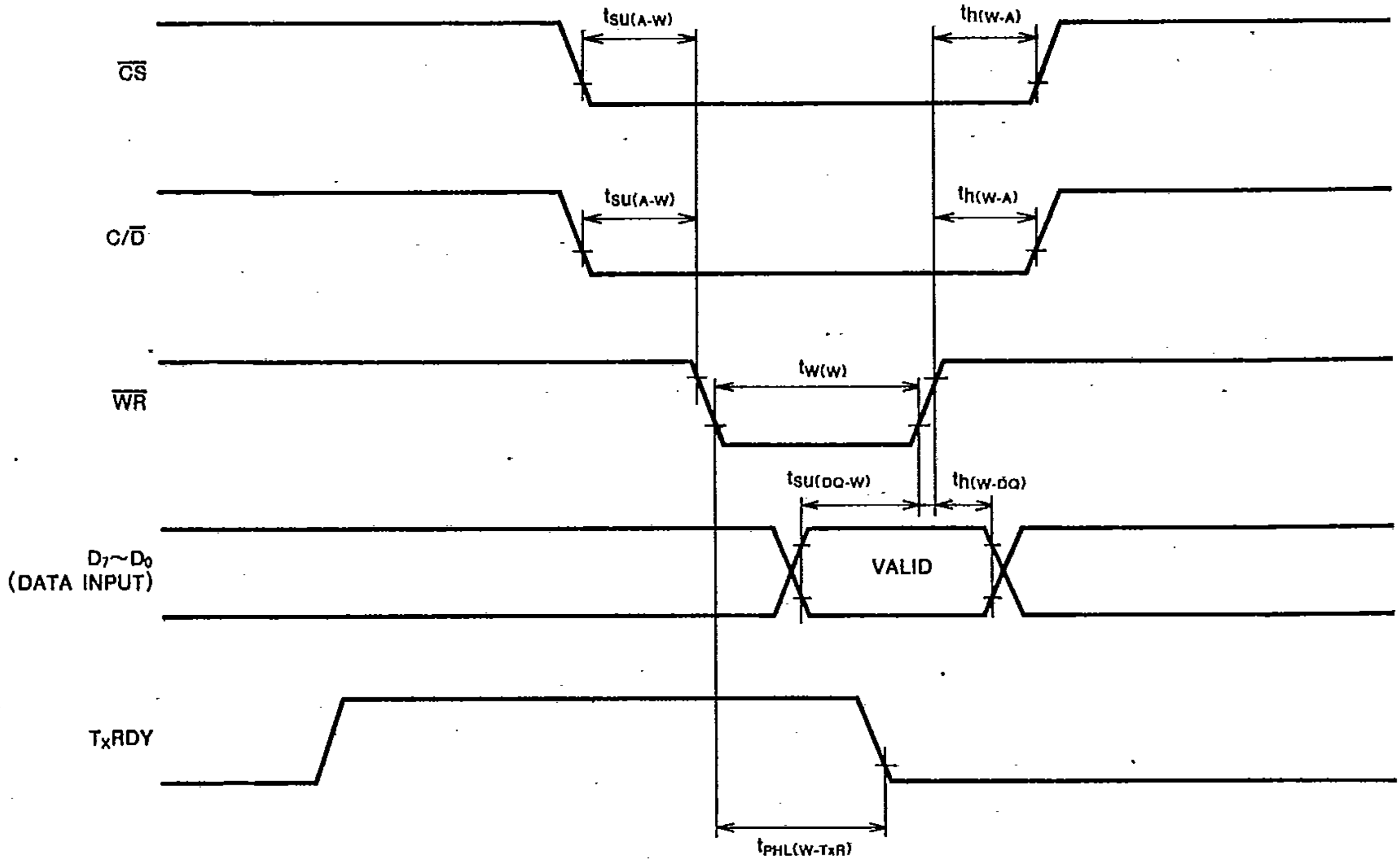
Write Control Cycle (CPU→USART)



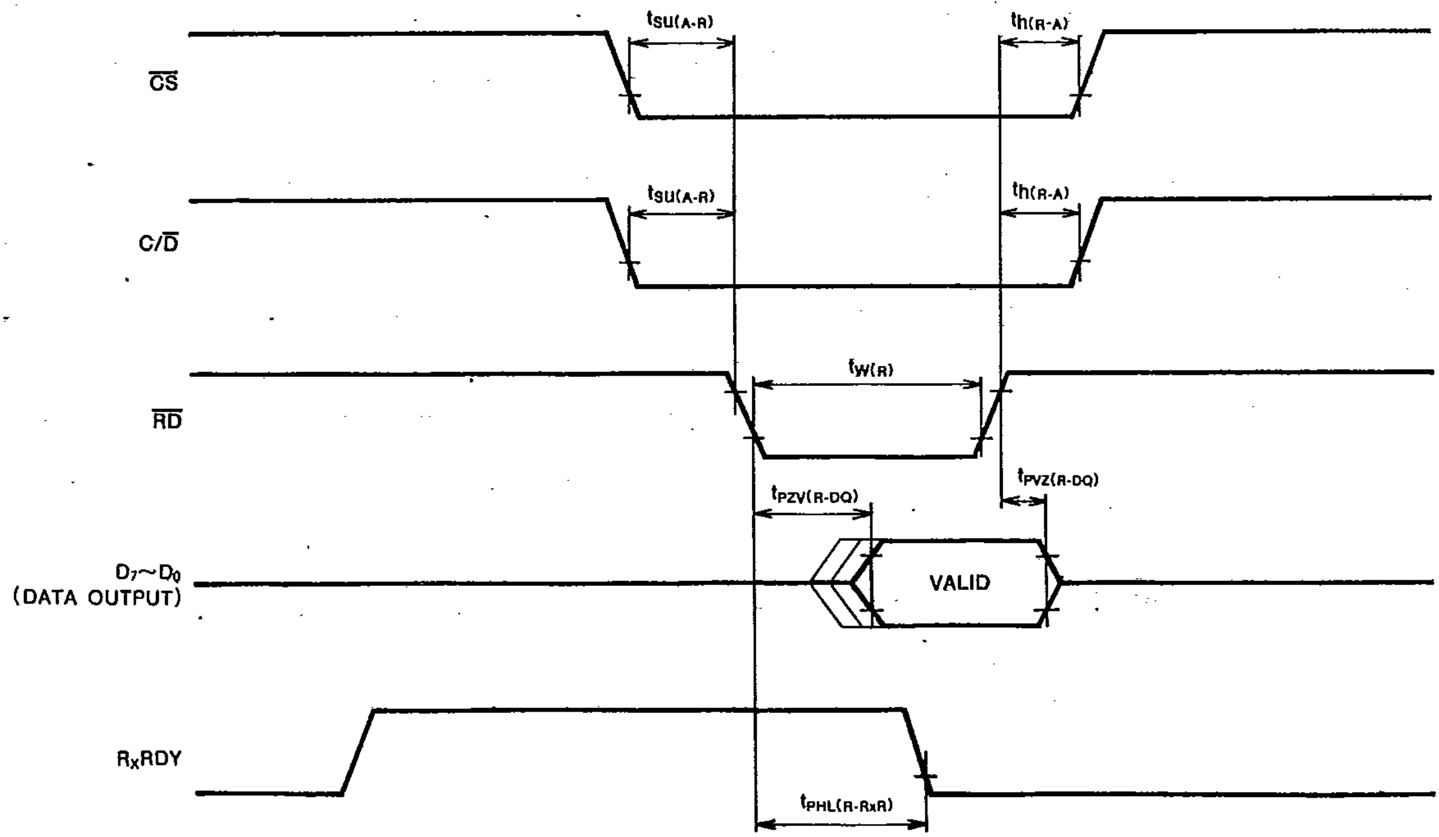
Read Control Cycle (USART→CPU)



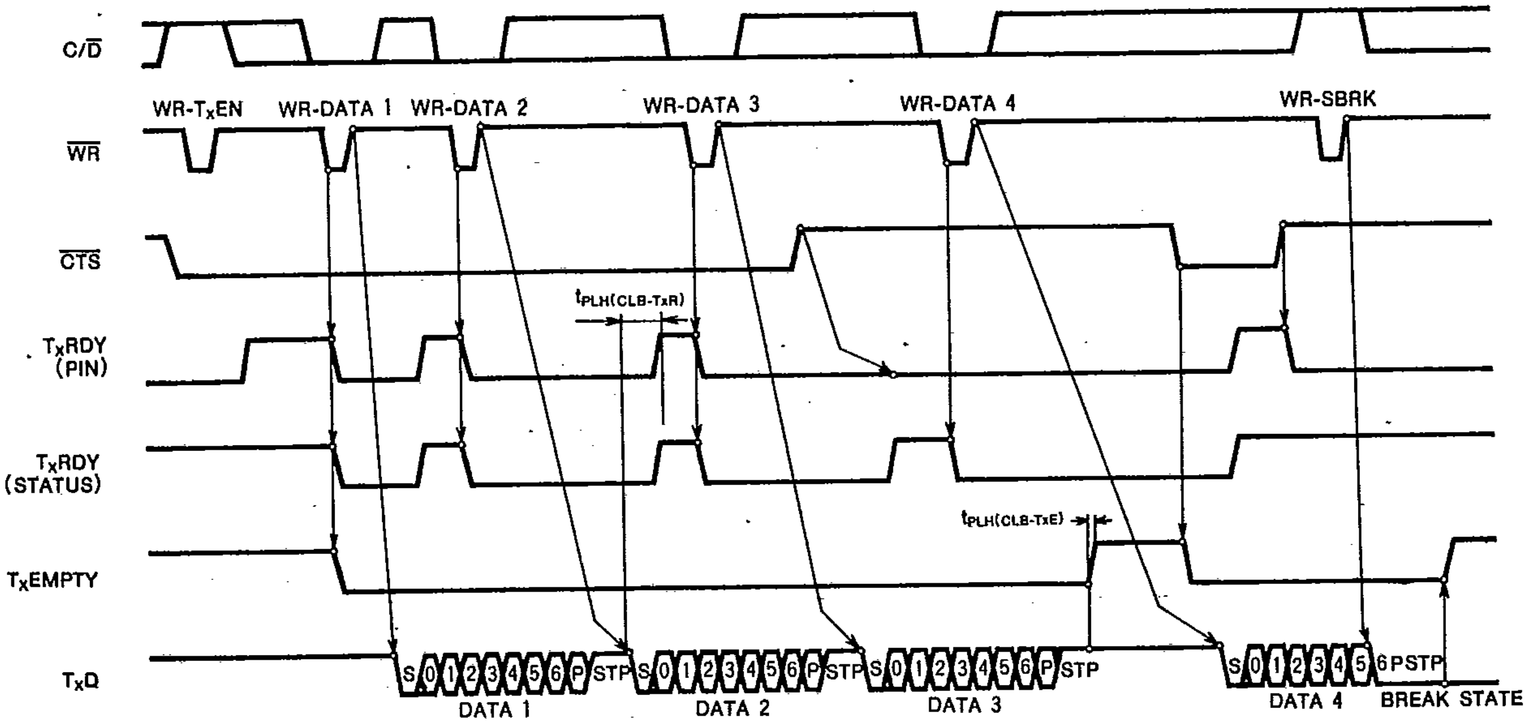
Write Data Cycle (CPU→USART)



Read Date Cycle (USART→CPU)

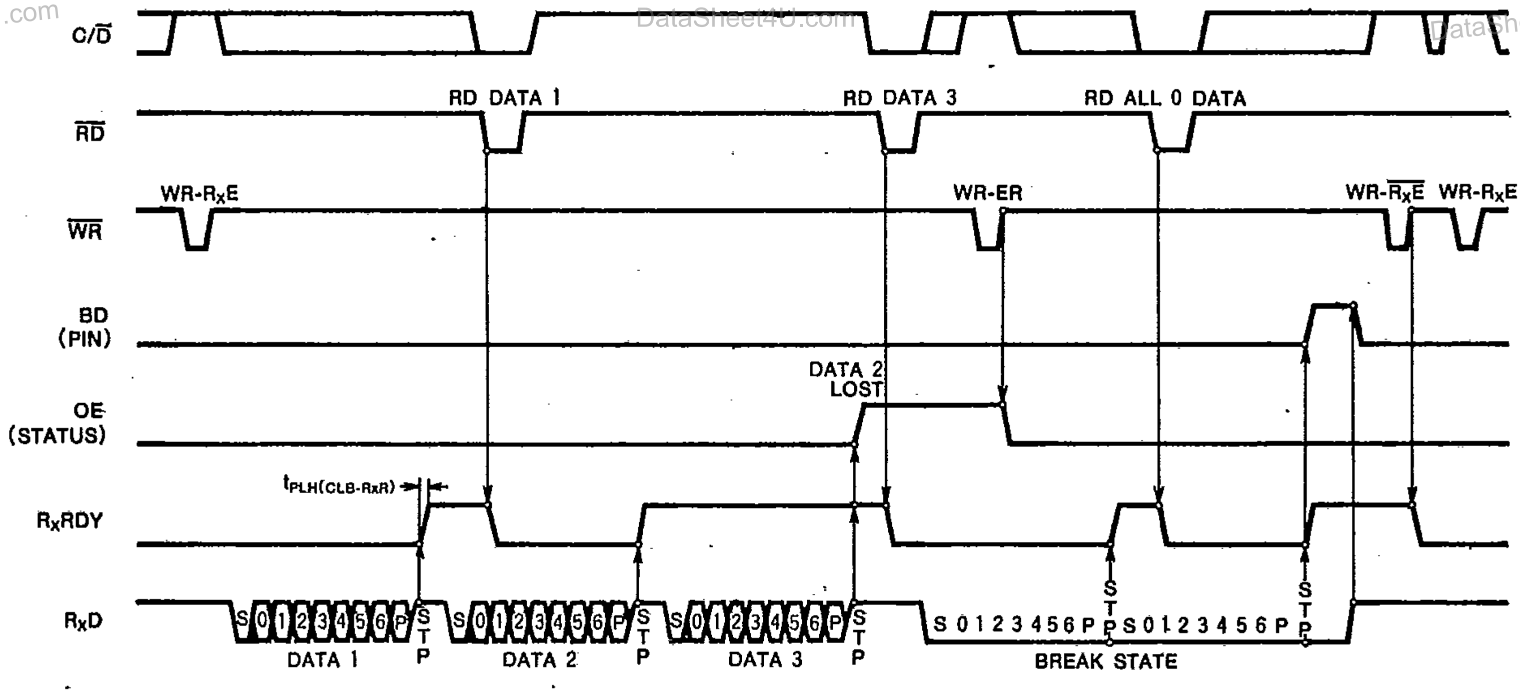


Transmitter Control & Flag Timing (Async Mode)



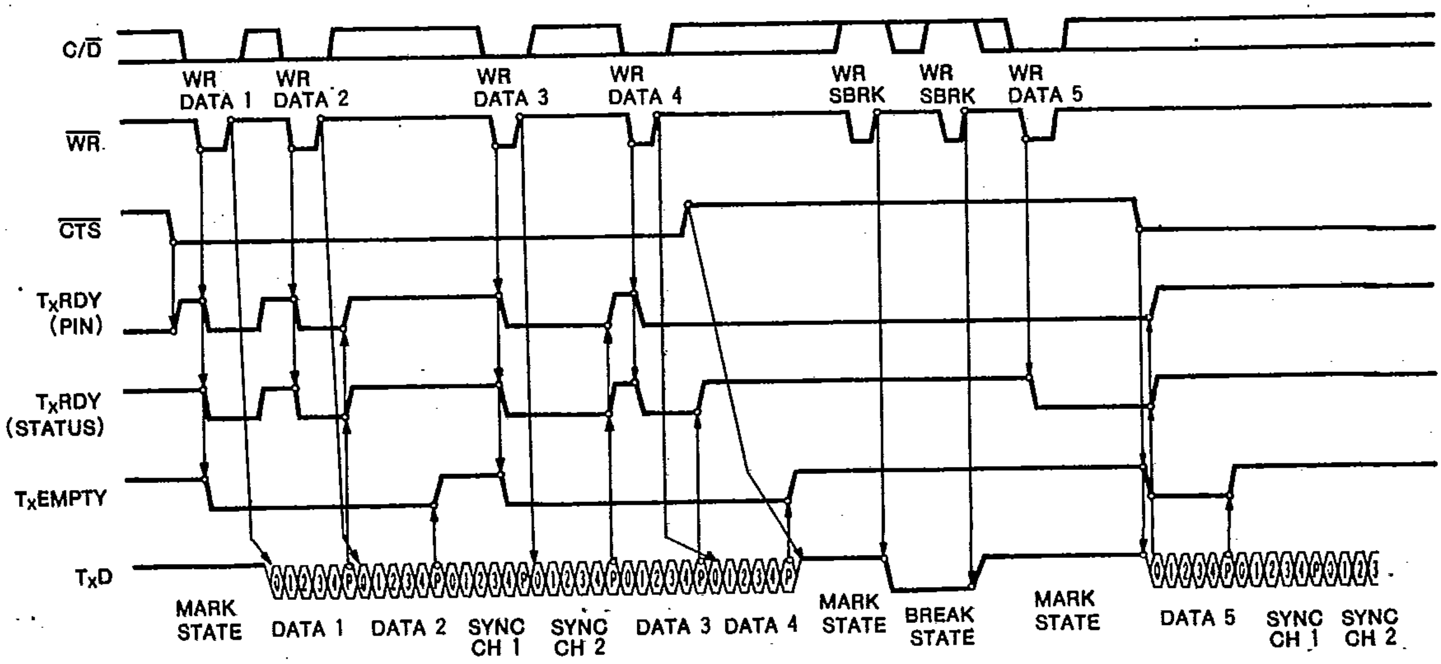
Note 11 : Example format = 7 bits/character with parity & 2 stop bits
12 : T_XRDY(pin) = "H" ←(Transmit-data buffer is empty) · (T_XEN = 1) · (CTS = "L")
13 : T_XRDY(status) = 1 ←(Transmit-data buffer is empty)

Receiver Control & Flag Timing (Async Mode)



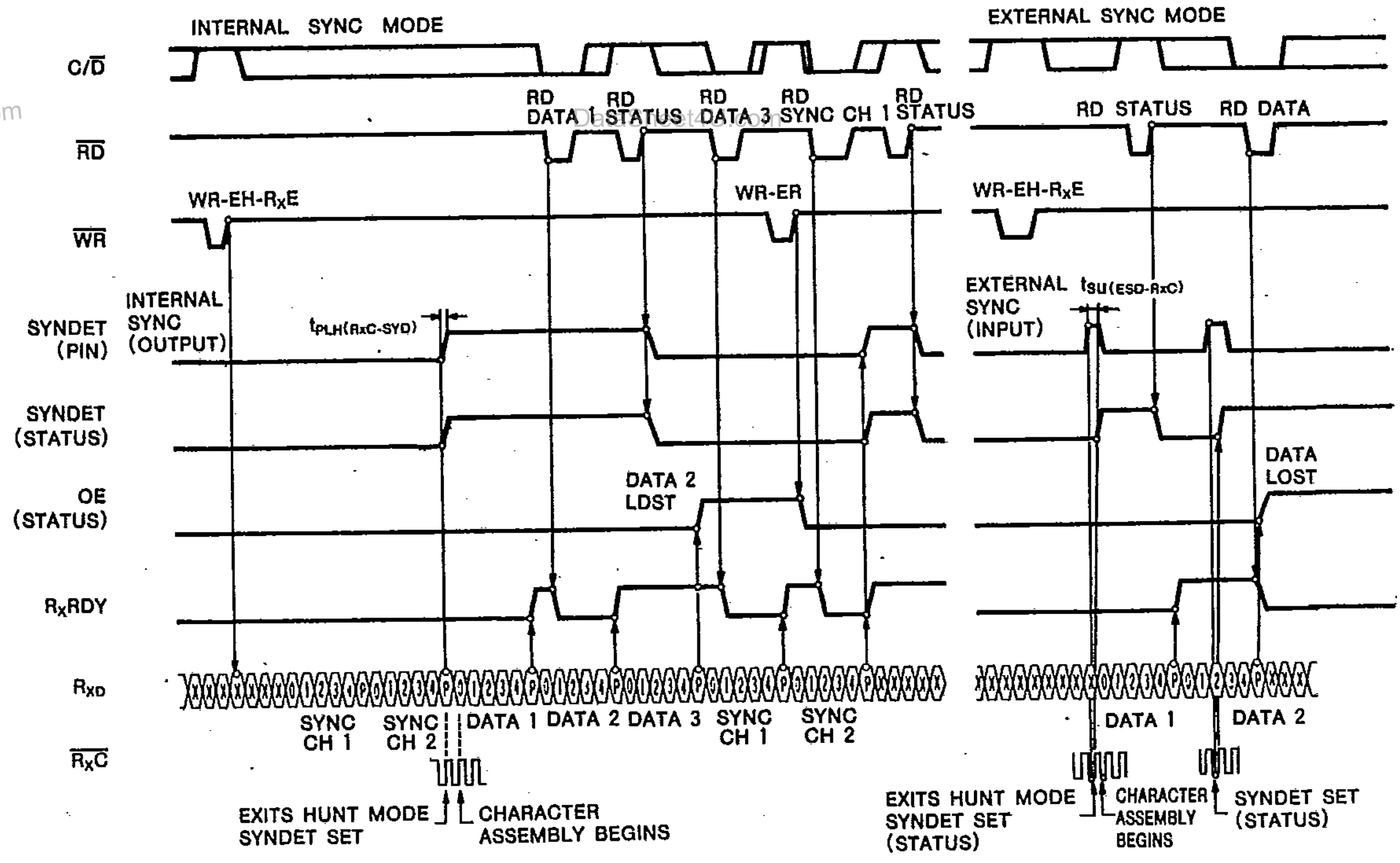
Note 14 : Example format = 7 bits/character with parity & 2 stop bits

Transmitter Control & Flag Timing (Sync Mode).



Note 15 : Example format = 5 bits/character with parity, bi-sync characters.

Receiver Control & Flag Timing (Sync Mode)



Note 16 : Example format = 5 bits/character with parity, bi-sync characters.