# GEC PLESSEY

SEMICONDUCTORS

S21600FDS Issue 1.2 November 1990

# MA9000A Sea of Gates

## Radiation Hard Advanced Gate Array Design System

## Features

- **Channelless array architecture**
- **Typical gate delay 1.0nS - toggle rates of 100MHz achievable**
- **1.25uW/MHz power dissipation per active gate**
- **Extensive CAD design and support system**
- **Comprehensive library of logic cells and logic function building macros, with RAM & ROM**
- **Double-Level-Metal CMOS/SOS Technology**
- **High SEU immunity, latch-up free**
- **Radiation hard to 1MRad(Si)**

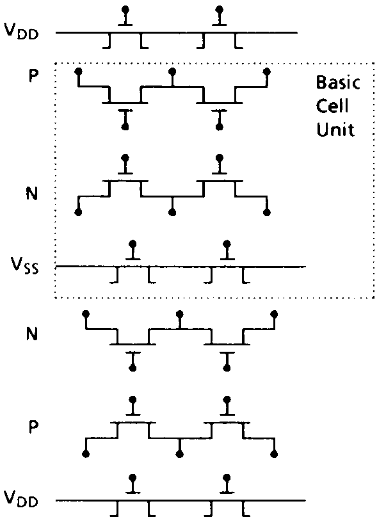


*Figure 1: Basic Cell Unit*

## General Description

The logic building block is a six transistor 'cell-unit', equivalent in size to a two input NAND gate. The cell contains four transistors for building logic circuits and two transistors which are used in RAM macros. These extra two transistors are placed under the logic power routing and so have no detrimental effect upon overall area. Back-to-back cell units form the core of the array.

The interconnection patterns that cause groups of cell-units to become defined logic cells, and the models which are used to simulate these cells, are stored as software in libraries. Cells up to the complexity of multiple bit shift registers are treated in this way.

## Array Options

| Array type | Cell units | Bonding pads | | |
|---|---|---|---|---|
| | | I/O | Power | Total |
| MA9140 | 14112 | 102 | 8 | 110 |
| MA9200 | 20296 | 120 | 8 | 128 |

Any I/O site may be configured as a power pad to give flexible bonding option, but to standardise testing preferred positions exist. Each cell-unit is the equivalent to either one 2 input NAND gate or one RAM storage bit.

8

# Radiation Hard Advanced Gate Array Design System

## DC Charcteristics and Ratings

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.5 | 7 | V |
| $V_I$ | Input voltage | -0.3 | $V_{DD}$ + 0.3 | V |
| $T_A$ | Operating temperature | -55 | 125 | °C |
| $T_S$ | Storage temperature | -65 | 150 | °C |

*Figure 2: Absolute Maximum Ratings*

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | - | 4.5 | 5.0 | 5.5 | V |
| $V_{IH1}$ | TTL input high voltage | - | 2.0 | - | - | V |
| $V_{IL1}$ | TTL input low voltage | - | - | - | 0.8 | V |
| $V_{IH2}$ | CMOS input high voltage | - | 70 | - | - | %$V_{DD}$ |
| $V_{IL2}$ | CMOS input low voltage | - | - | - | 30 | %$V_{DD}$ |
| $V_{OH1}$ | TTL output high voltage | $I_{OH}$ = -2.0mA | 2.4 | - | - | V |
| $V_{OL1}$ | TTL output low voltage | $I_{OL}$ = 5.0mA | - | - | 0.4 | V |
| $V_{OH2}$ | CMOS output high voltage | $I_{OH}$ = -4mA | 90 | - | - | %$V_{DD}$ |
| $V_{OL2}$ | CMOS output low voltage | $I_{OL}$ = 4mA | - | - | 10 | %$V_{DD}$ |
| $I_I$ | Input leakage current | - | - | - | 10 | uA |
| $I_{OZ}$ | Output leakage current | Tristate Output | - | - | 10 | uA |
| $I_{DD}$ | Static power supply current | - | - | 0.5 | 5 | mA |

$V_{DD}$ = 5V ± 10%, over full operating temperature range

*Figure 3: Electrical Characteristics*

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SEMICONDUCTORS

# MA9000A Sea of Gates

## Radiation Hard Advanced Gate Array Design System

## AC Characteristics

| Cell Name | Function | O/P Edge | Inherent Delay | Per 1pF Load* | Units |
|---|---|---|---|---|---|
| NOP | Inverting buffer | Rising | 0.3 | 0.2 | ns |
| | | Falling | 0.3 | 0.2 | |
| NAND2 | 2 input NAND | Rising | 0.7 | 5.0 | ns |
| | | Falling | 0.5 | 4.8 | |
| DT | D type | Rising CK - QB | 2.7 | 8.9 | ns |
| | | Falling CK - QB | 3.0 | 4.8 | |
| | | Data set-up time | 3.1 | - | |
| | | Data Hold time | 1.9 | - | |

* 1pF is equivalent to fanout of 8 standard gates.

*Figure 4: Electrical Characteristics*

## Propagation Delay

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 75% of those listed.

Use the following to predict delays at any other working temperature or voltage:

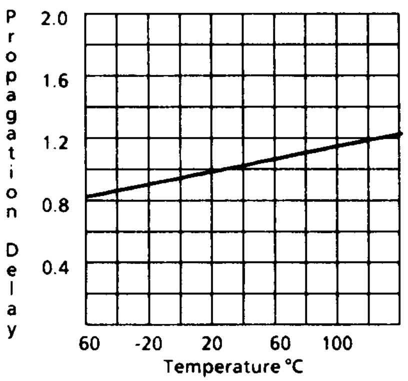


*Figure 5: Propagation Delay Vs Temperature*

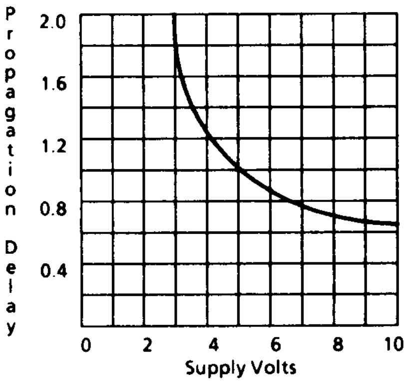


*Figure 6: Propagation Delay Vs Supply Voltage*

8

# Radiation Hard Advanced Gate Array Design System



## Standard Package Options

Marconi offer a wide range of packages as standard. Other package styles are available. If you require a package not covered on this list, contact Marconi.

| | | | | | | |
|---|---|---|---|---|---|---|
| Ceramic DIL | 24 | 28 | 40 | 48 | 64 | - |
| Cerdip | 24 | 28 | 40 | 48 | - | - |
| Leaded Flatpack | 28 | 42 | 48 | 64 | 84 | 132 |
| Pin Grid Array | 68 | 84 | 100 | 120 | 144 | - |
| Ceramic LCC | (40) | 44 | (48) | 68 | 84 | - |
| Cerquad | 44 | 68 | 84 | - | - | - |

*Figure 7: Standard Package Options*

## Development Interfaces

All design activities prior to mask creation, including automatic layout may be carried out by the equipment manufacturer, and may be delegated to a Marconi design centre.

The full design package runs on a Vax/11 series system, MicroVax (including Daisy LOGICIAN MicroVax combination), and Apollo and Mentor workstations. MEDL support for the DAZIX workstation permits schematic entry of data, workfile verification by simulation and the production of the HILO formatted data base required for automatic layout.

Design specific software, including schematic capture and simulation libraries for DAZIX and Mentor workstations, is supplied by Marconi.

Connection to the Marconi design centre via an X25 protocol or similar telephone link or the use of terminals within a Marconi 'design shop' are other possible options which permit a customer to participate in design activities without involvement in major capital outlay.

Training courses that cover all aspects of design and cater for different levels of starting experience are run at the Marconi Wembley Design centre. Some of these courses may be combined with 'design shop' activities.

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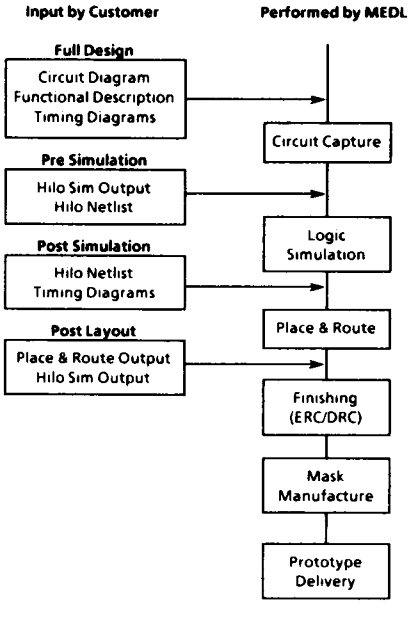


*Figure 8: Development Interfaces*

# MA9000A Sea of Gates

## Radiation Hard Advanced Gate Array Design System

## RadiationTolerance

### Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

| | |
|---|---|
| Total Dose (Function to specification) note 1 | $1x10^6$ Rad(Si) |
| Total Dose (Function to specification) note 2 | $3x10^5$ Rad(Si) |
| Transient Upset (stored data loss) | $10^{11}$ Rad(Si)/sec |
| Transient Upset (survivability) | $>10^{12}$ Rad(Si)/sec |
| Neutron Hardness (Function to specification) | $>10^{15}$ neutrons/cm$^2$ |
| Single Event Upset (GSO 10% worst case) | $<5x10^{-11}$ errors/bitday |
| Latch-up | Not possible |

1 Circuits with all CMOS type inputs
2 Circuits with all TTL type inputs

*Table 9: Radiation Hardness Parameters*

## Macro Design Service

Marconi offer a flexible macro design service to support customer requirements for non-standard cells. Listed are examples of some customer specified Macros that have been designed.

- MA29xx bit slice series elements.
- ALU
- Asynchronous counters
- Parity detectors
- Ripple carry adders
- Selectors
- Gray counters
- Johnson counters
- Lookahead adders

The MA9000A Sea of Gates is a particularly effective route for creating RAM macros.

For more information on Macros and additions to the family contact our nearest office.

# MA9000A Sea of Gates

## Radiation Hard Advanced Gate Array Design System

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### Cell Library Quick Guide

| Cell Name | Function | Cell Units |
|---|---|---|
| **COMBINATIONAL GATES** | | |
| INV | Inverter | 1 |
| INVB | Fast inverter | 1 |
| INVC | Super fast inverter | 2 |
| BUFF | Non-inverting buffer | 1 |
| BUFFB | Fast non-inverting buffer | 2 |
| BUFFC | Super fast non-inverting buffer | 3 |
| NAND2 | 2 input NAND | 1 |
| NAND2B | Fast 2 input NAND | 2 |
| NAND3 | 3 input NAND | 2 |
| NAND4 | 4 input NAND | 2 |
| AND2 | 2 input AND | 2 |
| AND3 | 3 input AND | 2 |
| AND4 | 4 input AND | 3 |
| NOR2 | 2 input NOR | 1 |
| NOR2B | Fast 2 input NOR | 2 |
| NOR3 | 3 input NOR | 2 |
| NOR4 | 4 input NOR | 2 |
| OR2 | 2 input OR | 2 |
| OR3 | 3 input OR | 2 |
| OR4 | 4 input OR | 3 |
| ANDNOR | 2 + 2 input AND/NOR | 2 |
| ORNAND | 2 + 2 OR/NAND | 2 |
| EXNOR | Exclusive NOR | 4 |
| EXOR | Exclusive OR | 4 |
| SEL2INV | Select 1 of 2 (inverting) | 4 |
| SEL2 | Select 1 of 2 | 4 |
| SEL4INV | 4 bit data selector (inverting) | 8 |
| SEL4 | 4 bit data selector | 8 |
| **ARITHMETIC** | | |
| HAD | Half adder | 4 |
| FAD | Full adder | 8 |
| FLAD | Fast look ahead adder | 6 |
| LAH2 | 2 bit look ahead unit | 12 |
| LAH3 | 3 bit look ahead unit | 16 |
| LAH4 | 4 bit look ahead unit | 25 |
| **SIMPLE LATCHES** | | |
| NASR | NAND set reset-latch | 3 |
| NOSR | NOR set-reset latch | 3 |
| **CLOCKED LATCHES** | | |
| DL | D-latch (Active low) | 4 |
| DLH | D-latch (Active high) | 4 |
| SDL | Set D-latch | 4 |
| RDL | Reset D-latch | 4 |
| SRDL | Set/reset D-latch | 6 |
| **EDGE TRIGGERED LATCHES** | | |
| RETS | | 8 |
| SRETS | | 8 |
| **MASTER-SLAVE FLIP-FLOPS** | | |
| DT | D-type | 6 |
| D2T | Dual input D-type | 8 |
| SDT | Set D-type | 4 |
| RDT | Reset D-type | 8 |
| SRDT | Set/reset D-type | 8 |

| Cell Name | Function | Cell Units |
|---|---|---|
| **TOGGLE FLIP-FLOPS** | | |
| STT | Set T-type | 8 |
| RTT | Reset T-type | 8 |
| SRTT | Set/reset T-type | 8 |
| **SYNCHRONOUS COUNTER** | | |
| SYNC | Synchronous counter stage | 8 |
| **REGISTERS / SHIFT REGISTERS** | | |
| SHR4 | Multibit serial register | 30 |
| SHR8 | Multibit serial register | 54 |
| RSHR4 | Multibit serial reg. with reset | 30 |
| RSHR8 | Multibit serial reg. with reset | 54 |
| DREG4 | Multibit parallel register | 15 |
| DREG8 | Multibit parallel register | 27 |
| DREGT4 | Multibit parallel register with tri-state outputs | 25 |
| DREGT8 | Multibit parallel register with tri-state outputs | 45 |
| **INVERTING TRI-STATE BUFFERS** | | |
| TRIBUFF | Tristate buffer (enable high) | 2 |
| TRIBUFFL | Tristate buffer (enable low) | 2 |
| TRINV | Tristate inv. buffer (enable high) | 2 |
| TRINVL | Tristate inv. buffer (enable low) | 2 |
| **INPUT OUTPUT AND PERIPHERAL CELLS** | | |
| TTLIP | TTLIN Non-inverting | |
| TTLIPN | TTLIN Inverting | |
| CMOSIP | CMOSIN Non-inverting | |
| CMOSIPN | CMOSIN Inverting | |
| CSCHMITT | CMOS Schmitt Non-inverting | |
| CSCHMITTN | CMOS Schmitt Inverting | |
| BOP | Buffered Output Non-inverting | |
| NOP | Buffered Output Inverting | |
| TRIOUT | Tri-state Output Non-inverting | |
| TRIOUTN | Tri-state Output Inverting | |
| BODN | Buffered Open Drain Output Pull Down | |
| NODN | Inverted Open Drain Output Pull Down | |
| BODP | Buffered Open Drain Output Pull Up | |
| NODP | Inverted Open Drain Output Pull Up | |
| PDOL | Pull Down 25k ohms approx | |
| PDOH | Pull Down 50k ohms approx | |
| PUPL | Pull Up 25k ohms approx | |
| PUPH | Pull Up 50k ohms approx | |
| **POWER SUPPLY PADS** | | |
| VDD | | |
| VSS | | |

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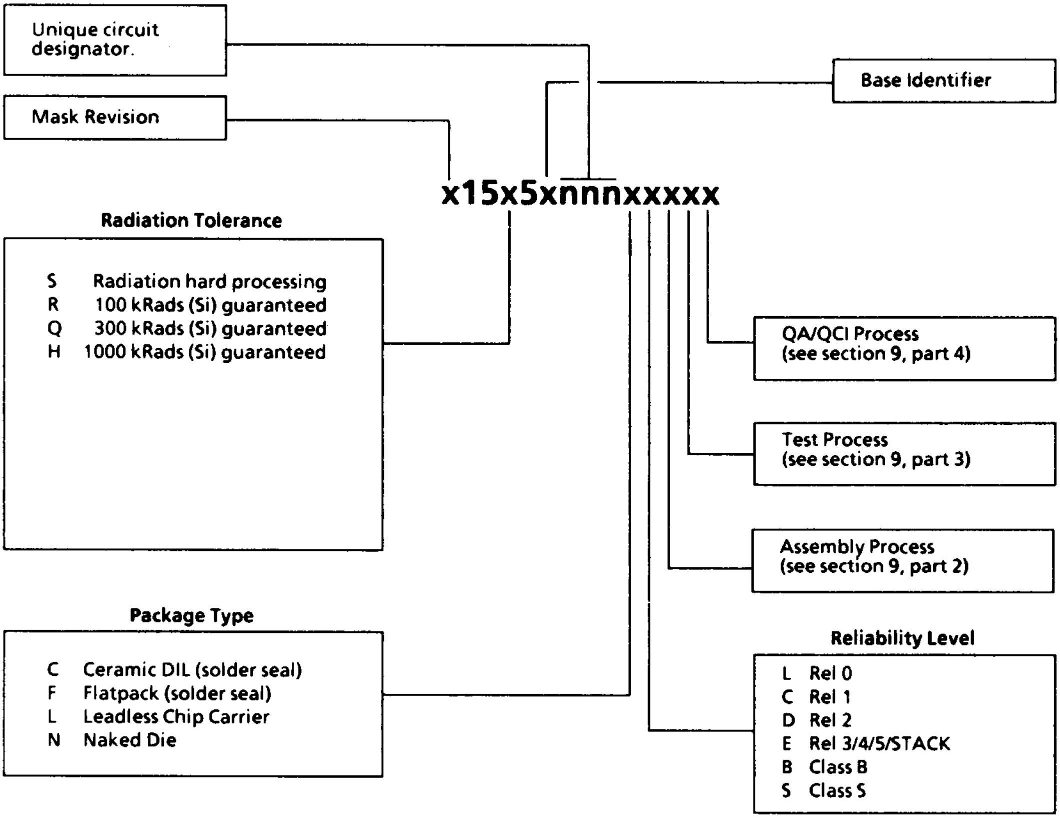
# MA9000A Sea of Gates

## Radiation Hard Advanced Gate Array Design System

### Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.




8