UPI™-C42
UNIVERSAL PERIPHERAL INTERFACE
CHMOS 8-BIT SLAVE MICROCONTROLLER

- Pin, Software and Architecturally Compatible with all UPI-41 and UPI-42 Products
- Integrated Auto A20 Gate Support
- Two New Power Down Modes
  — STANDBY
  — SUSPEND
- 8-Bit CPU plus ROM/OTP™ EPROM, RAM, I/O, Timer/Counter and Clock in a Single Package
- 4096 x 8 ROM/OTP, 256 x 8 RAM 8-Bit Timer/Counter, 18 Programmable I/O Pins
- One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface

- DMA, Interrupt, or Polled Operation Supported
- Fully Compatible with all Intel and Most Other Microprocessor Families
- Interchangeable ROM and OTP EPROM Versions
- Expandable I/O
- Sync Mode Available
- Over 90 Instructions: 70% Single Byte
- Quick Pulse Programming™ Algorithm — Fast OTP Programming
- Available in 40-Lead Plastic, 44-Lead Plastic Leaded Chip Carrier, and 44-Lead Quad Flat Pack Packages
  (See Packaging Spec., Order #240800-001, Package Type P, N, and S)

The UPI-C42 is an enhanced CHMOS version of the industry standard Intel UPI-42 family. It is fabricated on Intel's CHMOS III-E process. The UPI-C42 is pin, software, and architecturally compatible with the NMOS UPI family. The UPI-C42 has all of the same features of the NMOS family plus a larger user programmable memory array (4K), integrated auto A20 gate support, and lower power consumption inherent to a CHMOS product.

The UPI-C42 is essentially a "slave" microcontroller, or a microcontroller with a slave interface included on the chip. Interface registers are included to enable the UPI device to function as a slave peripheral controller in the MCS™ Modules and iAPX family, as well as other 8-, 16-, and 32-bit systems.

To allow full user flexibility, the program memory is available in ROM and One-Time Programmable EPROM (OTP).

290414-1

Figure 1. DIP Pin Configuration

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Figure 2. PLCC Pin Configuration

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Figure 3. QFP Pin Configuration