# PROGRAMMABLE TIMER

## GENERAL DESCRIPTION

MMC 361A, MMC 361B programmable timer is a metal gate CMOS integrated circuit. The circuit can drive a 4-digit display.
The 4 internal counters can be programmed to divide by: 10*10*10*10, 10*6*10*10, 10*10*24 or 10*6*24.
The counters transfer their content to the BCD outputs of the circuit in a multiplexed way. The circuit compares the state of the counters with that of 4 external „tumble-switches".
The coincidence is sensed as a 0-1-0 pulse or as a 0-1 step.

The circuit can be supplied in a 16-lead (MMC 361A) or in a 24-lead (MMC361B) dual-in-line package, according to the specific application.

## FEATURES

- wide supply range 3 . . . 18 V
- low current consumption: less than 1 mA
- available in 16-lead (MMC 361A) or 24-lean (MMC 361B) dual-in-line package

## ABSOLUTE MAXIMUM RATINGS

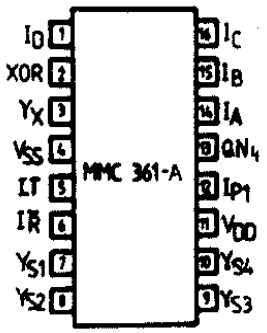
| | | | | |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | −0.5 . . . | 18 | V |
| $V_I$ | Input voltage | −0.5 . . . | $V_{DD}$ + 0.5 | V |
| $I_I$ | DC input current | +10 mA | | |
| $P_D$ | Total power dissipation | 200 mW | | |
| $T_A$ | Operating temperature | −40 . . . | + 85 | °C |
| $T_S$ | Storage temperature | −65 . . . | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

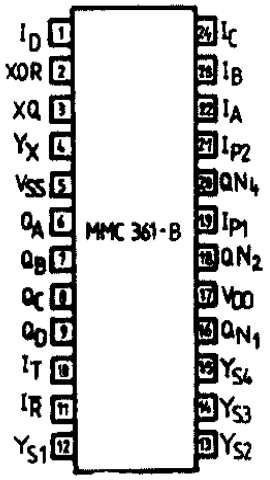
| | | | | |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3 . . . | 15 | V |
| $V_I$ | Input voltage | 0 . . . | $V_{DD}$ | |
| $T_A$ | Operating temperature | −40 . . . | +85 | °C |

## CONNECTION DIAGRAM

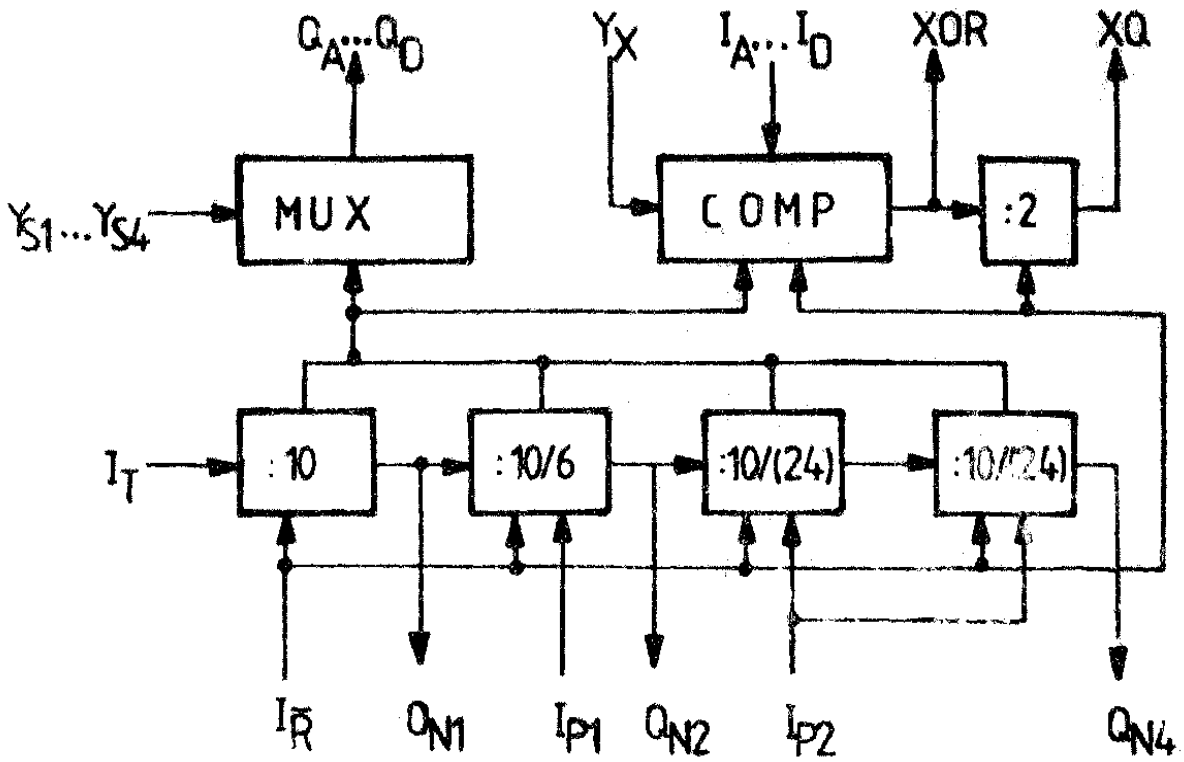
### MMC 361A




### MMC 361B



## BLOCK DIAGRAM




## FUNCTIONAL DESCRIPTION

The clock input, $I_T$, is applied to a chain of 4 counters at rates in the range 0 ... 100 Hz.
According to the connection to $V_{SS}$ of the inputs $I_{P1}$, $I_{P2}$, the counters can be programmed to divide by:

10*10*10*10 — $I_{P1}$, $I_{P2}$ not connected
10*6*10*10 — $I_{P1}$ to $V_{SS}$, $I_{P2}$ not connected
10*10*24 — $I_{P2}$ not conected, $I_{P2}$ to $V_{SS}$
10*6*24 — $I_{P1}$, $I_{P2}$ to $V_{SS}$

The transfer from the outputs of the 4 counters to the BCD outputs of the circuit, $Q_A$ ... $Q_D$, is controlled by the 25% duty cycle, 1 KHz frequency multiplexing signals $Y_{S1}$ ... $Y_{S4}$.
The circuit compares the state of the counters with the information received at the $I_A$ ... $I_D$ inputs from 4 „tumbles-witches", controlled by the multiplexing signals $Y_{S1}$ ... $Y_{S4}$.
In order to sense coincidence, a signal of period equal to the width of the multiplexing signals $Y_{S1}$ ... $Y_{S4}$ is applied at input $Y_X$ to a chain of 2 flip-flops inside the compare logic.
The coincidence is sensed as a pulse 0—1—0 at XOR output and as a step 0—1 at XQ output; in order to directly drive LEDs, these outputs have NPN bipolar transistors connected to $V_{DD}$.
A low level on the $I_{\overline{R}}$ input resets to 0 the flip-flops of the circuit; Schmitt Trigger action on this input permits unlimited clock rise and fall times.
For the option in 16-lead package (MMC 3621A), the programming input $I_{P2}$, the BCD outputs $Q_A$ ... $Q_D$ and the serial outputs $Q_{N1}$ ... $Q_{N4}$ are not connected.

## STATIC ELECTRICAL CHARACTERISTICS

| PARAMETER | | | TEST CONDITIONS $V_I$ (V) | $V_O$ (V) | $I_O$ (μA) | $V_{DD}$ (V) | VALUES $T_{LOW}$ min. | $T_{LOW}$ max. | 25°C min. | 25°C max. | $T_{HIGH}$ min. | $T_{HIGH}$ max. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_L$ | Quiescent current | G, H types | 0/ 5 | | | 5 | | 20 | | 20 | | 600 | μA |
| | | | 0/10 | | | 10 | | 40 | | 40 | | 1200 | |
| | | | 0/15 | | | 15 | | 80 | | 80 | | 2400 | |
| | | | 0/20 | | | 20 | | 400 | | 400 | | 12000 | |
| | | E, F types | 0/ 5 | | | 5 | | 80 | | 80 | | 600 | |
| | | | 0/10 | | | 10 | | 160 | | 160 | | 1200 | |
| | | | 0/15 | | | 15 | | 320 | | 320 | | 2400 | |
| $V_{OH}$ | Output high voltage | | 0/ 5 | | < 1 | 5 | 4 | | 4 | | 4 | | V |
| | | | 0/10 | | < 1 | 10 | 9 | | 9 | | 9 | | |
| | | | 0/15 | | < 1 | 15 | 14 | | 14 | | 14 | | |
| $V_{OL}$ | Output low voltage | | 5 /0 | | < 1 | 5 | | 0.05 | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input high voltage | | | 0.5/4.5 | < 1 | 5 | 4.95 | | 4.95 | | 4.95 | | V |
| | | | | 1/9 | < 1 | 10 | 9 | | 9 | | 9 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 12 | | 12 | | 12 | | |
| $V_{IL}$ | Input low voltage | | | 4.5/0.5 | < 1 | 5 | | 1.35 | | 1.35 | | 1.35 | V |
| | | | | 9/1 | < 1 | 10 | | 1.9 | | 1.9 | | 1.0 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 2.7 | | 2.7 | | 2.7 | |
| $I_{IH}$ | Input leakage curent | G, H types | 0/18 | | | 18 | | .1 | | 1 | | 1.0 | μA |
| | | E, F types | 0/15 | | | 15 | | .3 | | .3 | | 1.0 | |
| $I_{IL}$ | Input leakage curent | G, H types | 0/18 | | | 18 | | .25 | | .25 | | 2.5 | mA |
| | | E, F types | 0/15 | | | 15 | | .75 | | .75 | | 2.5 | |
| $I_{OH}$ | Output drive current | G, H types | 0/ 5 | 2.5 | | 5 | −2.0 | | −1.6 | | −1.1 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | −0.6 | | −0.5 | | −0.3 | | |
| | | | 0/10 | 9.5 | | 10 | −1.6 | | −1.3 | | −0.9 | | |
| | | | 0/15 | 13.5 | | 15 | −4.2 | | −3.4 | | −2.4 | | |
| | | E, F types | 0/ 5 | 2.5 | | 5 | −1.5 | | −1.3 | | −1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | −0.5 | | −0.4 | | −0.3 | | |
| | | | 0/10 | 9.5 | | 10 | −1.3 | | −1.1 | | −0.9 | | |
| | | | 0/15 | 13.5 | | 15 | −3.6 | | −3.0 | | −2.4 | | |
| $I_{OL}$ | Output sink current | G, H types | 0/ 5 | 0.4 | | 5 | 0.6 | | 0.5 | | 0.3 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | | 2.4 | | |
| | | E, F types | 0/ 5 | 0.4 | | 5 | 0.5 | | 0.4 | | 0.3 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | | 2.4 | | |
| $C_I$ | Input capacitance | | Any input | | | | | | | 7.5 | | | pF |

## DYNAMIC ELECTRICAL CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS $V_{DD}$ (V) | VALUES min. | VALUES max. | UNIT |
|---|---|---|---|---|---|
| $t_{PLH}$ YQ, $t_{PHL}$ YQ | Propagation delay time $Y_{S1}...Y_{S4}$—$Q_A...Q_D$ | 15 | | 750 | ns |
| $t_{PLH}$ IQ, $t_{PHL}$ IQ | Propagation delay time $I_T$—$Q_A...Q_D$ | 15 | | 3 | µs |
| $t_{TLHL}$, $t_{THL}$ | Transition time $Q_A...Q_D$ | 15 | | 150 | ns |
| $f_{CK}$ | Clock frecuency $I_T$ | 5<br>15 | | 400<br>800 | KHz |