iT2025J

30 kHz to 18 GHz High-Gain Power Amplifier

Description

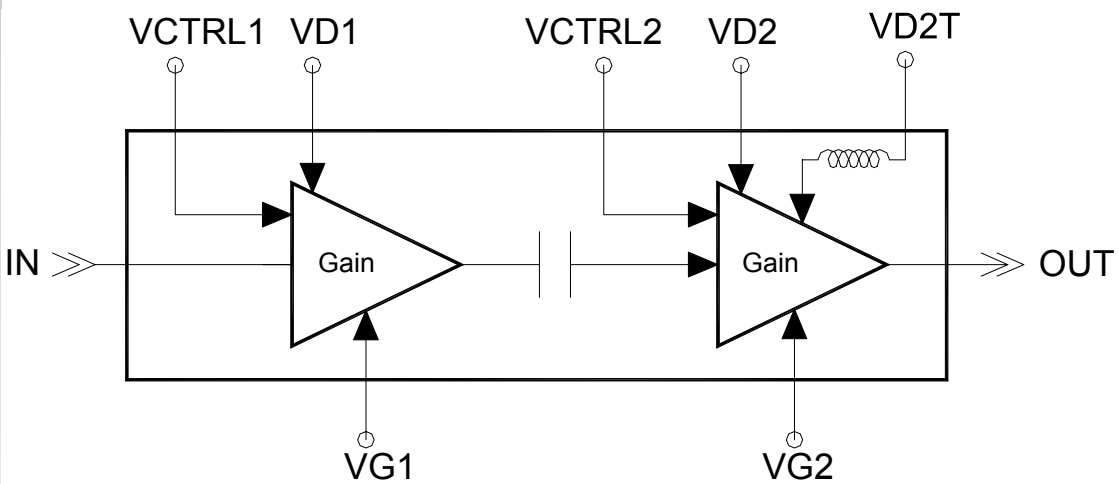
The iT2025J is a RoHS-6-compliant packaged broadband GaAs MMIC traveling wave amplifier designed for medium output power applications where low-frequency extension capabilities are also required. The iT2025J provides saturated output power greater than 25 dBm up to 8 GHz, greater than 23 dBm up to 16 GHz, and greater than 20 dBm at 18 GHz. Average gain is greater than 25 dB. DC power consumption as low as 2.4 W. Input/output ports are DC coupled.

Features

- Frequency range: 2 GHz – 18 GHz with low-frequency extension capability down to 30 KHz
- >25 dBm nominal Psat (30 kHz – 8 GHz)
- >20 dBm nominal Psat (30 kHz – 18 GHz)
- >25 dB nominal gain up to 18 GHz
- 2.4 W DC power consumption
- Nominal DC bias conditions: 8 V at 300 mA
- Full chip passivation for high reliability
- RoHS-6-compliant small-form-factor (0.450 x 0.350 x 0.078 in.) SMD package

Device Diagram

Both gain stages and their respective RF and DC connections are shown at right. The internal coupling capacitor value between the cascaded gain stages is 0.1 µF. VD1 and VD2 are applied to the gain stages through on-chip resistors.



Recommended bias conditions:

VD1 = 8 V, VG1 = -0.8 V to – 0.9 V, VCTRL1 = 0 V, ID1 = 80 mA
VD2T = 8 V, VG2 = -0.5 V to -0.7 V, VCTRL2 = +3.5 V, ID2T = 220 mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Drain voltage	V_{D1}, V_{D2}, V_{D2T}		10.0	V	1
Gate voltage	V_{G1}, V_{G2}	-2.5		V	1
Control voltage	V_{CTRL1} V_{CTRL2}	V_{D1} - 8V V_{D2T} - 8V	V_{D1} V_{D2T}	V	1
Drain current	I_{D1}, I_{D2} I_{D2T}		150 300	mA	1,2
Input power	P_{IN}		5	dBm	
Power dissipation	P_D		4	W	1
Junction operating temperature	T_J		150	°C	3
Mounting temperature	T_M		230	°C	
Storage temperature	T_{STO}	-65	150	°C	
Storage relative humidity	RH_{STO}	5	95	%	

Notes:

1. Combinations of drain voltage, drain current, and output power shall not exceed P_D at package base temperature of 85° C.

2. Set VG1 and VG2 such that drain currents are below maximum limits.

3. See “Thermal Characteristics”.

Electrical Characteristics

(at 25 °C) in 50-ohm system.

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range*	0.00003		18	GHz
S21	Small-signal gain	24	30		dB
S11	Input return loss	10	12		dB
S22	Output return loss	7	10		dB
S12	Isolation	50			dB
Psat	Saturated power output (3-dB gain compression) 30 Hz – 8 GHz 30 kHz – 18 GHz	 24 19	 26 21		 dBm dBm
P1dB	Output power (1-dB gain compression) 30 kHz – 8 GHz 30 kHz – 18 GHz	 22 17	 24 20		 dBm dBm
OIP3	Output third-order intercept point		32		dBm
NF	Noise figure 500 MHz – 2 GHz 2 GHz – 10 GHz 10 GHz – 18 GHz			 5.5 4.5 6.0	 dB dB dB

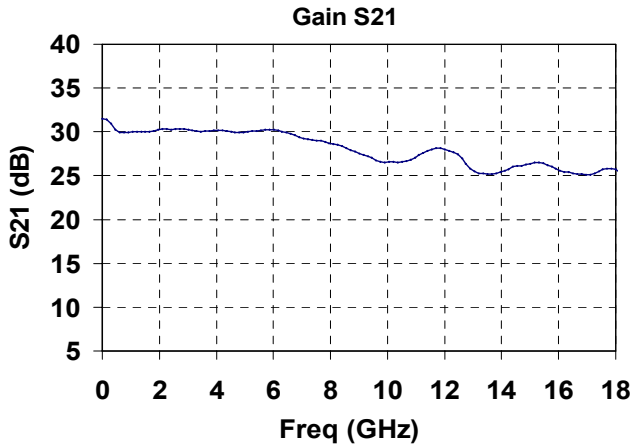
(*) Low-frequency extension available with recommended choke network.

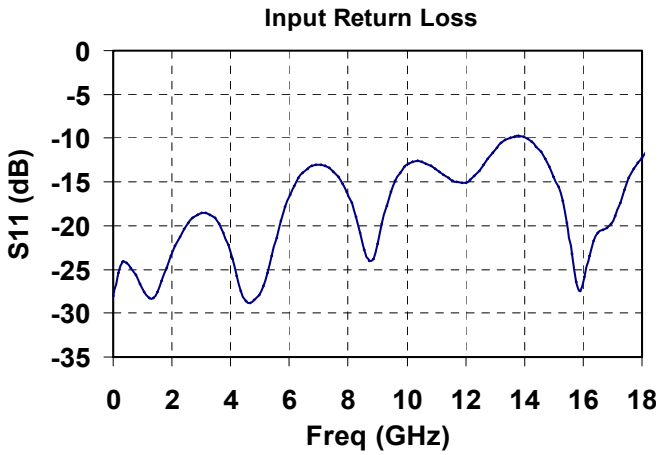
Performance Data

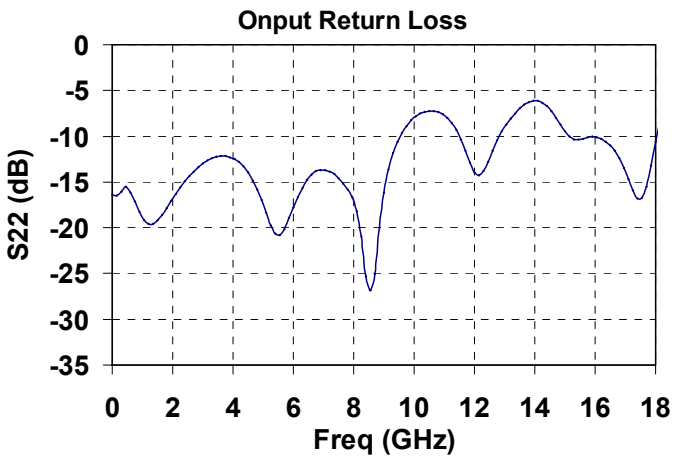
T = 25° C

Test includes effects of evaluation board.

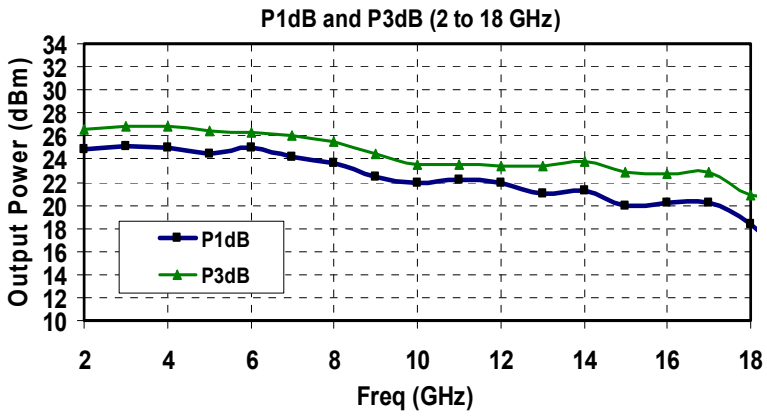
VD1 = 8 V
VCTRL1 = 0 V
ID1 = 80 mA
VD2T = 8 V
VCTRL2 = +3.5 V
ID2T = 220 mA

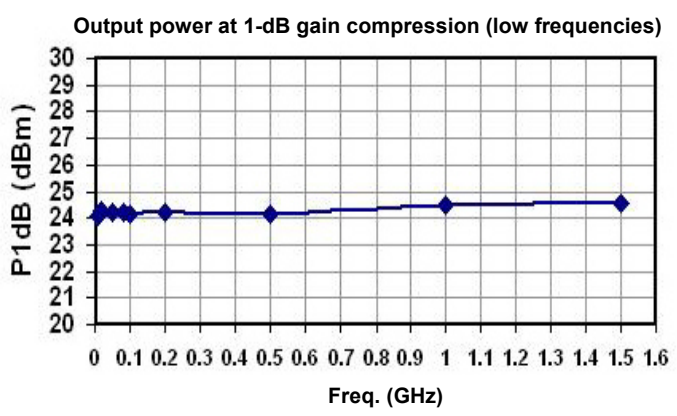


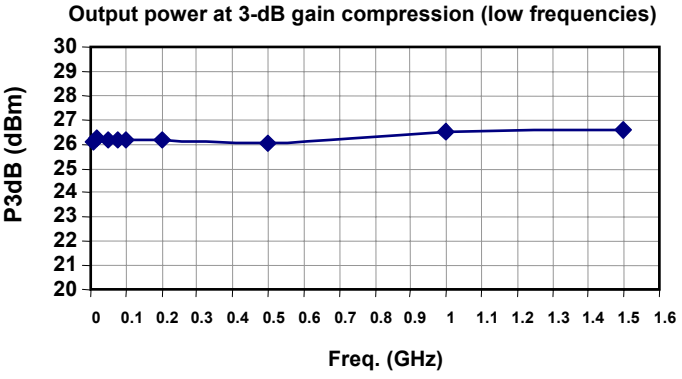




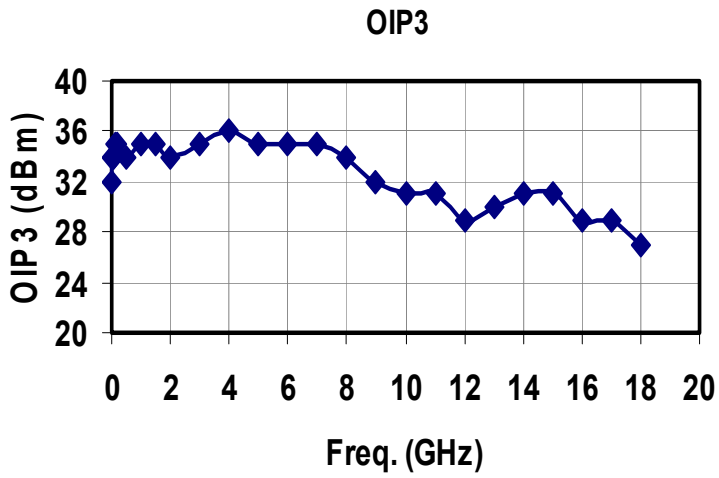
Output Power Performance



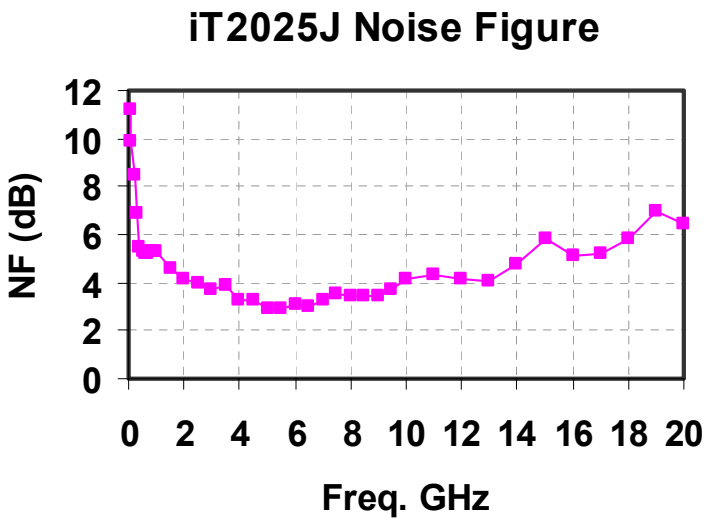




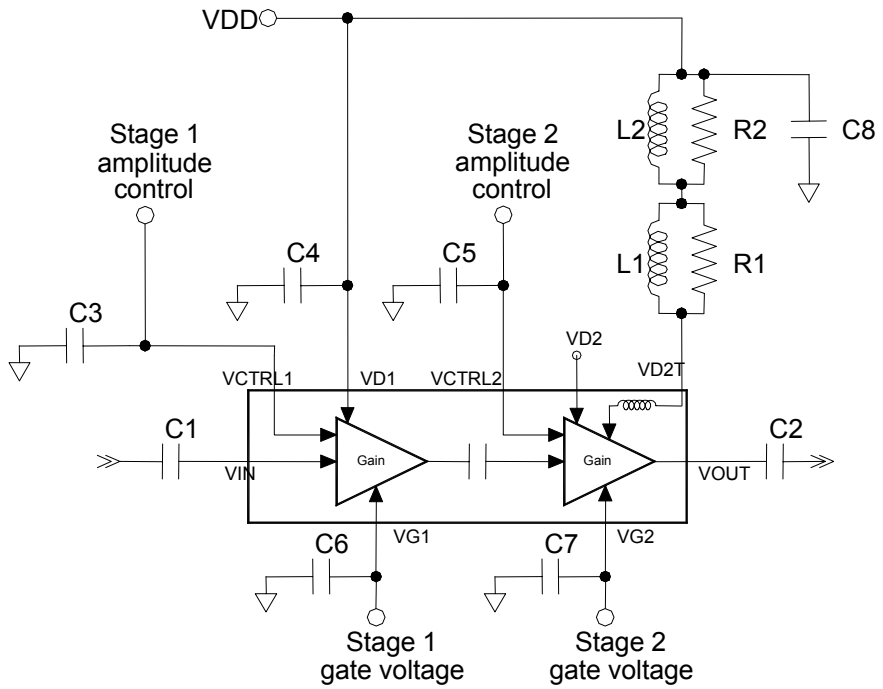
Output Power Performance (cont.)



Noise Figure



Circuit Design for low-Frequency Extension Applications to 30 kHz*



Reference Designation	Description	Manufacturer	Part Number
C1, C2	0.10 µF cap, 0402, X5R, 10 V	Panasonic	ECJ-0EB1A104K
C3 – C8	1.00 µF cap, 0603, X5R, 16 V	Panasonic	ECJ-1VB1C105K
R1, R2	180 ohm resistor, 0402, 5%	Panasonic	ERJ-2GEJ181X
L1	0.33 µH inductor	Toko America	FSLU2520-R33K
L2	100 µH inductor	Coilcraft	DO1608-104MLB

This application circuit is used on the iT2025J evaluation board, which is available to customers who desire a convenient test platform for this product. The iT2025J design was verified with the components and configuration described above. Note that VD2 is not used in this configuration. C1 and C2 are coupling capacitors for the RF input and output. High-performance capacitors (such as those manufactured by Presidio) may be substituted. C3 to C8 are power supply decoupling capacitors. L1, L2, R1, and R2 are the required external components for the choke network that supplies the output stage bias current for applications down to 30 kHz. These components can be replaced with different values if the low-frequency cutoff is higher than 30 kHz.

(*) For applications in which the minimum frequency is 2 GHz, L1, L2, R1, and R2 can be removed and only C8 is required.

Package Details

Notes:

1. Tolerances on package length and width are ± 0.005 in.

2. Tolerance on package height is ± 0.006 in.

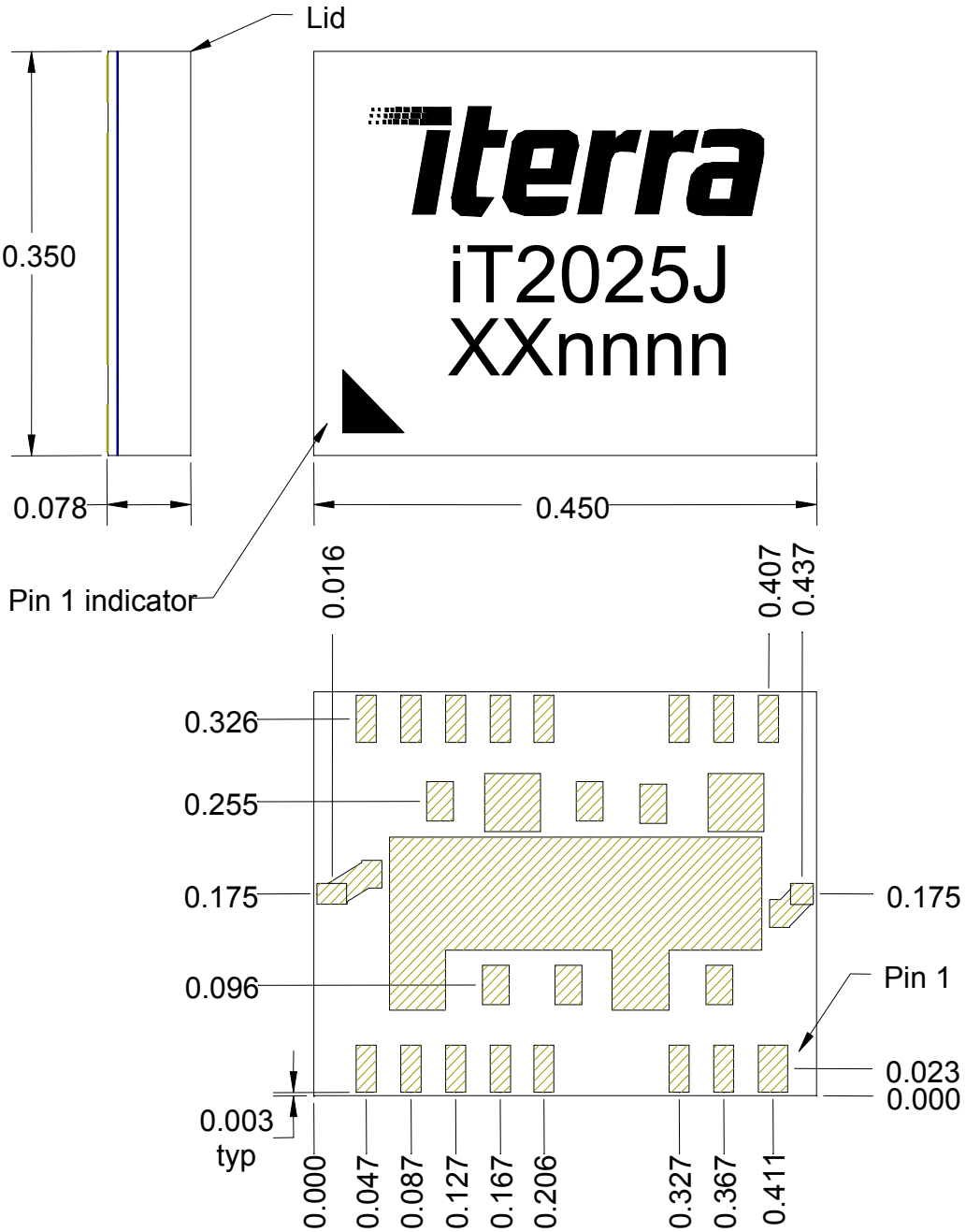
3. Tolerances on all pad dimensions and features are ± 0.002 in.

4. Substrate material: RO4003, 0.008-in.-thick, ½ oz. copper.

5. Plating: 100 to 350 µin nickel, 5 to 10 µin. flash gold finish.

6. Package footprint available in DXF format. Contact iTerra Communications for details.

7. RoHS compliant. Backward compatible with SnPb soldering.



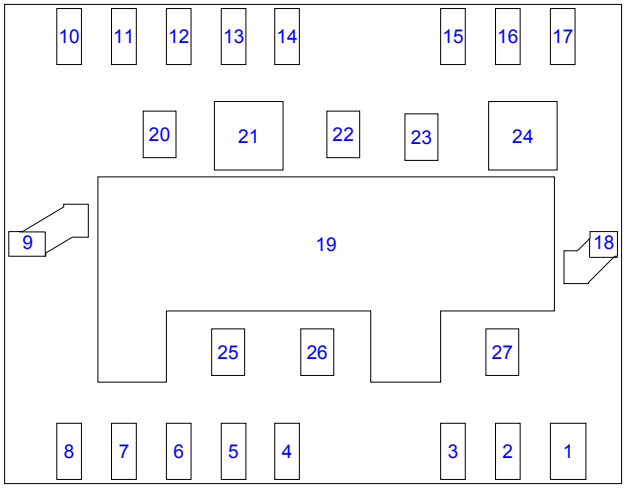
Pad Details

Notes:

1. Pad widths and heights are in mils.

2. Pads 19 to 27 are ground pads. Although they are shown as independent structures, they should all be connected to one contiguous ground pad on the application board.

3. Package footprint available in DXF format. Contact iTerra Communications for details.



Pad	Function	Width	Height	Pad	Function	Width	Height
1	N/C	26	41	10	N/C	18	41
2	N/C	18	41	11	N/C	18	41
3	V_{G1}	18	41	12	V_{D2T}	18	41
4	N/C	18	41	13	V_{D2}	18	41
5	N/C	18	41	14	V_{CTRL2}	18	41
6	V_{G2}	18	41	15	V_{D1}	18	41
7	N/C	18	41	16	N/C	18	41
8	N/C	18	41	17	V_{CTRL1}	18	41
9	V_{OUT}	27	18	18	V_{IN}	20	18

Thermal Characteristics

The thermal impedance between the package base (ground pad 19) and each amplifier junction (**θ**JB) is approximately 25°C/W. Consider this thermal impedance as well as thermal conditions in the final application and the desired iT2025J bias settings to keep internal junction temperatures below their specified limits.

The following formulas may be used to calculate the operating junction temperatures (TJ1 and TJ2) for each of the two cascaded amplifiers in the iT2025J.

$TJ1 = TBASE + (VD1 \times ID1) \times 25^{o}\ C/W$

$TJ2 = TBASE + (VD2T \times ID2T) \times 25\ C/W$

or

$TJ2 = TBASE + (VD2 \times ID2) \times 25\ C/W$