YDA146

D-530

STEREO 5W-30W DIGITAL AUDIO POWER AMPLIFIER

■Overview

YDA146 (D-530) is a high-efficiency digital audio power amplifier IC with the maximum output of 30W × 2ch.
YDA146 has a "Pure Pulse Direct Speaker Drive Circuit" that directly drives speakers while reducing distortion of pulse output signal and reducing noise on the signal, which realizes the highest standard low distortion rate characteristics and low noise characteristics among digital amplifier ICs in the same class.
In addition, supporting filterless design allows circuit design with fewer external parts to be realized depending on use conditions.
YDA146 features Power Limit Function, Non-clip Function, and DRC (Dynamic Range Control) Function that were developed by Yamaha original digital amplifier technology.
YDA146 has overcurrent protection function for speaker output terminals, high temperature protection function, and lowsupply voltage malfunction prevention function.

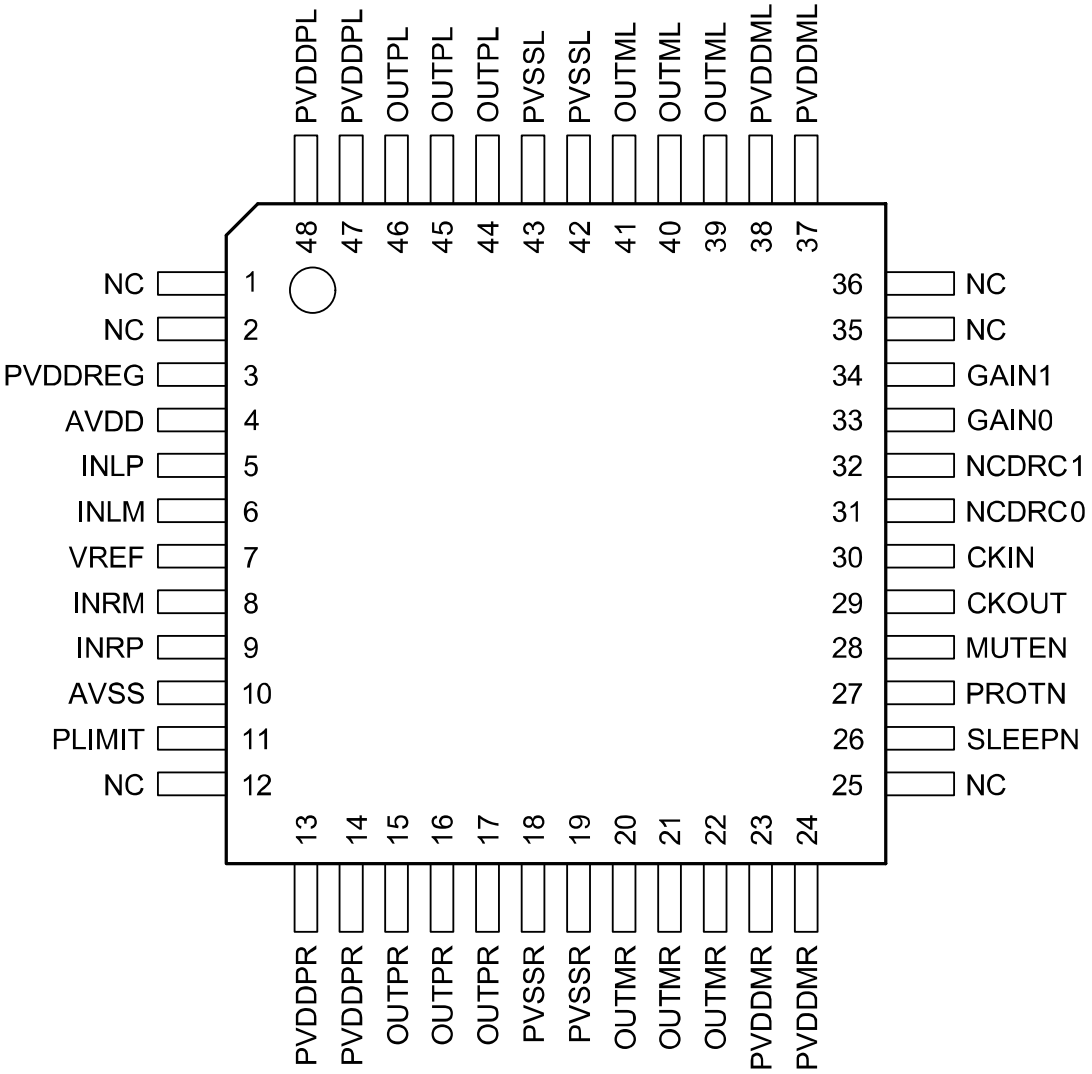
■Features

- Operating supply voltage range
  PVDD: 8.0V to 16.5V
- Maximum momentary output
  30 W×2ch (V_{DDP}=15V, R_L=4Ω, THD+N=10%)
  20 W×2ch (V_{DDP}=14V, R_L=4Ω, THD+N=10%)
- Maximum continuous output
  15 W*[1]×2ch (V_{DDP}=15V, R_L=8Ω, THD+N=10%, Ta=70°C)
  13.5W*[1]×2ch (V_{DDP}=15V, R_L=4Ω, THD+N=10%, Ta=25°C)
- Distortion Rate (THD+N)
  0.02 % (V_{DDP}=12V, R_L=8Ω, Po=0.2W, 1kHz)
- Residual Noise
  48μVrms (V_{DDP}=12V, GAIN[1:0]=L,L, NCDRC[1:0]=L,L)
- Efficiency
  92 % (V_{DDP}=12V, R_L=8Ω)
- S/N Ratio
  105 dB (V_{DDP}=12V, GAIN[1:0]=L,L, NCDRC[1:0]=L,L)
- Channel separation
  -80 dB (V_{DDP}=12V, GAIN[1:0]=L,L, NCDRC[1:0]=L,L)
- PSRR
  60dB (V_{DDP}=12V,Vripple=100mV, 1kHz, GAIN[1:0]=L,L, NCDRC[1:0]=L,L)
- Non-clip function/DRC function (switchable)
- Power limit function
- Clock External Synchronization Function
- Master/Slave Synchronization Function using clock outputs
- Over-current Protection Function, High Temperature Protection Function, Low Voltage Malfunction Prevention Function, and DC Detection Function
- Sleep Function using SLEEPN terminal and Output Mute Function using MUTEN terminal
- Spread Clock Function
- Pop Noise Reduction Function
- Package
  Lead-free 48-pin Plastic SQFP (Exposed stage)

Note) *1: A value based on Yamaha's board implementation conditions (See Note *2 of page 26)

YDA146 CATALOG
CATALOG No.:LSI-4DA146A51
2009.1

■Terminal Configuration



< 48-pin SQFP Top View >

■Terminal Function

No.	Name *4)	I/O *1), *2), *3)	Function
1	NC	—	Normally, use this terminal in no-connection
2	NC	—	Normally, use this terminal in no-connection
3	PVDDREG	PVDD	Power supply terminal for regulators
4	AVDD	OA	3.3V regulator output terminal
5	INLP	IA	Analog input terminal (Lch+)
6	INLM	IA	Analog input terminal (Lch-)
7	VREF	OA	Reference voltage output terminal
8	INRM	IA	Analog input terminal (Rch-)
9	INRP	IA	Analog input terminal (Rch+)
10	AVSS	GND	Analog ground terminal
11	PLIMIT	IA	Power limit setting terminal
12	NC	—	Normally, use this terminal in no-connection
13	PVDDPR	PVDD	Power supply terminal for digital amplifier output (Rch+)
14	PVDDPR	PVDD	Power supply terminal for digital amplifier output (Rch+)
15	OUTPR	O	Digital amplifier output terminal (Rch+)
16	OUTPR	O	Digital amplifier output terminal (Rch+)
17	OUTPR	O	Digital amplifier output terminal (Rch+)
18	PVSSR	GND	Ground terminal for digital amplifier output (Rch)
19	PVSSR	GND	Ground terminal for digital amplifier output (Rch)
20	OUTMR	O	Digital amplifier output terminal (Rch-)
21	OUTMR	O	Digital amplifier output terminal (Rch-)
22	OUTMR	O	Digital amplifier output terminal (Rch-)
23	PVDDMR	PVDD	Power supply terminal for digital amplifier output (Rch-)
24	PVDDMR	PVDD	Power supply terminal for digital amplifier output (Rch-)
25	NC	—	Normally, use this terminal in no-connection
26	SLEEPN	I	Sleep control terminal *5)
27	PROTN	O/D	Error flag output terminal
28	MUTEN	I	MUTE control terminal
29	CKOUT	O	Clock output terminal for synchronization
30	CKIN	I	External clock input terminal
31	NCDRC0	I	Non-clip/DRC1/DRC2 mode selection terminal 0
32	NCDRC1	I	Non-clip/DRC1/DRC2 mode selection terminal 1
33	GAIN0	I	GAIN setting terminal 0
34	GAIN1	I	GAIN setting terminal 1
35	NC	—	Normally, use this terminal in no-connection
36	NC	—	Normally, use this terminal in no-connection
37	PVDDML	PVDD	Power supply terminal for digital amplifier output (Lch-)
38	PVDDML	PVDD	Power supply terminal for digital amplifier output (Lch-)
39	OUTML	O	Digital amplifier output terminal (Lch-)
40	OUTML	O	Digital amplifier output terminal (Lch-)
41	OUTML	O	Digital amplifier output terminal (Lch-)
42	PVSSL	GND	Ground terminal for digital amplifier output (Lch)
43	PVSSL	GND	Ground terminal for digital amplifier output (Lch)
44	OUTPL	O	Digital amplifier output terminal (Lch+)
45	OUTPL	O	Digital amplifier output terminal (Lch+)
46	OUTPL	O	Digital amplifier output terminal (Lch+)
47	PVDDPL	PVDD	Power supply terminal for digital amplifier output (Lch+)
48	PVDDPL	PVDD	Power supply terminal for digital amplifier output (Lch+)

(Note) *1 I: Input terminal, O: Output terminal, A: Analog terminal, O/D: Open/Drain output terminal

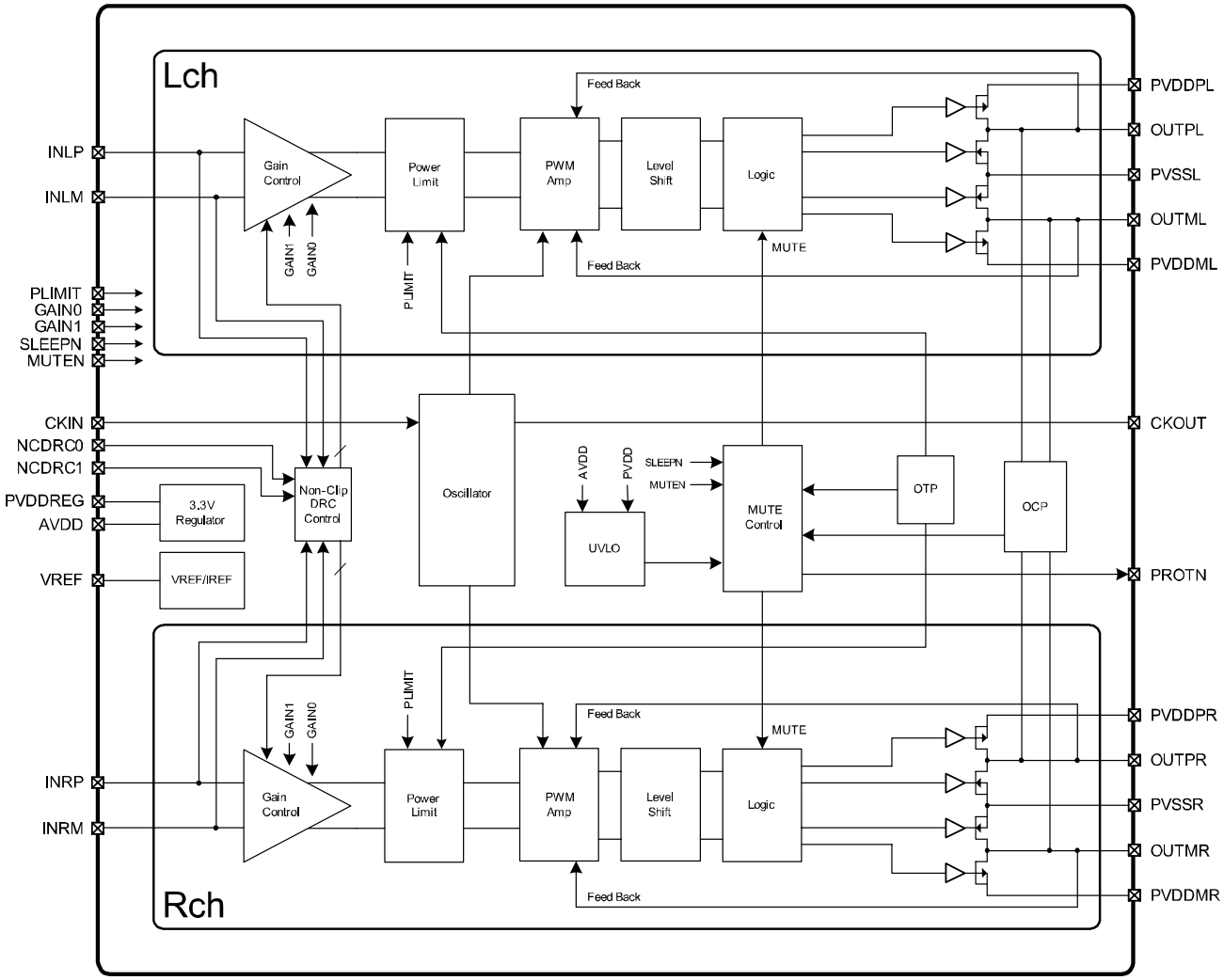
*2 PVDD should be connected each other on a board.

*3 GND should be connected each other on a board.

*4 Each output terminal with the same name (OUTPR, OUTMR, OUTPL, and OUTML) should be connected on a board.

*5 Do not use AVDD pin to apply "H" level to SLEEPN pin.
The device will not start when using AVDD pin as "H" level signal because AVDD goes up at the time SLEEPN pin becomes "H".

■Block Diagram



■Functional Description

● Digital Amplifier Function

YDA146 has digital amplifiers with analog input, PWM pulse output, the maximum output of 30W × 2ch.
Adopting "Pure Pulse Direct Speaker Drive Circuit" reduces distortion and noise on PWM pulse output signal.

・Digital Amplifier Gain

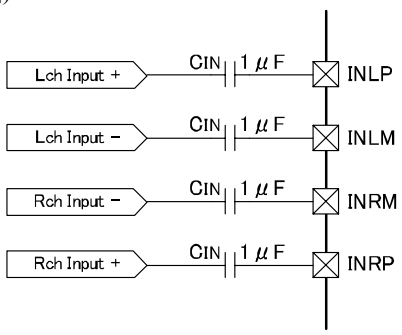
The total gain of the digital amplifier varies depending on operation modes, as shown below.

NCDRC1	NCDRC0	GAIN1	GAIN0	Total Gain	Operation Mode
L	L	L	L	+22dB	Normal mode Non-clip: OFF DRC: OFF
		L	H	+28dB	
		H	L	+34dB	
		H	H	+16dB	
L	H	L	L	+34dB	Non-clip mode
		L	H	+40dB	
		H	L	+46dB	
		H	H	+28dB	
H	L	L	L	+34dB	DRC1 mode
		L	H	+40dB	
		H	L	+46dB	
		H	H	+28dB	
H	H	L	L	+34dB	DRC2 mode
		L	H	+40dB	
		H	L	+46dB	
		H	H	+28dB	

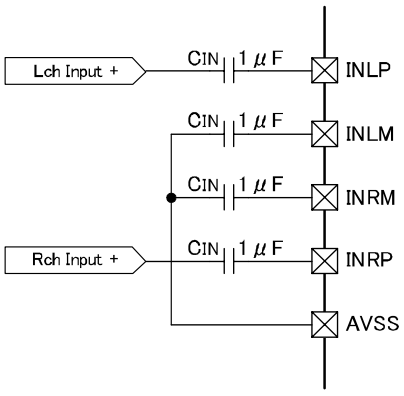
・Audio Signal Input

For a differential input, the signal should be input to INLP and INLM terminals (Lch) and to INRP and INRM terminals (Rch) through a DC-cut capacitor (C_{IN}).

On the contrary, for a single-ended input, the signal should be input to INLP terminal (Lch) and to INRP terminal (Rch) through a DC-cut capacitor (C_{IN}). At this time, INLM and INRM terminals should be connected to AVSS through DC-cut capacitors (C_{IN}) with the same value.



Input terminal connection in a differential input



Input terminal connection in a single-ended input

In the differential input mode, use signal sources with the same impedance to reduce pop-noise. Its value should be 10kΩ or less. Use a DC-cut capacitor (C_{IN}) of 1μF. (The capacitance value should be less than 1.5μF throughout the operating temperature range.)

(Cautions)
When inputting audio signals in Power-off state (PVDD < V_{HUVLL}) or Sleep state, current may flow toward the former device from YDA146's ground, through each protection circuit of analog pins (INLP, INLM, INRP, and INRM).
For this reason, audio signals should not be input in Power-off state (PVDD < V_{HUVLL}) or Sleep state.

・Input Impedance

The input impedance (Z_{IN}) is 18.8kΩ regardless of a Gain setting.

・Reference Voltage Output Function

Half a voltage of AVDD terminal is output to the reference voltage terminal (VREF).
Connect a capacitor of 0.1μF for voltage stabilization.

・Maximum Output

The output varies depending on load impedance and a supply voltage, as shown below.

Maximum momentary Output	30W×2ch	(PVDD=15V, R_L=4Ω, THD+N=10%)
	20W×2ch	(PVDD=14V, R_L=4Ω, THD+N=10%)
Maximum Continuous Output	15W×2ch	(PVDD=15V, R_L=8Ω, THD+N=10%, Ta=70℃)
	13.5W×2ch	(PVDD=15V, R_L=4Ω, THD+N=10%, Ta=25℃)

The maximum momentary output means a possible maximum output by considering heat problems due to power loss separately.

The maximum continuous output means a maximum output with Tjmax not exceeding 150°C at a given temperature while outputting a sine wave continuously. In addition, this value is based on Yamaha's board implementation conditions. (See Note *2 of Page 26)

A possible maximum continuous output in other settings can be converted by the following data:

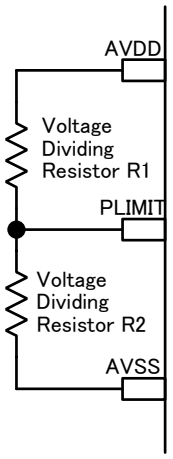
1. Graph of Power Dissipation vs Output Power of Example of typical characteristics. (See Page 30)
2. Power Dissipation of Electrical Characteristics. (See Page 26)

●Control Function

・Output Power limit Function

This is the function to set a voltage at which the output is clipped.
At this time, a value at which the output is clipped is defined as a power limit value (V_{PL}).
Using this function prevents increase of temperature in a device as well as allowing the maximum output power to be limited.
The output power limit value is determined by a voltage (voltage dividing resistor 1, 2) applied to PLIMIT terminal.
In addition, changing the voltage at PLIMIT terminal during power-on is prohibited.

The relation between a resistor ratio (R2/(R1+R2)(between voltage dividing resistor 1 and 2) and an output power with a 10% distortion is shown below.
Since it may vary between MIN and MAX due to variation of internal AVDD, select resistors in consideration of the variation.



PLIMIT terminal setting circuit

PLIMIT resistor R1 and R2 should be set as follows.

R1+R2=500kΩ or less

R1//R2=50kΩ to 70kΩ (R1//R2 means a parallel resistance between R1 and R2)

Example 1: 4Ω max30W (8Ω max15W)

R1=220k+4.7k, 、R2=75k

Example 2: 8Ω min10W

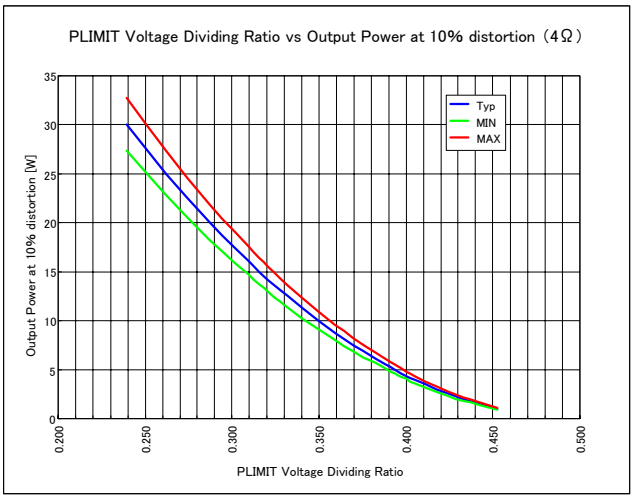
R1=200k, R2=75k+1.5k

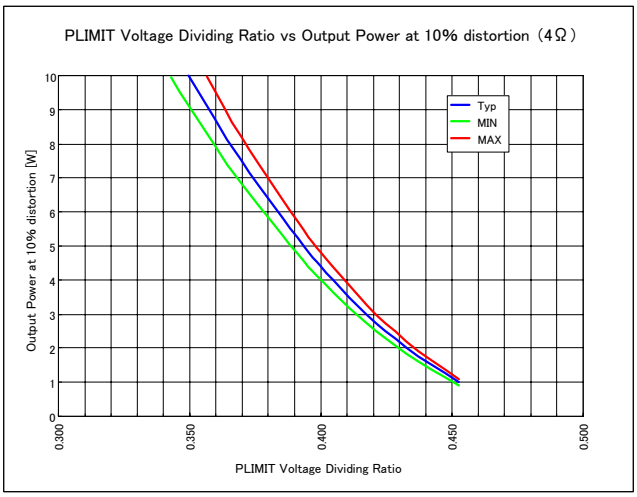
* Minimum value restriction on the output power limit.
The minimum value of the output-power limit values is restricted by the value determined with the resistance voltage division ratio of "0.45."
Even though the resistance voltage division ratio is set beyond "0.45," the output-power limit value wouldn't be set lower.

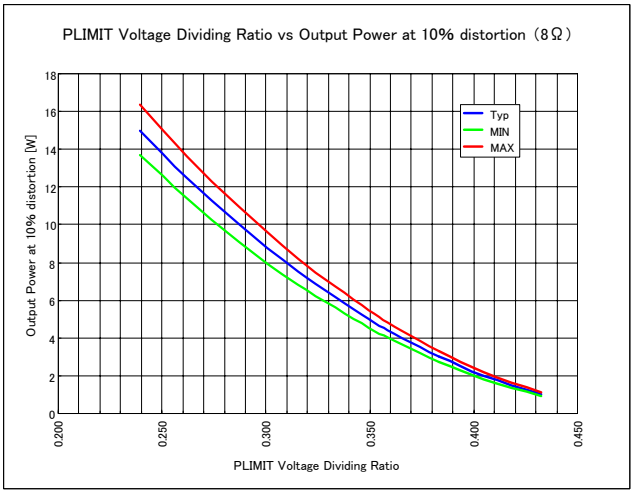
* Cancellation of the output power limit function.
It is possible to disable the power limit by setting "0"V (voltage division ratio "0") to the PLIMIT pin.
However, it is necessary to set the power limit value when the following function is used.
- Non-clip function (Non-clip/DRC Function : P.9).
- DRC function (Non-clip/DRC Function : P.9).
- High Temperature Power Limiter State of High Temperature Protection
(High Temperature Protection Function : P.18).

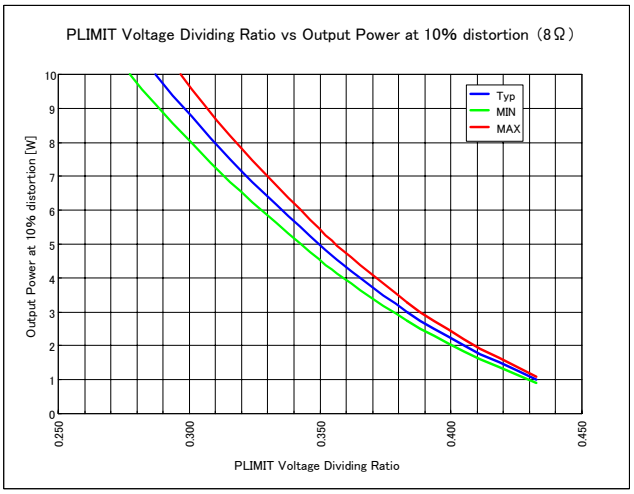
For the relation between each function and the power limit value, see the item of each function.

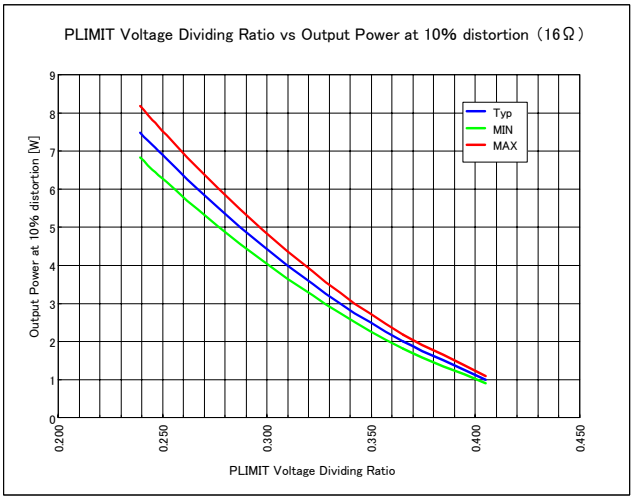
Enlarged Figures

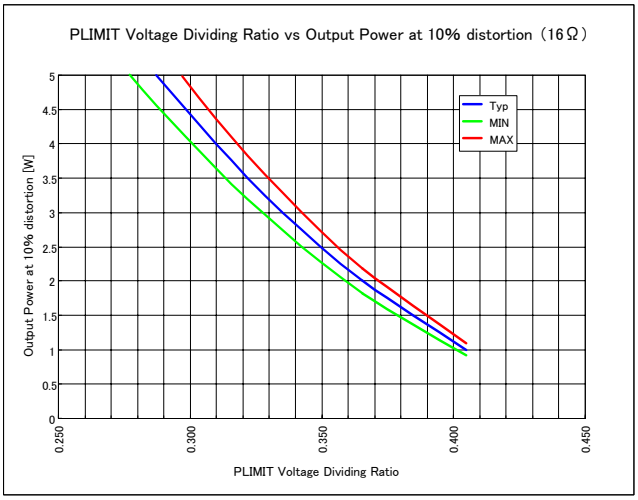












・Non-clip/DRC Function

This is the function to change the gain by detecting an input level to the PWM amplifier and to raise an average output level while suppressing clipping.

A mode is determined by the combination of NCDRC[1:0] terminals, as shown below.

NCDRC1	NCDRC0	Mode
L	L	Non-clip & DRC mode OFF
L	H	Non-clip mode
H	L	DRC1 mode
H	H	DRC2 mode

In Non-clip mode, the gain increases by 12dB. The gain is automatically adjusted so that an output peak voltage becomes a power limit value. The maximum attenuation is -12dB. Attack Time is 0 second. The release time from -12dB to 0dB is 7.7 s (typ.).

In DRC1 mode, the gain increases by 12dB. Dynamic Range Compression (a half of gain in dB) is performed within an output range of -12dB (-24dB for input range) from the power limit value. Attack Time is 0 s. The release time from -12dB to 0dB is 3.9 s (typ.).

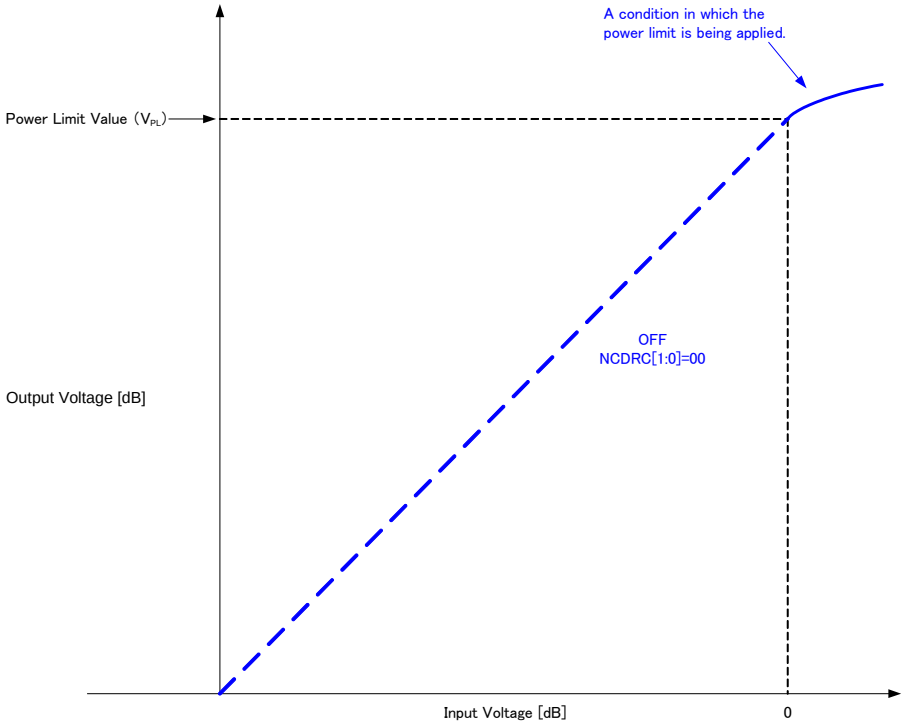
In DRC2 mode, the gain increases by 12dB. As with DRC1, similar compression is performed, but power-limit operation is not performed. PLIMIT terminal can be used to set a DRC operating point. Therefore, the setting of a gain curve is possible regardless of the maximum output power, and this allows for DRC operation from a low output power.

NCDRC [1:0] terminal should be switched under either of the following conditions.

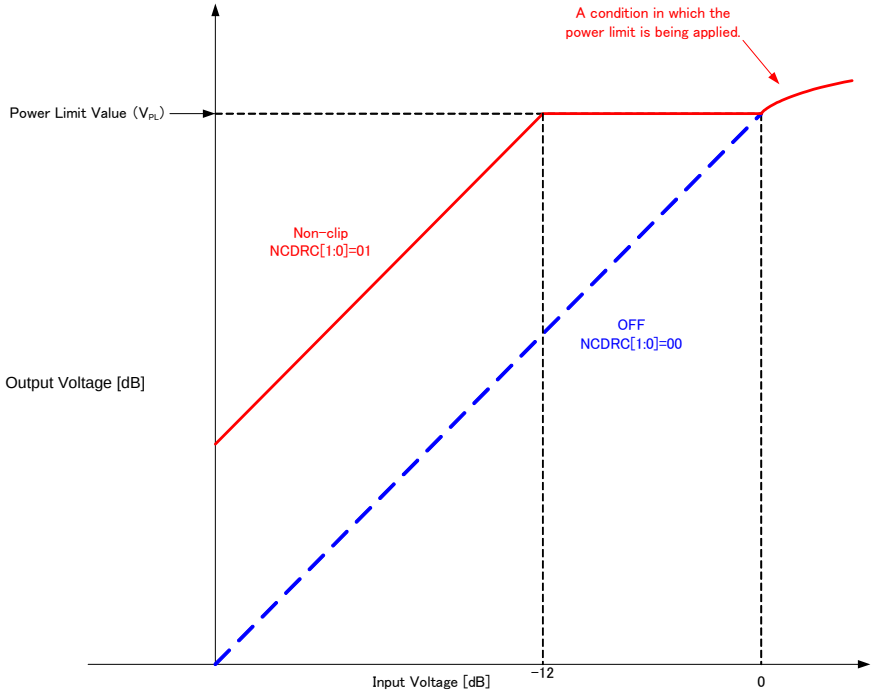
・Before PVDD power-on (lower than the PVDD start-up threshold voltage (V_{HUVLH}))

・SLEEPN=L

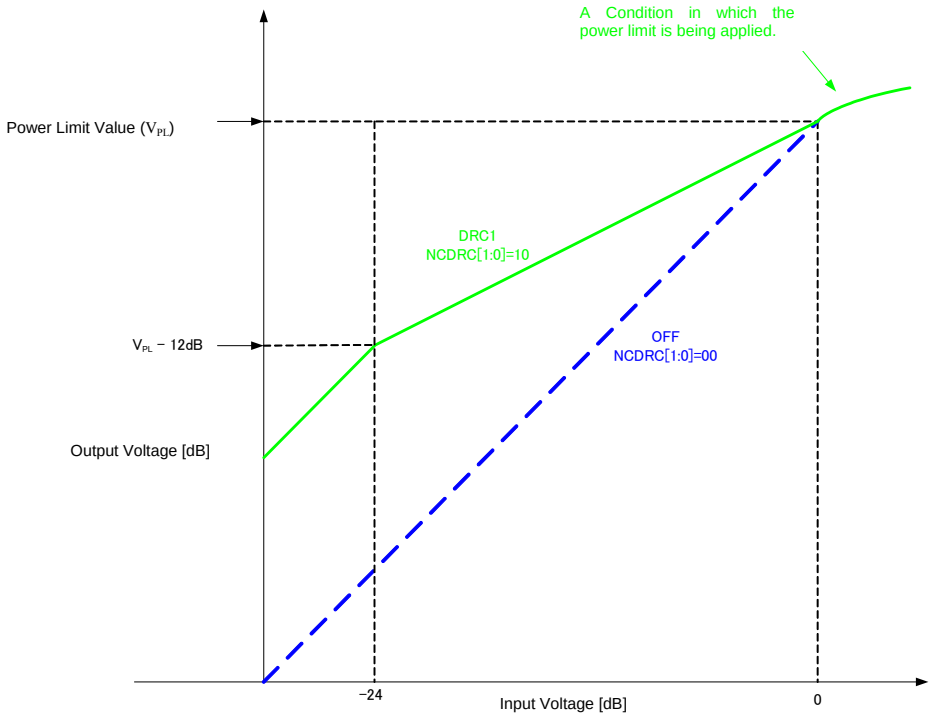
Pop noise may occur when switching it under an operating condition other than the above.



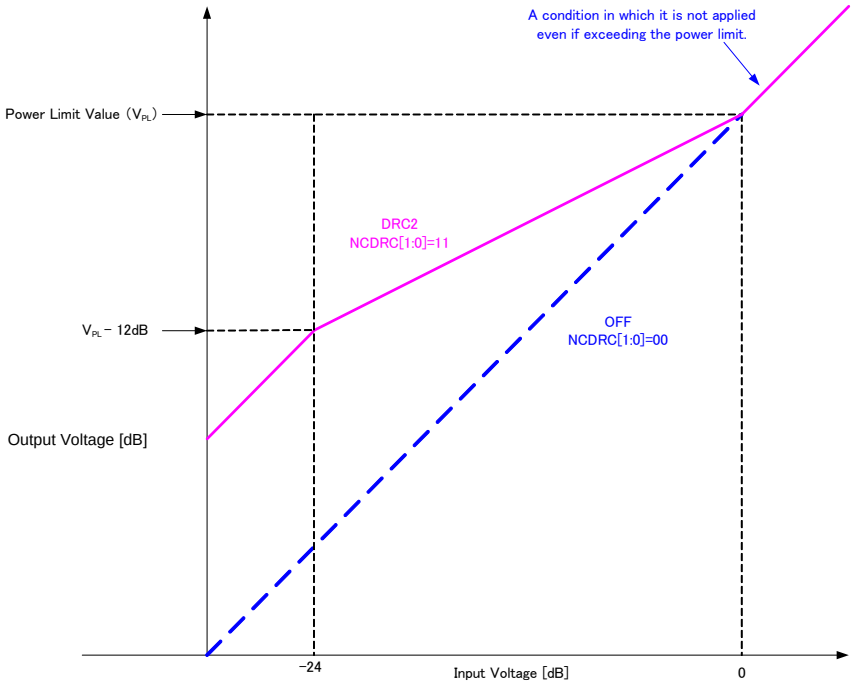
Non-clip/DRC Gain Curve (OFF)



Non-clip/DRC Gain Curve (Non-clip)



Non-clip/DRC Gain Curve (DRC1)



Non-clip/DRC Gain Curve (DRC2)

・Sleep Function

YDA146 shifts into sleep mode when SLEEPN terminal goes to "L" level.
In the sleep mode, all functions stop and consumption current is minimized (I_{SLEEP}).
When shifting into sleep mode during any protection mode, the protection mode is cancelled and PROTN terminal output becomes Hi-Z state.
The digital amplifier output becomes Weak Low (a state grounded through a high resistance).
AVDD and VREF outputs are pulled down.
When the level at SLEEPN terminal is changed from "L" to "H" under the condition that the voltage at PVDDREG terminal is higher than the threshold voltage (V_{HUVLH}) for low voltage malfunction prevention cancellation, the sleep mode is cancelled and the state shifts into the normal operation state after the period of sleep recovery time (t_{WU}).

・Mute Function

YDA146 shifts into mute mode when MUTEN terminal goes to "L" level.
In the mute mode, the digital amplifier output becomes Weak Low (a state grounded through a high resistance).
When the level at MUTEN terminal is changed from "L" to "H" under the condition that the voltage at PVDDREG terminal is higher than the threshold voltage (V_{HUVLH}) for low voltage malfunction prevention cancellation and state of SLEEPN terminal=H, the mute mode is cancelled and the state shifts into the normal operation state after the period of mute recovery time (t_{MRCV}).

・Clock Control Function

The setting of CKIN terminal controls the clock mode as shown below.

CKIN terminal Setting	Mode	CKOUT
L fixed	Internal Clock mode	Internal Clock (frequency: f_{CK}) output
H fixed	Internal Clock (Spread clock) mode	Internal Clock (Spread Clock) frequency: (f_{CK}) output
Clock input	External Clock mode	CKIN input buffer output (frequency: f_{CKIN})

When CKIN terminal is held L or H level, internal clock mode is selected to generate a clock internally.
And, when CKIN terminal is held H level, Spread Clock function operates to reduce EMI.
When an external clock is input to CKIN terminal, its frequency should be f_{CKIN}.
Do not use with CKIN terminal left open.

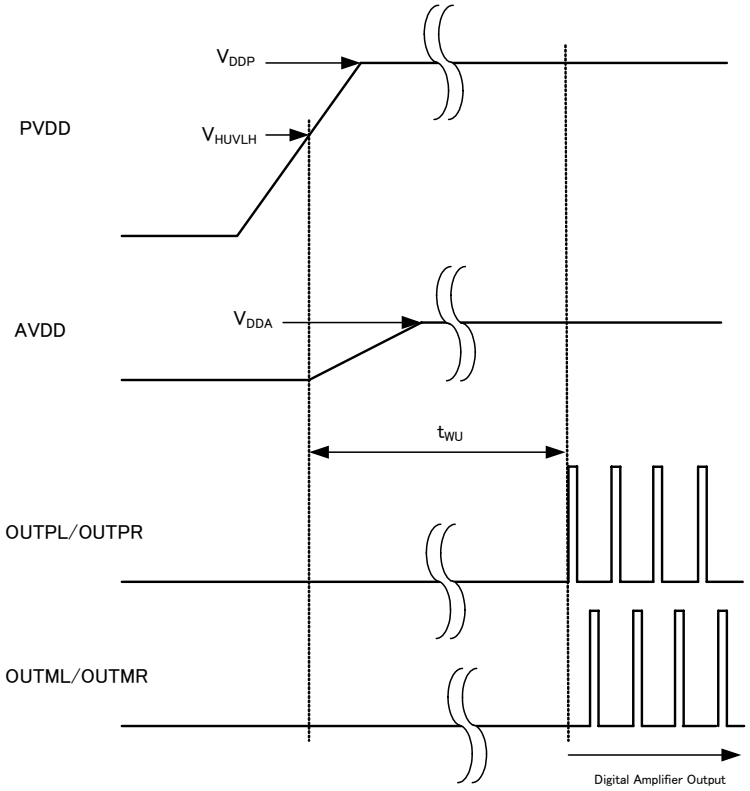
・Digital Amplifier Pop Noise Reduction Function

Pop noise that may occur at the power-on, power-off, power-down, and power-down cancel operations, etc. is reduced by minimizing an output offset voltage.

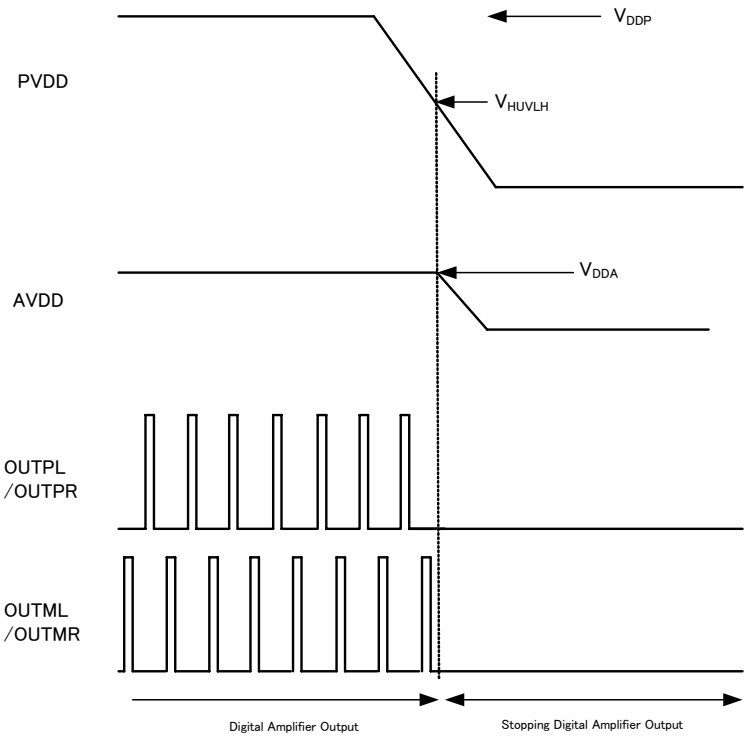
・Multi-chip Synchronization Function

The external clock synchronization function and clock output function are prepared and the use of master/slave configuration realizes carrier clock synchronization.
When using it with multi chips synchronized, one is used as a master chip and the other is used as a slave chip. At this time, connect CKOUT terminal of a master chip to CKIN terminal of a slave chip.
When using 3 chips (master/slave1/slave2), connect CKOUT terminal of a slave1 chip to CKIN terminal of a slave2 chip.
For details of connections, see "MASTER-SLAVE operation" (See page 24-25) in the "Examples of Application Circuits."
PVDD pins should be connected each other on a board.

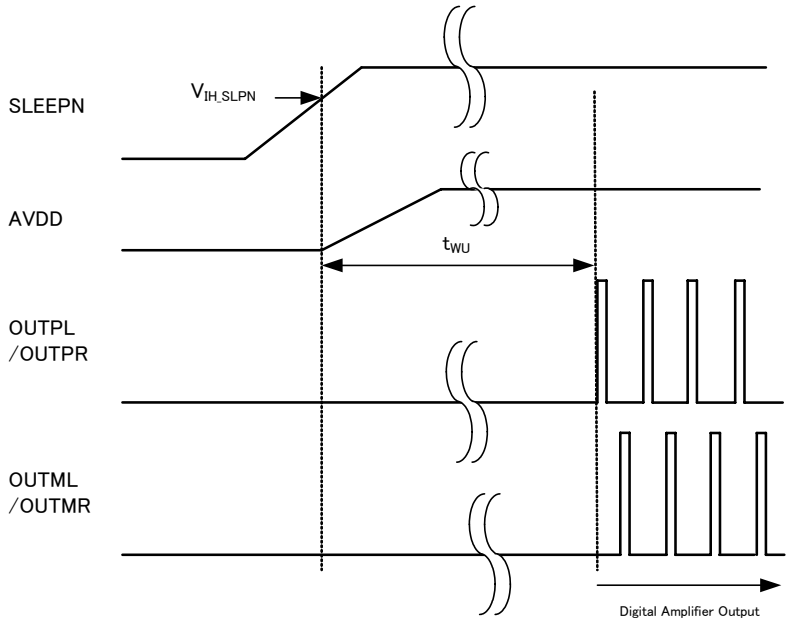
・Startup Sequence, Shutdown Sequence



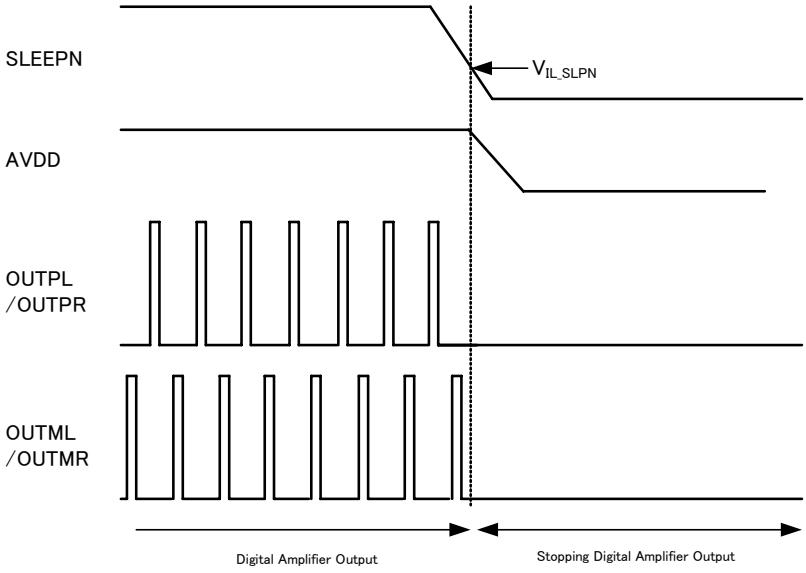
Power Supply Startup Sequence



Power Supply Shutdown Sequence



Startup Sequence from Sleep State



Transient Sequence to Sleep State

● Regulator Output

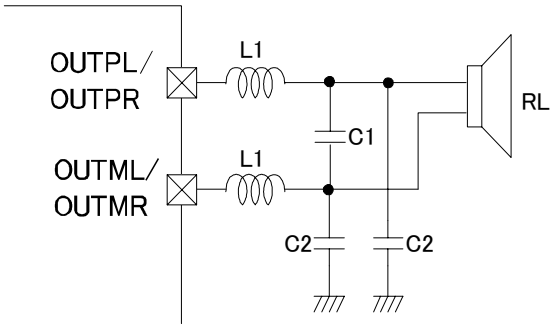
When SLEEPN terminal is at H, YDA146 outputs V_{DDA} to AVDD terminal. Connect a capacitor of 1μF to 4.7μF to AVDD terminal for stabilization. (0.8μF or more should be secured including its variation and temperature change.)
AVDD output must be used only for YDA146. If this output is used in a peripheral circuit of YDA146, the maximum current that can be driven will be I_{DDA}.

●LC Filter

YDA146 adopts the modulation method that reduces speaker loss sufficiently at mute state by the use of only an inductance the speaker has, and this allows for direct connection to a speaker without an LC filter.
When an LC filter is used, use the LC filter circuits shown below. At this time, the following constant should be used according to an impedance of a speaker. Using these constants makes a low-pass filter with a cut-off frequency of 50kHz or so, Q=0.7 or so.

LC filter constants:

RL	L1	C1	C2
4Ω	10μH	0.33μF	0.22μF
8Ω	22μH	0.22μF	0.1μF



LC Filter circuit

∗ With use of LC filters, if there is a possibility of not using a speaker, audio signals within 20kHz should be input.
And, if its band limitation is not possible, remove the speaker under the following conditions: SLEEPN terminal = L or MUTEN terminal = L, or PVDD = Power Off.

●Speaker Inductance

In the following cases, use a speaker with an inductance of 20μH or more (at around the switching frequency (f_{CKIN} or f_{CK})).
1. Direct connection of a speaker to an output pin of the digital amplifier without an LC filter.
2. Connection of a speaker to a position after components for EMI measures such as ferrite beads etc. (filterless).
With an inductance of less than 20μH, power loss in the speaker and this device may increase.

●Protection Function

YDA146 has the following four digital amplifier protection functions: overcurrent protection function, high temperature protection function, low voltage malfunction prevention function, and DC detection function.

Protection Functions	PROTN terminal Output	PROTN terminal Latch	Digital Amplifier Output State	Protection Mode Cancel
Over current Protection Function	Low	Latched	WL*1)	SLEEPN terminal=L or PVDD shutdown
High Temperature Protection Function (High Temp. power limiter state)	–	Not latched	Power Limit (-6dB)	SLEEPN terminal=L or PVDD shutdown or lower temperature
High Temperature Protection Function (High Temp. shutdown state)	Low	Not latched	WL*1)	SLEEPN terminal=L or PVDD shutdown or lower temperature
Low Voltage Malfunction Prevention Function	(HighZ)	–	WL*1)	–
DC Detection Function	Low	Latched	WL*1)	SLEEPN terminal=L or PVDD shutdown

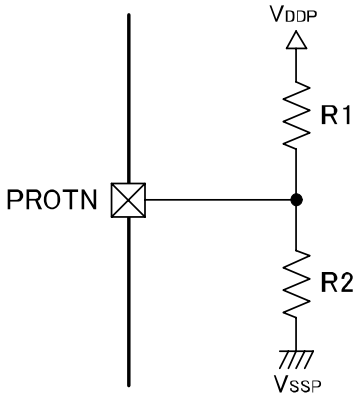
*1: WL=Weak Low (a state when grounded with a high resistance)

Use a circuit as shown below when pulling up PROTN terminal output externally.

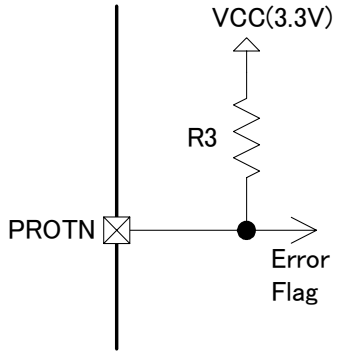
1) Pull up the terminal to a voltage obtained by dividing the voltage between PVDD and GND with voltage-dividing resistors.
   Find values with reference to the following formula so that a voltage at the terminal becomes 3.3V or less when PROTN terminal is in "H" output (Hi-Z).
   $2.0V \leqq (R2 / (R1 + R2)) \times V_{DDP} \leqq 3.3V$;however, R1 > 100kΩ, 10kΩ < R2 < 100kΩ

2) The pull-up should be performed to an external supply voltage lower than 3.3V. The pull-up resistor R3 should be a value as follows. 40kΩ < R3 < 200kΩ (47kΩ is recommended.)

In each case, select these values so that 0.4mA or more current will not flow into the terminal while PROTN terminal is in L state.



PROTN terminal Pull-Up Connection 1 (A pull-up to PVDD)



PROTN terminal Pull-Up Connection 2 (A pull-up to 3.3V)

* If automatic return setting is given by connecting PROTN terminal to SLEEPN terminal, use a separate power supply as VCC, not the same power supply as AVDD.
* When VCC is used as AVDD, see Startup Sequence (page 13 and 14).

・Digital Amplifier Over current Protection Function

This is the function to protect the device by detecting short-circuiting (to the supply voltage, to the ground, and between terminals) at digital amplifier output terminals.

In the protection mode, PROTN terminal becomes L level and output terminals become Weak Low state (a state grounded through a high resistance).

The protection mode can be cancelled by turning off the power supply or inputting an L level signal to SLEEPN terminal momentarily.

And, when PROTN terminal is externally connected to SLEEPN terminal, automatic return mode is selected. At this time, the protection mode is cancelled even if the protection mode is established by detecting an overcurrent state, and PROTN terminal output is turned from L level into Hi-Z state and a normal operation state is given after a given standby time (t_{WU}). (Automatic Return Function)

The current value to detect a short-circuiting between terminals is 8A (typ,V_{DDP}=12V), 10A (typ,V_{DDP}=15V).

・High Temperature Protection Function

This is the function to protect the device by detecting an unusual temperature in YDA146.

The protection mode operates in the following two modes according to the temperature.

1) High Temperature Power Limiter State

If the temperature rises and reaches 155°C (typ.), the high temperature power limiter state is given. This state decreases the power limit level by 6dB in order to limit the digital amplifier output power, and attempts to lower the temperature.

In this way, when the temperature falls and lowers than 130°C (typ.), the high temperature power limiter state is automatically cancelled and the gain is restored to the original setting value.

In the power limiter state, this does not affect on PROTN terminal.

2) High Temperature Shutdown State

If the temperature rises and reaches 165°C (typ.) during the high temperature power limiter state, the high temperature shutdown state is given. This state outputs an L level signal from PROTN terminal and digital amplifier output terminals become Weak Low state (a state grounded through a high resistance).

In this way, when the temperature goes down and lowers than 130°C (typ.), the high temperature shutdown state is automatically cancelled.

And, even if the shutdown state is established by detecting an unusual temperature, when PROTN terminal is externally connected to SLEEPN terminal, the shutdown state is cancelled and PROTN terminal output is turned from L into Hi-Z state and a normal operation state is given if the temperature is sufficiently lowered after a given standby time (t_{WU}). (Automatic Return Function)

If the temperature is not sufficiently lowered, the high temperature protection mode will be established.

・Low Voltage Malfunction Prevention Function

This is the function to protect the device when the supply voltage at PVDDREG terminal is unusually lowered.

In this protection mode, the digital amplifier output terminals become Weak Low state (a state grounded through a high resistance).

This protection mode is given if the supply voltage at PVDDREG terminal becomes a voltage lower than PVDD shutdown threshold voltage (V_{HUVLL}).

When the supply voltage at PVDDREG terminal exceeds PVDD startup threshold voltage (V_{HUVLH}), the protection mode is cancelled and a normal operation mode is given after a given standby time (t_{WU}). (Automatic Return Function)

・DC Detection Function

This is the function to protect the speaker connected to the digital amplifier output when a DC signal is continuously output from the digital amplifier.

When MUTEN terminal=L, the DC detection function is disabled.

When a voltage in excess of a given time (t_{DCDET}) and a given level (V_{DCDET}) is output to the digital amplifier output, the DC detection mode is given. This state outputs an L level signal from PROTN terminal and digital amplifier output terminals become Weak Low state (a state grounded through a high resistance).

Once the DC detection mode is given, an L level signal keeps outputting from PROTN terminal even if the DC output state is cancelled. The protection mode is cancelled by turning off the power supply or inputting an L level signal to SLEEPN terminal momentarily.

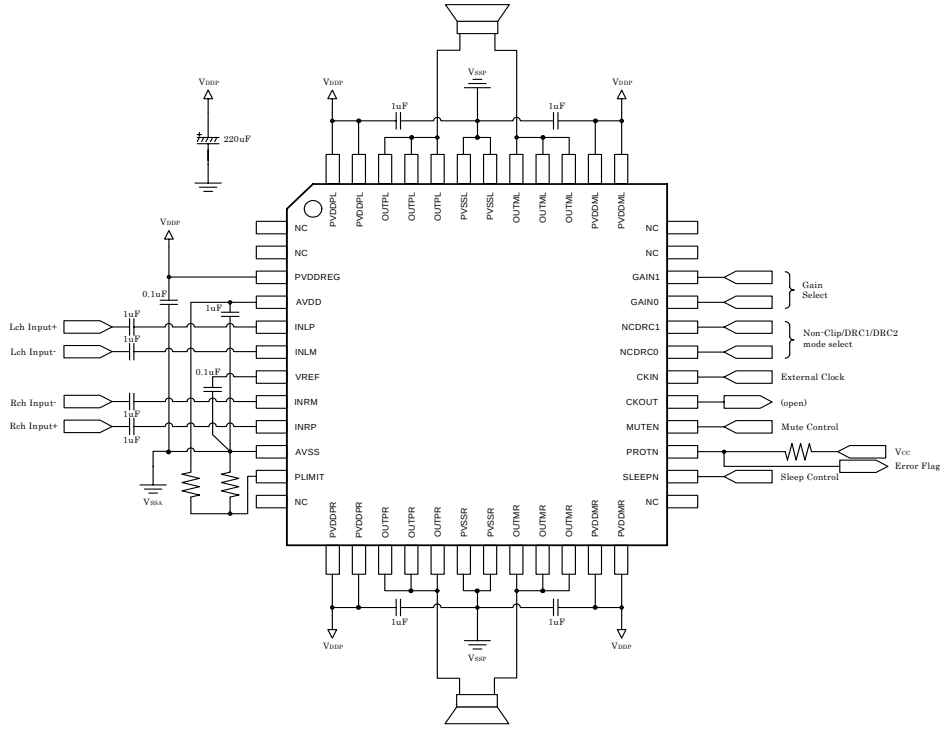
And, even if DC protection mode is established by detecting a DC signal, when PROTN terminal is externally connected to SLEEPN terminal, the protection mode is cancelled and PROTN terminal output is turned from L into Hi-Z state and a normal operation state is given after a given standby time (t_{WU}).

■Examples of Application Circuits

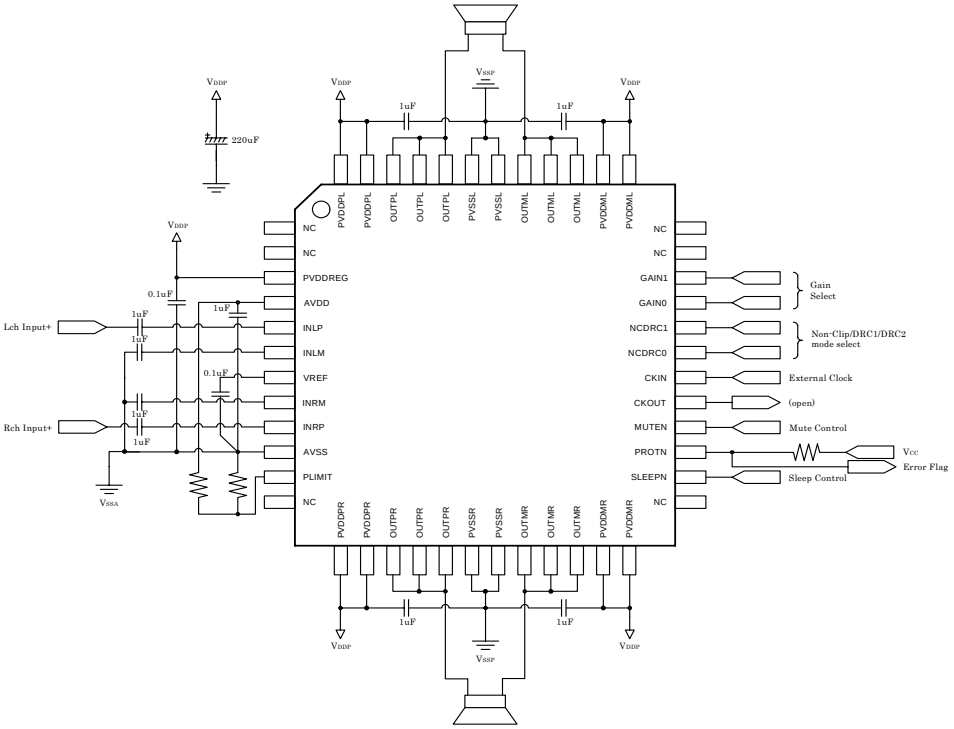
(Caution)

- A ceramic capacitor of 1µF should be used as a bypass capacitor between the following terminals: PVDDPL-PVSSL, PVDDML-PVSSL, PVDDPR-PVSSR, and PVDDMR-PVSSR. Please mount the capacitor as close as possible to each terminal.
- A former-stage impedance of input terminals should be 10kΩ or less.
- Select resistor values so that a voltage becomes 2.0V to 3.3V when PROTN terminal is at H level and current becomes 0.4mA or less when PROTN terminal is at L.
- For PLIMIT terminal setting, see page 6 and 7.
- For a pull-up resistor for PROTN terminal, see page 16 and 17.

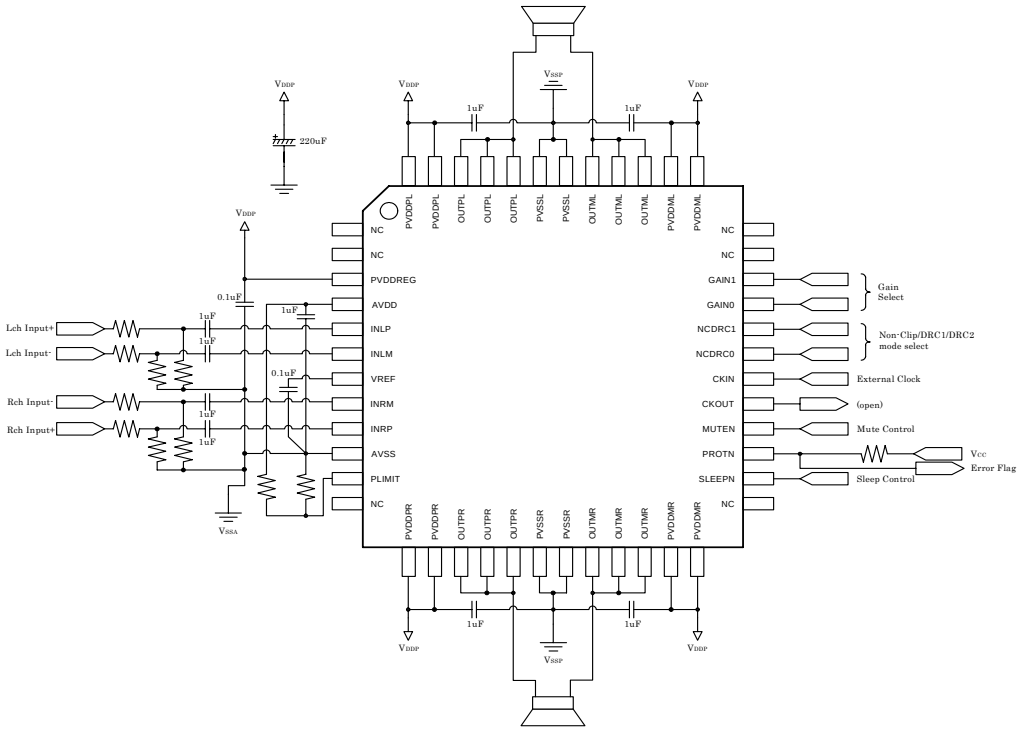
Single operation in stereo mode (differential-input, external clock operation)



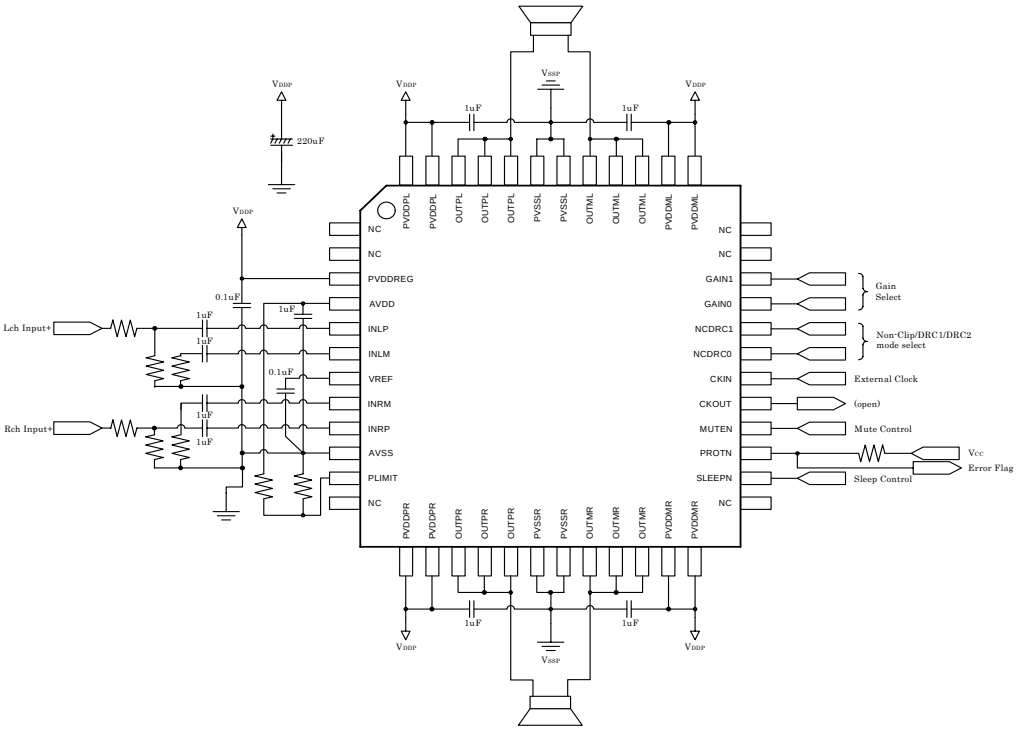
Single operation in stereo mode (single-ended input, external clock operation)



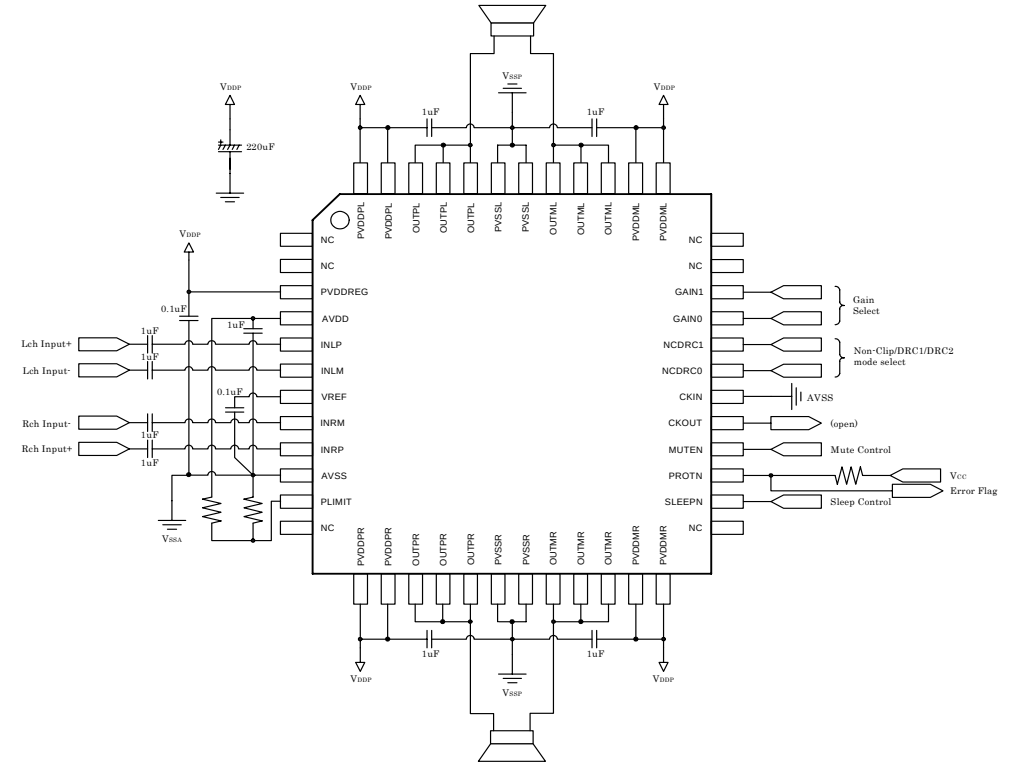
Single operation in stereo mode (differential-input, input signal level (externally set), external clock operation)



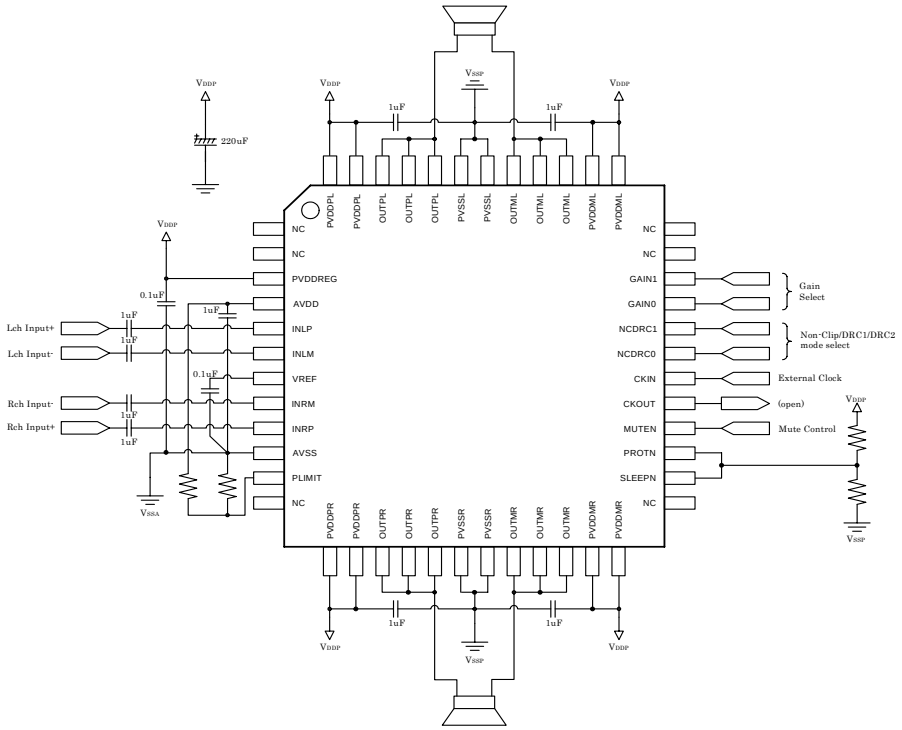
Single operation in stereo mode (single-ended input, input signal level (externally set), external clock operation)



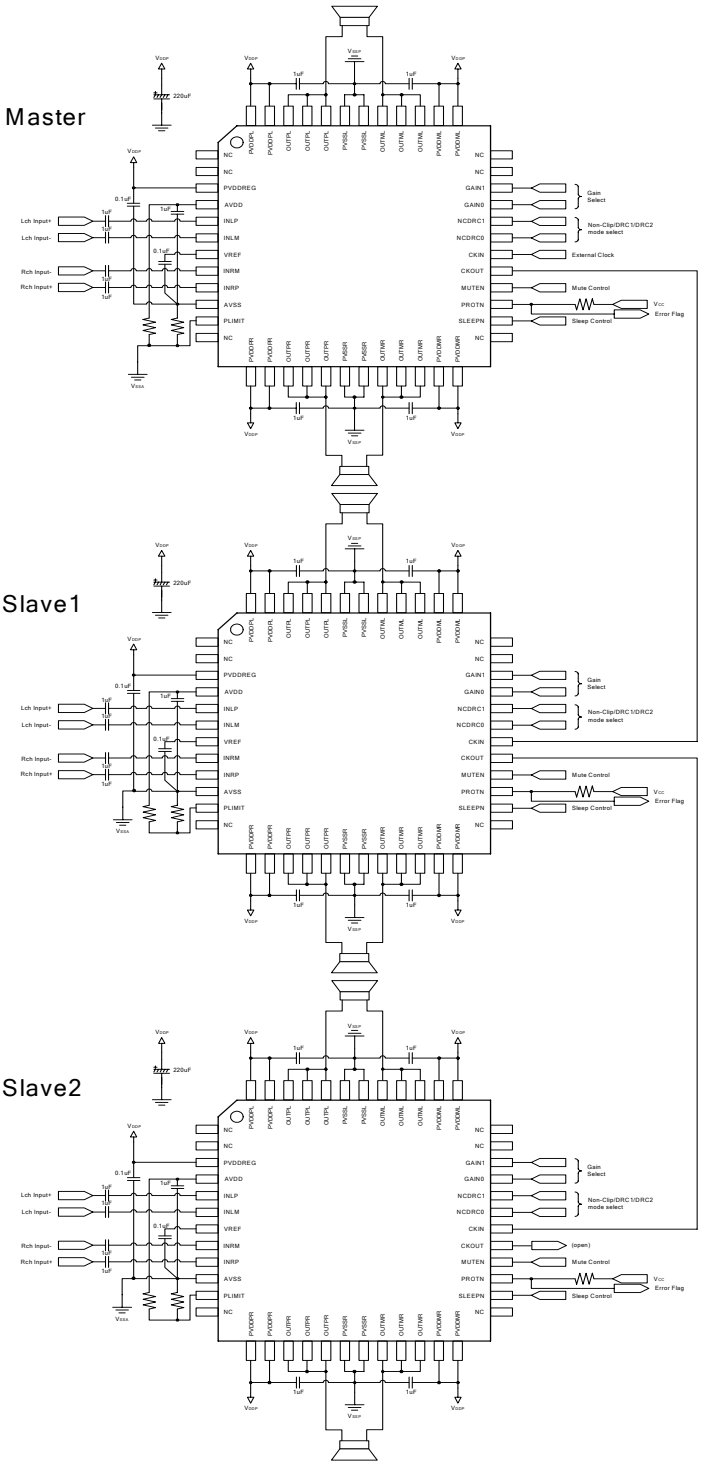
Single operation in stereo mode (differential-input, internal clock operation)



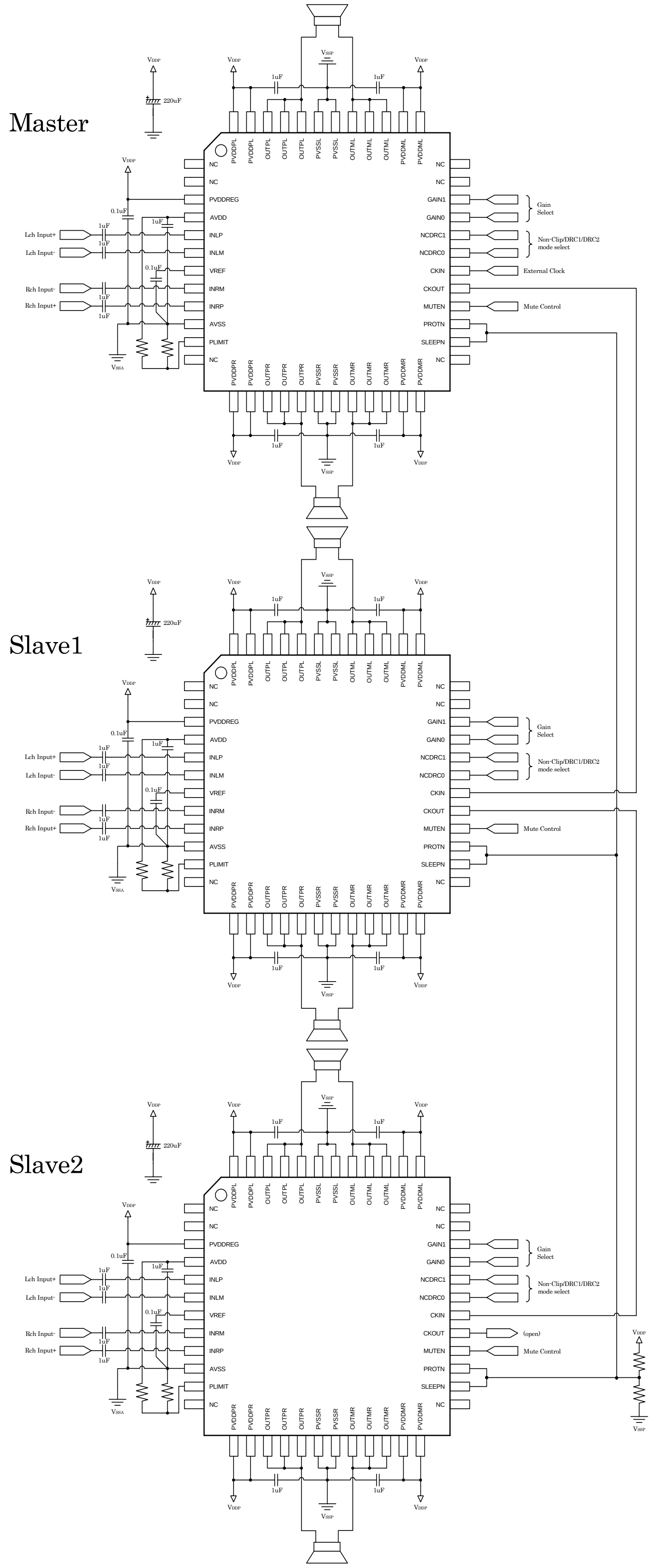
Single operation in stereo mode (differential-input, external clock operation, automatic return setting)



MASTER-SLAVE operation (differential-input, external clock operation)



MASTER-SLAVE operation (differential-input, external clock operation, automatic return setting)



■Electrical Characteristics

●Absolute Maximum Ratings *1)

Parameter			Symbol	Min.	Max.	Unit
Power Supply terminal (PVDD) Voltage Range			V_{DDP}	-0.3	20	V
Input Terminal Voltage Range			V_{IN}	-0.3	4	V
PROTN Terminal Voltage Range			V_{PROTN}	-0.3	4	V
SQFP48	4 layers	Power Dissipation (Ta=25°C)	P_{D25}		6.5 *2)	W
		Power Dissipation (Ta=70°C)	P_{D70}		4.21 *2)	W
		Power Dissipation (Ta=85°C)	P_{D85}		3.4 *2)	W
	2 layers	Power Dissipation (Ta=25°C)	P_{D25}		3.72 *3)	W
		Power Dissipation (Ta=70°C)	P_{D70}		2.38 *3)	W
		Power Dissipation (Ta=85°C)	P_{D85}		1.93 *3)	W
Junction Temperature			T_{JMAX}		150	°C
Storage Temperature			T_{STG}	-40	150	°C

Note) *1: Absolute Maximum Ratings is values which must not be exceeded to guarantee device reliability and life, and when using a device in excess even a moment, it may immediately cause damage to device or may significantly deteriorate its reliability.

*2: A value based on the following implementation conditions:
LC Filter : L=22 [µH]/C=0.47[µH], Board Layer : 4 layers(FR-4), Board Size : 136 [mm] × 85 [mm],
Board Copper Foil Thickness : 35 [µm], Wiring Density : 379%, Device Heat Pad : soldering on the board
Through Hole for heat dissipation : 25 (5×5) holes from a point just below the exposed stage to the inner layer (VSS) and B layer.

*3: A value based on the following implementation conditions:
Board Layer: 2 layers (FR-4), Board Size: 136 [mm] × 85 [mm], Board Copper Foil Thickness: 35 [µm],
Wiring Density: 187%, Exposed stage: soldering on the board
Through Hole for heat radiation: 25 (5×5) holes from a point just below the exposed stage to B layer.

●Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (PVDD)	V_{DDP}	8	-	16.5	V
Digital terminals *4) H level input voltage	V_{IN}	2.52	3.3	3.6	V
SLEEPN terminal H level input voltage	V_{IN}	2.0	3.3	3.6	V
Operating Ambient Temperature	T_a	-40	25	85	°C
Speaker Impedance	R_L	3.6	4	-	Ω

Note) *4:MUTEN, CKIN, NCDRC0, NCDRC1, GAIN0, GAIN1(CMOS I/F) terminals

●DC Characteristics (V_{SS}=0V, V_{DDP}=8V to 16.5V, Ta=-40°C to 85°C, CKIN=1MHz, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PVDD Startup threshold voltage	V_{HUVLH}	-	-	6.5	-	V
PVDD Shutdown threshold voltage	V_{HUVLL}	-	-	6.0	-	V
DC Detection Voltage	V_{DCDET}	PVDD=15V	-	4	-	V
DC Detection Time	t_{DCDET}	-	-	0.5	-	s
Digital terminal*5) H level input voltage	V_{IH}	-	2.52	-	-	V
Digital terminal*5) L level input voltage	V_{IL}	-	-	-	0.9	V
Digital terminal*5) Input Impedance	R_{IN_D}	-	3.3	-	-	MΩ
SLEEPN terminal H level input voltage	V_{IH_SLPN}	-	2.0	-	-	V
SLEEPN terminal L level input voltage	V_{IL_SLPN}	-	-	-	0.8	V
SLEEPN terminal Input Impedance	R_{IN_SLPN}	-	3.3	-	-	MΩ
CKOUT Output Voltage	V_{OL}	I_{OL}=4mA	-	-	0.4	V
CKOUT Output Voltage	V_{OH}	I_{OH}=-4mA	2.4	-	-	V
PROTN Output Voltage	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V
INLP, INLM, INRP, INRM terminals Input impedance	R_{IN}	-	-	18.8	-	kΩ
AVDD Output Voltage	V_{DDA}		3.0	3.3	3.6	V
AVDD Output Current	I_{DDA}		-	-	1	mA
VREF Output Voltage	V_{REF}		-	V_{DDA} /2	-	V
PVDD Consumption Current	I_{DDP}	V_{DDP}=12V, no-load	-	32	-	mA
PVDD consumption current during power-down mode (SLEEPN=L)	I_{SLEEP}	V_{DDP}=15V, Ta=25°C	-	30	-	μA
PVDD consumption current during Mute state (MUTEN=L)	I_{MUTE}	V_{DDP}=15V, Ta=25°C	-	16	-	mA
PVDD consumption current during no signal input	I_{NOSIG}	V_{DDP}=15V, Ta=25°C	-	38	-	mA

Note) *5: This value is applicable to MUTEN, CKIN, NCDRC0, NCDRC1, GAIN0, and GAIN1 (CMOS I/F) terminals.

●AC characteristics (V_{SS}=0V, V_{DDP}=8V to 16.5V, Ta=-40°C to 85°C, CKIN=1MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CKIN Input Frequency	f_{CKIN}	0.9	1,0	1.1	MHz
CKIN Input Duty	DT_{CKEXT}	40	-	60	%
Self-excited Clock Frequency	f_{CK}	-	1.0	-	MHz
Sleep Recovery Time	t_{WU}	-	1	1.5	s
Mute Recovery Time	t_{MRCV}	-	-	1	ms

●Analog Characteristics

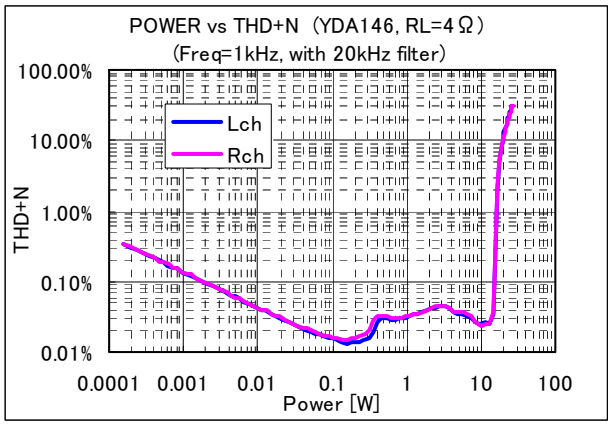
(V_{SS}=0V, V_{DDP}=12V, Ta=25°C, GAIN[1:0]=L,L, NCDRC[1:0]=L,L, CKIN= L[*7)], unless otherwise specified.)

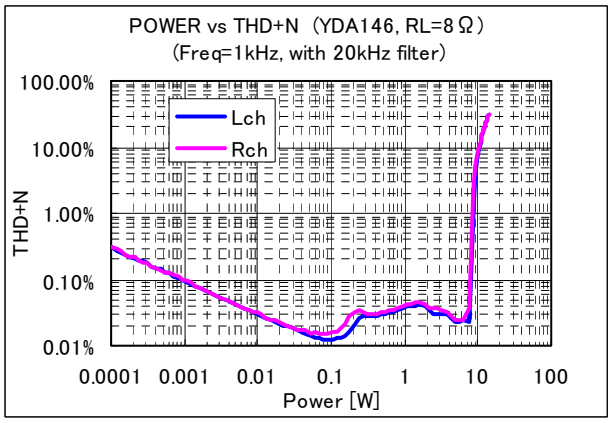
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum momentary Output	Po	R_L=4Ω, V_{DDP}=12V, THD+N=10%		19.4		W
		R_L=8Ω, V_{DDP}=15V, THD+N=10%		15		W
		R_L=4Ω, V_{DDP}=15V, THD+N=10%		30		W
Voltage Gain	A_V	GAIN[1:0]=L,L		22		dB
		GAIN[1:0]=L,H		28		dB
		GAIN[1:0]=H,L		34		dB
		GAIN[1:0]=H,H		16		dB
Total Harmonic Distortion Rate (BW::20kHz)	THD+N	V_{DDP}=15V, R_L=4Ω, P_O=0.2W		0.02		%
		V_{DDP}=12V, R_L=8Ω, P_O=0.2W		0.02		%
Signal /Noise Ratio (BW::20kHz A-Filter)	SNR	R_L=4Ω,GAIN[1:0]=H,H		105		dB
Residual Noise (BW::20kHz A-Filter)	Vn	R_L=4Ω,GAIN[1:0]=H,H		48		μVrms
Channel Separation Ratio	CS	1kHz		80		dB
Power Supply Rejection Ratio (PVDD applied)	PSRR	Vripple=100mV, f=1kHz		60		dB
Common Mode Rejection Ratio	CMRR	f=1kHz		41		dB
Maximum Efficiency	η	V_{DDP}=15V, R_L=4Ω		90		%
		V_{DDP}=15V, R_L=8Ω		92		%
Output Offset Voltage [*6)]	|Vo|			5	15	mV
Frequency characteristics	f_{RES}	f=20Hz	-1	0	1	dB
		f=20kHz	-1	0	1	dB

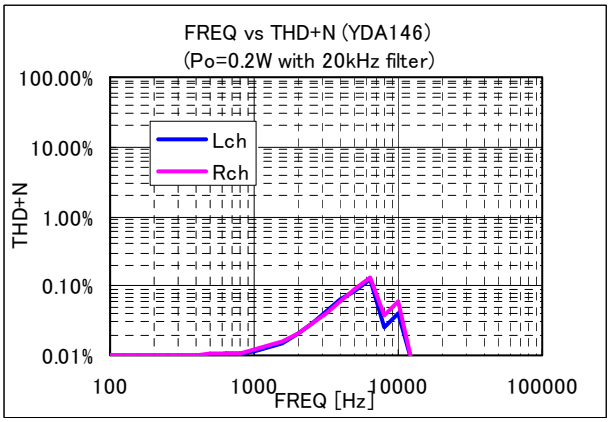
Note) *6: The offset voltage is denoted by considering a typical value and the maximum value as σ and 3σ, respectively.
*7: The same specification is applied to the external clock mode and internal clock (spread clock mode).
All the values of analog characteristics were obtained in our evaluation circumstance.
Depending upon pattern layout etc., characteristics may vary.
The measurement is performed with an 8Ω or 4Ω resistor connected in series with a 30μH coil as an output load.

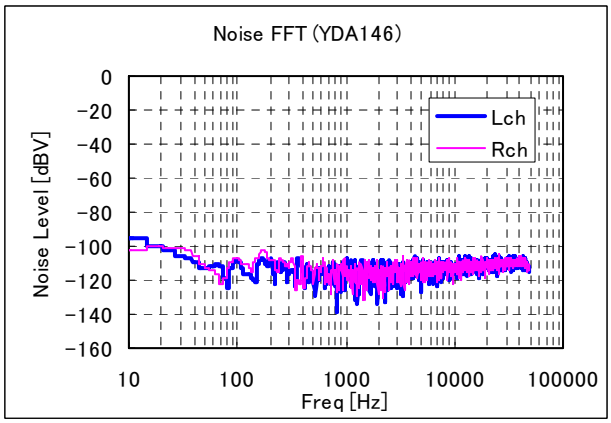
●Example of typical characteristics

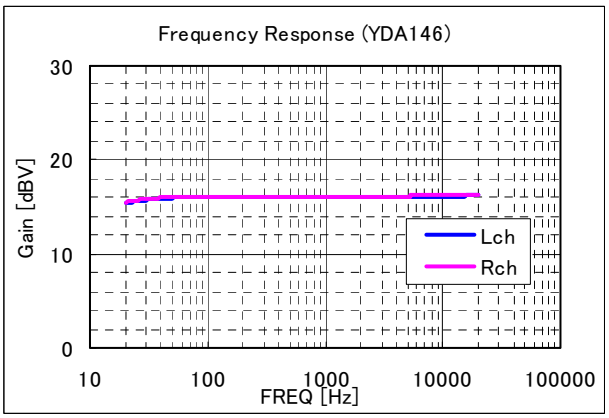
(V_{SS}=0V, V_{DDP}=12V, Ta=25°C, GAIN[1:0]=L,L, NCDRC[1:0]=L,L, CKIN=1MHz, unless otherwise specified)

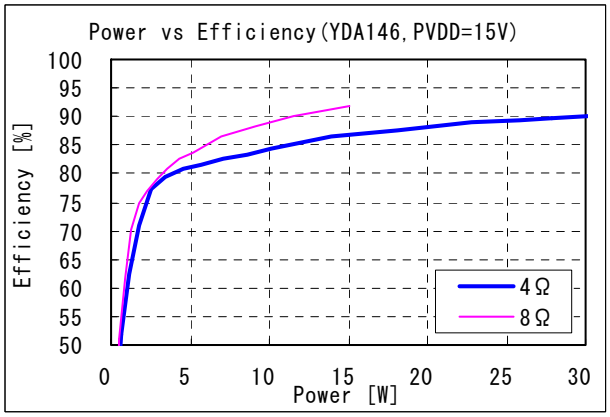


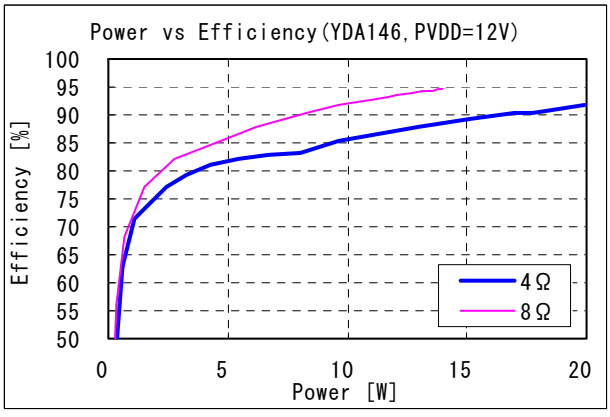


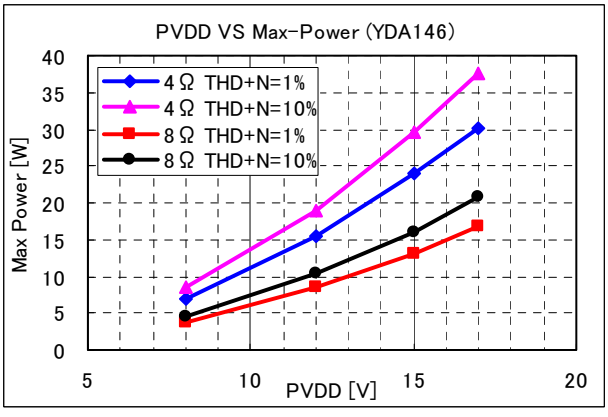


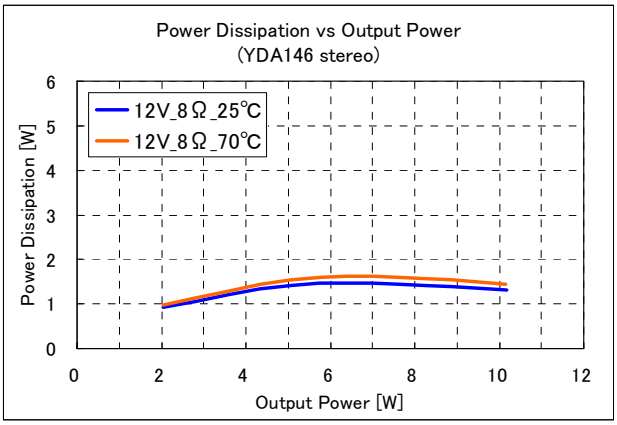


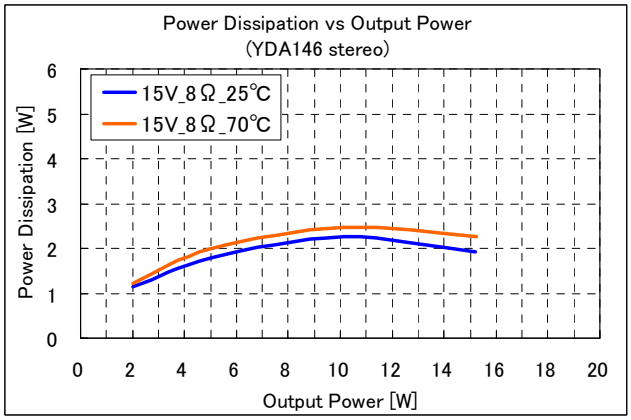


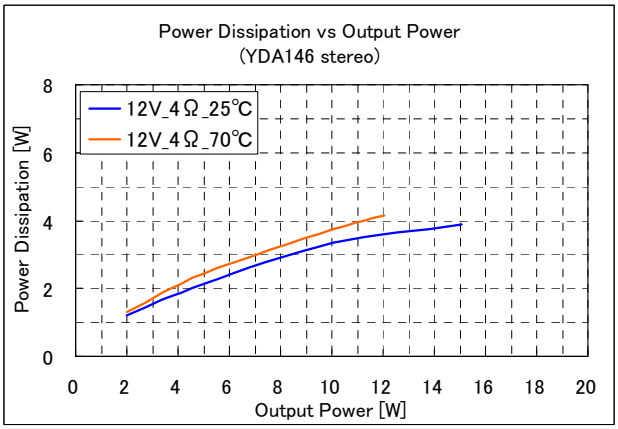


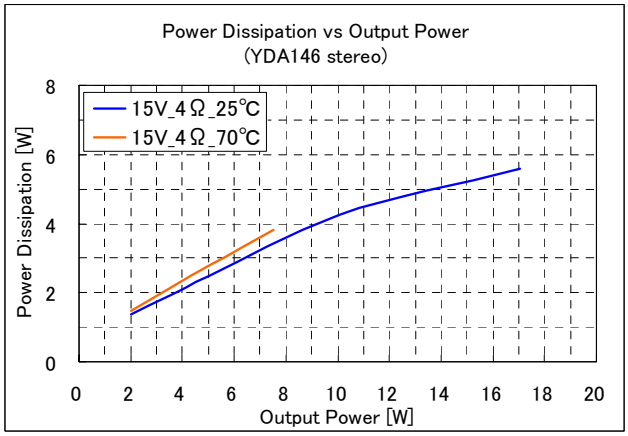






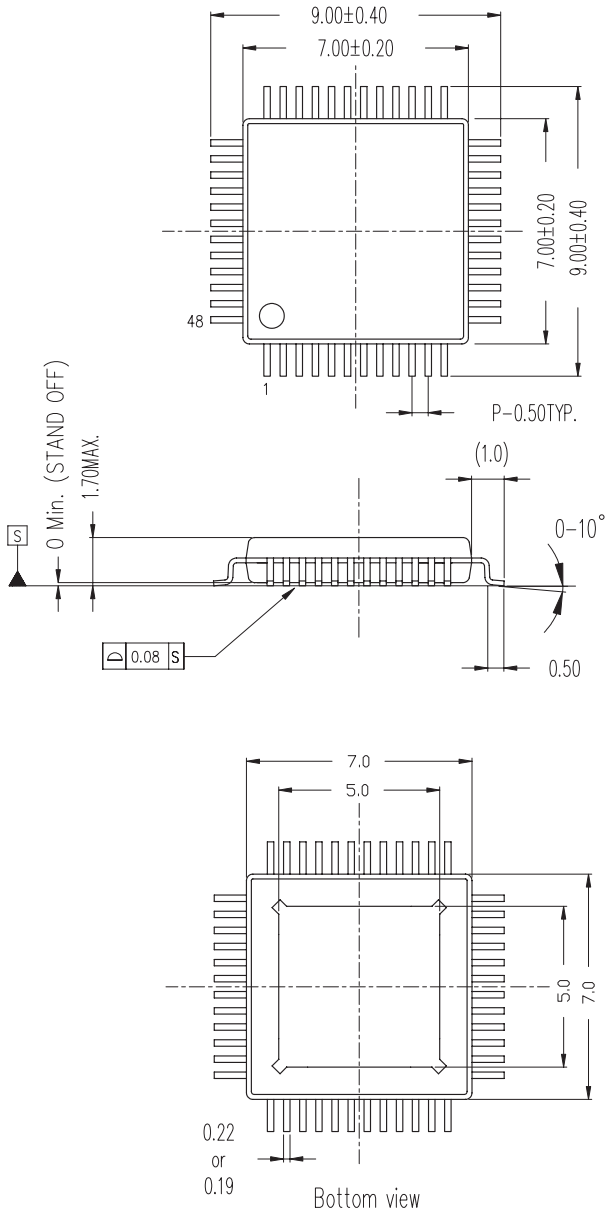






■Package Outline

C-PK48SP1-3



端子厚さ/Lead Thickness : 0.15 or 0.17

モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位 : mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

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7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

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