SINO WEALTH

SH67K93

24K 4-bit Micro-Controller with LCD Driver

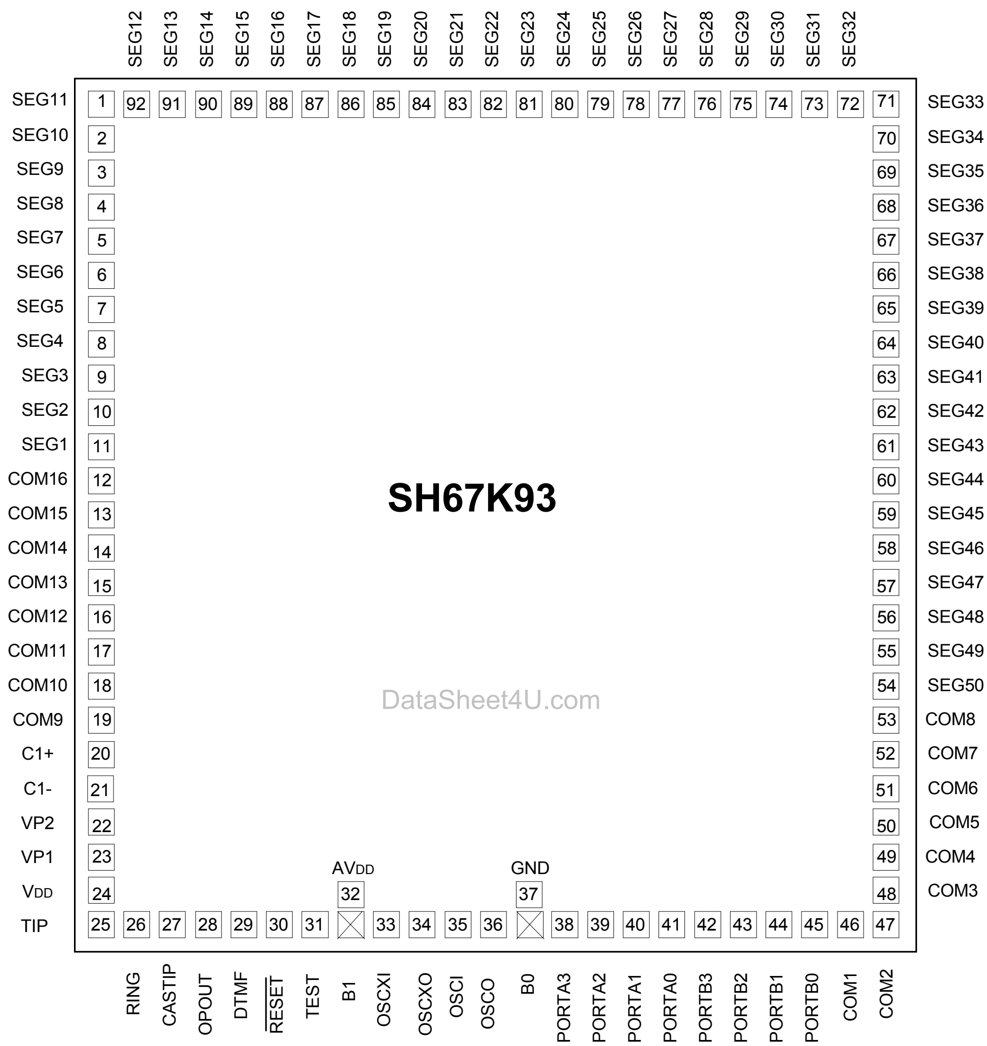
Feature

- SH6610D-Based Single-Chip 4-bit Micro-Controller
- ROM: 24K X 16 bits
- RAM: 5784 X 4 bits
  - 48 bytes System Control Register
  - 5536 bytes Data Memory
  - 200 bytes LCD RAM
- Operation Voltage: 2.4V - 3.6V
- 23 CMOS Bi-directional I/O pads (15 shared with LCD Segments)
- 12 Segments of LCD Shared with Scan Output port
- 8-Level Stack (including interrupts)
- Two 8-bit Timer/Counter
- Powerful Interrupt Sources
  - External Interrupt (PORTA.0 Rising/Falling edge)
  - Timer0 Interrupt
  - Timer1 Interrupt
  - External Interrupts: PORTB, PORTC and PORTD (Falling edge)
- LCD Driver
  - 50 Seg X 16 Com (1/16 duty 1/4 bias or 1/5 bias)
  - 50 Seg X 8 Com (1/8 duty 1/4 bias or 1/5 bias)
- Oscillator (Code Option)
  OSC
  - Crystal Oscillator 32.768kHz
  - RC Oscillator: 262kHz
  OSCX
  - Ceramic Resonator 3.58MHz/Crystal Oscillator 3.579545MHz
  - RC oscillator 1.8MHz
- Instruction Cycle Time
  - 122.07μs for 32.768kHz crystal
  - 15.27μs for 262 kHz RC
  - 2.22μs for 1.8 MHz RC
  - 1.1μs for 3.58MHz ceramic
- Two Low Power Operation Modes: HALT and STOP
- Warm-up Timer for Power-On Reset (POR)
- Watchdog Timer
- DTMF/FSK Generator
- Available In CHIP FORM

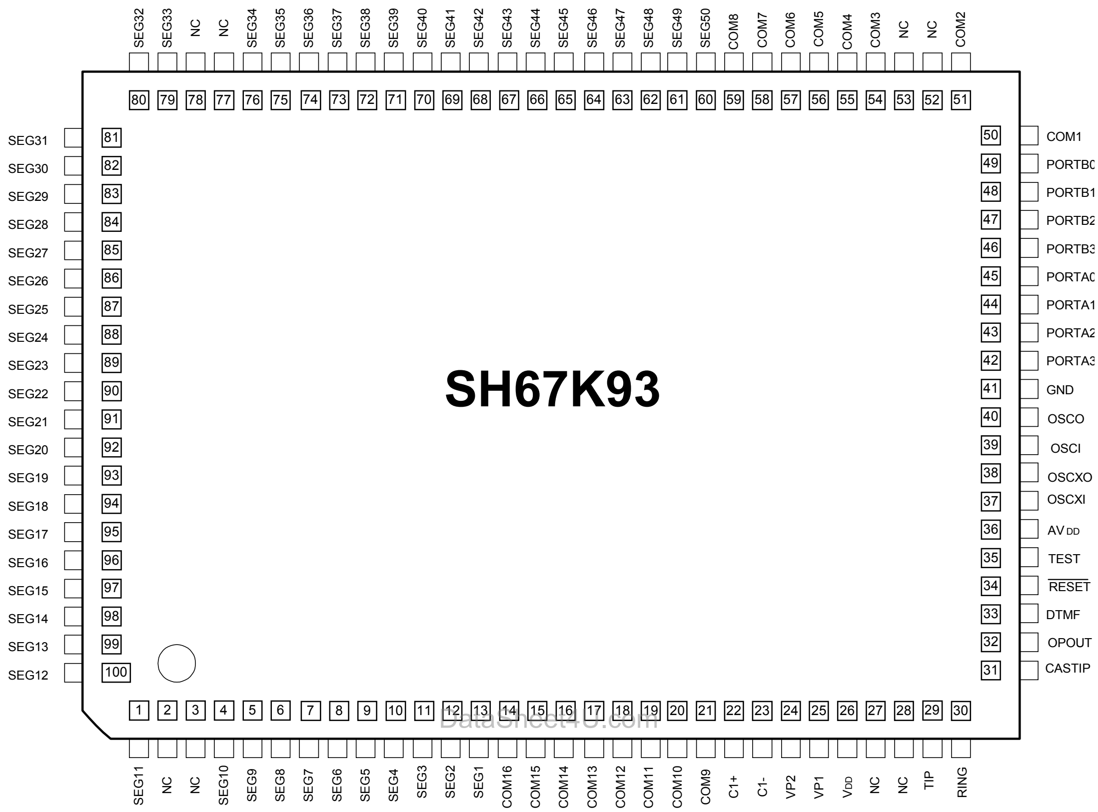
General Description

SH67K93 is a single-chip 4-bit micro-controller. The device integrates a SH6610D CPU core, RAM, ROM, Timer, LCD driver, I/O port, DTMF/FSK Generator and FSK/DTMF/CAS decoder. This chip builds in a dual-oscillator to enhance the total chip performance. The device is suitable for TypeI/II CID cord phone.

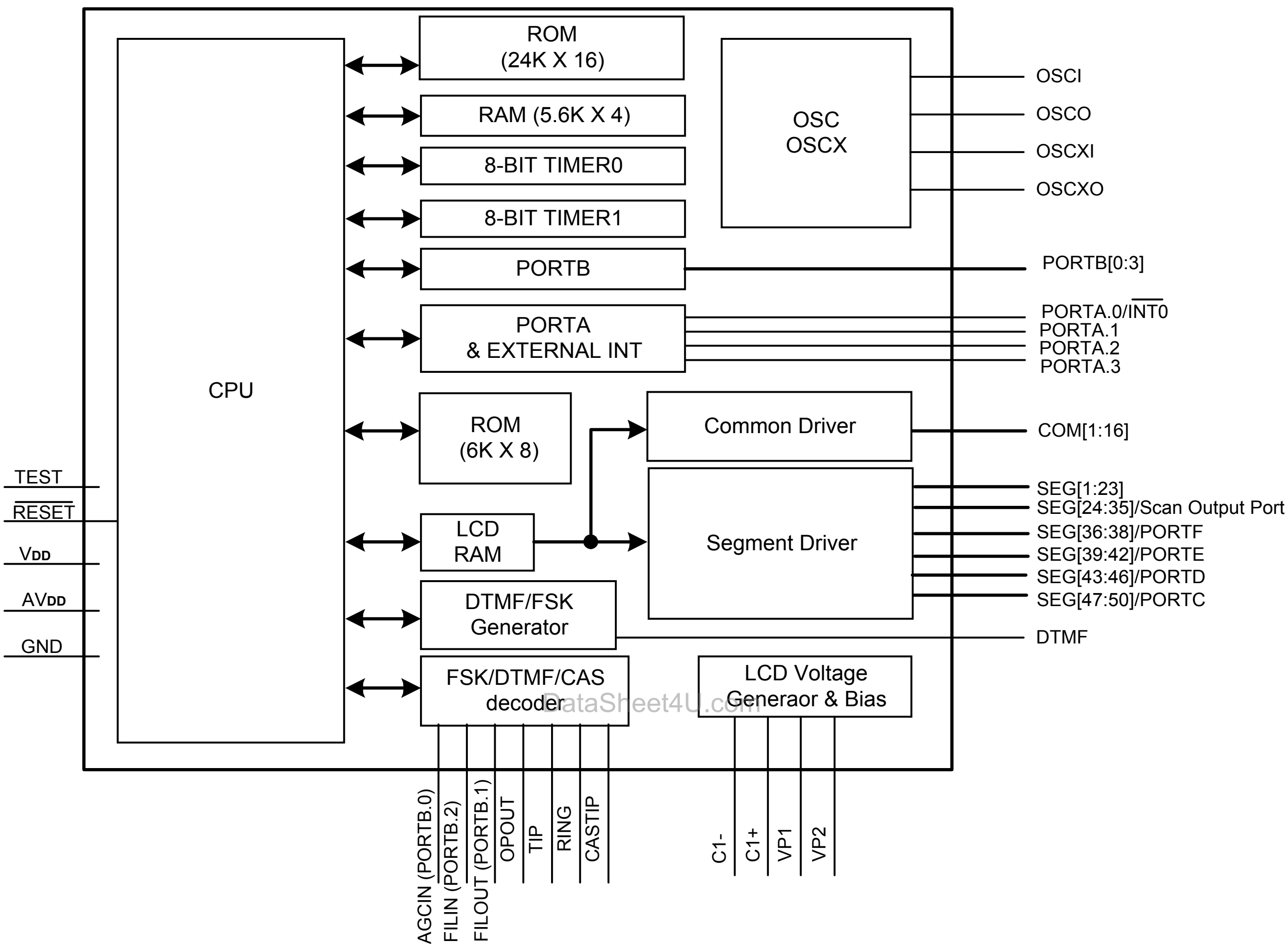
Pad Configuration



Pin Configuration



Block Diagram



Pad Description (Total 92 pads)

Pad No.	Pin No. (QFP100)	Designation	I/O	Description
24	26	V_{DD}	P	Digital Power supply
32	36	AV_{DD}	P	Analog Power supply
37	41	GND	P	Ground pad
30	34	$\overline{RESET}$	I	Reset pad (internal floating, connection for user)
31	35	TEST	I	Test Pad, internal pull-low (no connection for user)
36	40	OSCO	O	Low Oscillator output pad (32.768kHz crystal or 262kHz RC)
35	39	OSCI	I	Low Oscillator input pad (32.768kHz crystal or 262kHz RC)
34	38	OSCXO	O	High Oscillator output pad (3.58MHz ceramic/3.579545MHz crystal or 1.8MHz RC)
33	37	OSCXI	I	High Oscillator input pad (3.58MHz ceramic/3.579545MHz crystal or 1.8MHz RC)
38 - 41	42 - 45	PORTA3 - 0	I/O	Bit programmable I/O PORTA.0 shared with $\overline{INT0}$ PORTA.3 had powerful sink capacity to driver LED directly
42 - 45	46 - 49	PORTB.3 PORTB.2/ FILIN PORTB.1/ FILOUT PORTB.0/ AGCIN	I/O	Bit programmable I/O, Vector interrupt ($\overline{INT1}$) For the caller ID application: PORTB.2 is shared with FILIN input pad PORTB.1 is shared with FILOUT output pad PORTB.0 is shared with AGCIN input pad When PORTB0 - 2 are shared, the interrupt function for PORTB0 - 3 are disable and the pull-high resistor setting for PORTB0 - 2 are disable
54 - 57	60 - 63	PORTC3 - 0 /Segment50 - 47	I/O	Bit programmable I/O, Vector interrupt ($\overline{INT1}$) Segment50 - 47 shared with PORTC
58 - 61	64 - 67	PORTD3 - 0 /Segment46 - 43	I/O	Bit programmable I/O, Vector interrupt ($\overline{INT1}$) Segment46 - 43 shared with PORTD
62 - 65	68 - 71	PORTE3 - 0 /Segment42 - 39	I/O	Bit programmable I/O Segment42 - 39 shared with PORTE
66 - 68	72 - 74	PORTF2 - 0 /Segment38 - 36	I/O	Bit programmable I/O Segment38 - 36 shared with PORTF
69 - 80	75 - 76 79 - 88	Segment35 - 24	O	Segment signal for LCD display/scan output port
81 - 11	89 - 1 3 - 13	Segment23 - 1	O	Segment signal output for LCD display
46 - 53 19 - 12	50 - 51, 54 - 59, 21 - 14	COM1 - COM16	O	Common signal output for LCD display
20, 21, 23, 22	22, 23, 25, 24	C1+, C1-, VP1, VP2	I	Connect with external components of LCD power
25, 26	29, 30	TIP, RING	I	Connected with TIP side & Ring side for twisted pair
29	33	DTMF/FSK	O	The output pad of DTMF/FSK Generator
27	31	CASTIP	I	CAS tone input pad
28	32	OPOUT	O	Pre-amplifier output

Functional Descriptions

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:
Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can only address 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations, provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that generates the arithmetic operation. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceed 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT status.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O:	\$000 - \$02F
Data memory:	\$030 - \$2FF
	\$3C8 - \$3FF
	\$430 - \$7FF
	\$830 - \$BFF
	\$C30 - \$FFF
	\$1030 - \$13FF
	\$1430 - \$1787
	(Total 5536 X 4 bits)
Reserved:	\$5D0- \$5FF
LCD RAM space:	\$300 - \$3C7(200 X 4 bits)

RAM Mapping

\$000 - \$02F	System Register
\$400 - \$42F	
\$800 - \$82F	
\$C00 - \$C2F	
\$1000 - \$102F	
\$1400 - \$142F	
\$030 - \$2FF	Data Memory
\$300 - \$3C7	LCD Display memory
\$3C8 - \$3FF	Data Memory
\$430 - \$7FF	
\$830 - \$BFF	
\$C30 - \$FFF	
\$1030 - \$13FF	
\$1430 - \$1787	

Note:

\$400 - \$42F, \$800 - \$82F, \$C00 - \$C2F, \$1000 - \$102F, \$1400 - \$142F, \$1800 - \$182F and \$000 - \$02F refer to the same System Register.

RAM bank table: (RAMBNK: System Register RAMBNK2 - 0)

RAMBNK = 000	**Bank 0** B = 000	**Bank 1** B = 001	**Bank 2** B = 010	**Bank 3** B = 011	**Bank 4** B = 100	**Bank 5** B = 101	**Bank 6** B = 110	**Bank 7** B = 111
	$030 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3FF
RAMBNK = 001	**Bank 8** B = 000	**Bank 9** B = 001	**Bank 10** B = 010	**Bank 11** B = 011	**Bank 12** B = 100	**Bank 13** B = 101	**Bank 14** B = 110	**Bank 15** B = 111
	$430 - $47F	$480 - $4FF	$500 - $57F	$580 - $5FF	$600 - $67F	$680 - $6FF	$700 - $77F	$780 - $7FF
RAMBNK = 010	**Bank 16** B = 000	**Bank 17** B = 001	**Bank 18** B = 010	**Bank 19** B = 011	**Bank 20** B = 100	**Bank 21** B = 101	**Bank 22** B = 110	**Bank 23** B = 111
	$830 - $87F	$880 - $8FF	$900 - $97F	$980 - $9FF	$A00 - $A7F	$A80 - $AFF	$B00 - $B7F	$B80 - $BFF
RAMBNK = 011	**Bank 24** B = 000	**Bank 25** B = 001	**Bank 26** B = 010	**Bank 27** B = 011	**Bank 28** B = 100	**Bank 29** B = 101	**Bank 30** B = 110	**Bank 31** B = 111
	$C30 - $C7F	$C80 - $CFF	$D00 - $D7F	$D80 - $DFF	$E00 - $E7F	$E80 - $EFF	$F00 - $F7F	$F80 - $FFF
RAMBNK = 100	**Bank 32** B = 000	**Bank 33** B = 001	**Bank 34** B = 010	**Bank 35** B = 011	**Bank 36** B = 100	**Bank 37** B = 101	**Bank 38** B = 110	**Bank 39** B = 111
	$1030 - $107F	$1080 - $10FF	$1100 - $117F	$1180 - $11FF	$1200 - $127F	$1280 - $12FF	$1300 - $137F	$1380 - $13FF
RAMBNK = 101	**Bank 40** B = 000	**Bank 41** B = 001	**Bank 42** B = 010	**Bank 43** B = 011	**Bank 44** B = 100	**Bank 45** B = 101	**Bank 46** B = 110	**Bank 47** B = 111
	$1430 - $147F	$1480 - $14FF	$1500 - $157F	$1580 - $15FF	$1600 - $167F	$1680 - $16FF	$1700 - $177F	$1780 - $1787

2.2 Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX0	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQEX0	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	TM0.3	TM0.2	TM0.1	TM0.0	R/W	Timer0 mode register
$03	TM1.3	TM1.2	TM1.1	TM1.0	R/W	Timer1 mode register
$04	TL0L.3	TL0L.2	TL0L.1	TL0L.0	W	Timer0 load low nibble
	TC0L.3	TC0L.2	TC0L.1	TC0L.0	R	Counter0 low nibble
$05	TL0H.3	TL0H.2	TL0H.1	TL0H.0	W	Timer0 load high nibble
	TC0H.3	TC0H.2	TC0H.1	TC0H.0	R	Counter0 high nibble
$06	TL1L.3	TL1L.2	TL1L.1	TL1L.0	W	Timer1 load low nibble
	TC1L.3	TC1L.2	TC1L.1	TC1L.0	R	Counter1 low nibble
$07	TL1H.3	TL1H.2	TL1H.1	TL1H.0	W	Timer1 load high nibble
	TC1H.3	TC1H.2	TC1H.1	TC1H.0	R	Counter1 high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	-	PF.2	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX1	INX.0	R/W	Index register (INX)
$10	DPL3	DPL2	DPL1	DPL0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PUMP_ON	LCDON	BIAS	DUTY	R/W	Bit0: Select LCD DUTY (1/16 or 1/8) Bit1: Select LCD Bias (1/4 or 1/5 Bias) Bit2: LCD on/off switch Bit3: LCD voltage Pump on
$14	LCDM3	LCDM2	LCDM1	LCDM0	R/W	Lcd contrast adjustment
$15	PB2 - 0/CID	O/S2	O/S1	O/S0	R/W	Bit2 - 0: Set LCD segment / I/O Port mode Bit3: PORTB2 - 0 shared with Caller ID control bit
$16	PA0_PEN	PL/PH	INT0 _FSKIN0	INT0 _PA0	R/W	Bit3: Pull-high/low resistor control bit of PORTA0 0: Pull-high/low resistor disable 1: Pull-high/low resistor enable Bit2: Pull-low resistor or pull-high resistor selection control bit of PORTA0 0: Pull- high resistor enable, Pull-low resistor disable 1: Pull- high resistor disable, Pull-low resistor enable Bit1: Interrupt mode of FSK recevier (one source of INT0) 0: Falling edge interrupt of FSK receiver 1: Rising edge interrupt of FSK receiver Bit0: Interrupt mode of PORTA0 (one source of INT0) 0: Falling edge interrupt of PORTA0 1: Rising edge interrupt of PORTA0

Configuration of System Register (Continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	FSKIN_ STAT	IRQ_ FSKTX	IRQ_ FSKIN	IRQ_PA0	R/W	IRQ_PA0: the interrupt flag of the PORTA0 IRQ_FSKIN: the interrupt flag of the FSK CMP IRQ_FSKTX: the interrupt flag of the FSK generator after a FSK data is transmitted FSKIN_STAT: the status bit of FSKIN level 1: the source of FSKIN is high level 0: the source of FSKIN is low level
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	Set PORTA to be output or input mode
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	Set PORTB to be output or input mode
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	Set PORTC to be output or input mode
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	Set PORTD to be output or input mode
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	Set PORTE to be output or input mode
$1D	-	PFCR.2	PFCR.1	PFCR.0	R/W	Set PORTF to be output or input mode
$1E	PPULL	HLM	OXM	OXON	R/W	Bit3: Port pull-High resistor control Bit2: Heavy load mode Bit1 CPU clocks select (1: OSCX/0: OSC) Bit0: Turn on OSCX oscillator
$1F	ROM BNK3	ROM BNK2	ROM BNK1	ROM BNK0	W	ROM bank register
$20	-	RAM BNK2	RAM BNK1	RAM BNK0	W	RAM bank register
$21	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address / data register
$22	RDT.7	RDT.6	RDT.5	RDT.4	R/W	
$23	RDT.11	RDT.10	RDT.9	RDT.8	R/W	
$24	RDT.15	RDT.14	RDT.13	RDT.12	R/W	
$25	DF_F	DC2	DC1	DC0	R/W	Bit2 - 0: The number of data filter table Bit3: Flag indicate Digital filter calculation is finished. When DFL is off or calculation is finished, the flag is 1. 0: calculation is in process 1: calculation is finished
$26	FSK_ON	FSK_ DTMF	TGC_COL	TGC_ROW	R/W	DTMF/FSK control register
$27	ADCC	FSK_MD	FSK_PRE	FSK_TXEN	R R/W R/W R/W	ADCC: the flag while ADC convert finished Bit2 - 0: FSK control bits
$28	FSK_D7	FSK_D6	FSK_D5	FSK_D4	R/W	High nibble data of FSK Data to be transimitted
$29	FSK_D3/ TGD3	FSK_D2/ TGD2	FSK_D1/ TGD1	FSK_D0/ TGD0	R/W	Low nibble data of FSK Data to be transimitted/ Tone data register

Configuration of System Register (Continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2A	AMP_ON	AGC_ON	DFIL_ON	ADC_ON	R/W	CID interface control register
$2B	GCD3	GCD2	GCD1	GCD0	W	AGC gain data
	ADCD3	ADCD2	ADCD1	ADCD0	R	ADC data register
$2C	WDT	WT2	WT1	WT0	R W W W	Bit3: Watchdog time-out flag bit (read operation to reset WDT) Bit2 - 0: Watchdog timer prescaler
$2D	CMPW1	CMPW0	-	O/S3	R/W	Bit3 - 2: the schmit-trigger voltage windows control bits Bit0: Set the segment35 - 24 as sacn output port or segment signal output for LCD 0: set Segment 35 - 24 as segment signal output for LCD 1: set Segment 35 - 24 as scan output port
$2E	-	-	B0	B1	R	Bit1, 0: Bonding option (read only)
$2F	CAS/ DTMF	-	-	INT0 _FSKIN1	R/W	Bit3: The DTMF/CAS decoder selected control bit 0: DTMF decoder 1: CAS decoder Bit0: The interrupt mode of FSK receiver control bit, when this bit is set to 1, the bit of INT0_FSKIN0 is unused. 0: the interrupt edge type of FSK receiver is set by INT0_FSKIN0 1: Dual edge interrupt mode (rising/falling edge) regardless of the bit of INT0_FSKIN0

Configuration of System Register (Continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1740	D7	D6	D5	D4	R/W	FL1C/S: sum sin value of 697Hz Or FCAS1L/S: sum sin value of 2130Hz
$1741	D3	D2	D1	D0	R/W	
$1742	D15	D14	D13	D12	R/W	
$1743	D11	D10	D9	D8	R/W	
$1744	D7	D6	D5	D4	R/W	FL1C/C: sum cos value of 697Hz Or FCAS1L/C: sum cos value of 2130Hz
$1745	D3	D2	D1	D0	R/W	
$1746	D15	D14	D13	D12	R/W	
$1747	D11	D10	D9	D8	R/W	
$1748	D7	D6	D5	D4	R/W	FL2C/S: sum sin value of 770Hz Or FCAS1H/S: sum sin value of 2750Hz
$1749	D3	D2	D1	D0	R/W	
$174A	D15	D14	D13	D12	R/W	
$174B	D11	D10	D9	D8	R/W	
$174C	D7	D6	D5	D4	R/W	FL2C/C: sum cos value of 770Hz Or FCAS1H/C: sum cos value of 2750Hz
$174D	D3	D2	D1	D0	R/W	
$174E	D15	D14	D13	D12	R/W	
$174F	D11	D10	D9	D8	R/W	
$1750	D7	D6	D5	D4	R/W	FL3C/S: sum sin value of 852Hz Or FCAS2L/S: sum sin value of 4260Hz
$1751	D3	D2	D1	D0	R/W	
$1752	D15	D14	D13	D12	R/W	
$1753	D11	D10	D9	D8	R/W	
$1754	D7	D6	D5	D4	R/W	FL3C/C: sum cos value of 852Hz Or FCAS2L/C: sum cos value of 4260Hz
$1755	D3	D2	D1	D0	R/W	
$1756	D15	D14	D13	D12	R/W	
$1A57	D11	D10	D9	D8	R/W	
$1758	D7	D6	D5	D4	R/W	FL4C/S: sum sin value of 941Hz Or FCAS2H/S: sum sin value of 5500Hz
$1759	D3	D2	D1	D0	R/W	
$175A	D15	D14	D13	D12	R/W	
$175B	D11	D10	D9	D8	R/W	
$175C	D7	D6	D5	D4	R/W	FL4C/C: sum cos value of 941Hz Or FCAS2H/C: sum sin value of 5500Hz
$175D	D3	D2	D1	D0	R/W	
$175E	D15	D14	D13	D12	R/W	
$175F	D11	D10	D9	D8	R/W	
$1760	D7	D6	D5	D4	R/W	FH1R/S: sum sin value of 1209Hz
$1761	D3	D2	D1	D0	R/W	
$1762	D15	D14	D13	D12	R/W	
$1763	D11	D10	D9	D8	R/W	

Configuration of System Register (Continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1764	D7	D6	D5	D4	R/W	FH1R/C: sum cos value of 1209Hz
$1765	D3	D2	D1	D0	R/W	
$1766	D15	D14	D13	D12	R/W	
$1767	D11	D10	D9	D8	R/W	
$1768	D7	D6	D5	D4	R/W	FH2R/S: sum sin value of 1336Hz
$1769	D3	D2	D1	D0	R/W	
$176A	D15	D14	D13	D12	R/W	
$176B	D11	D10	D9	D8	R/W	
$176C	D7	D6	D5	D4	R/W	FH2R/C: sum cos value of 1336Hz
$176D	D3	D2	D1	D0	R/W	
$176E	D15	D14	D13	D12	R/W	
$176F	D11	D10	D9	D8	R/W	
$1770	D7	D6	D5	D4	R/W	FH3R/S: sum sin value of 1477Hz
$1771	D3	D2	D1	D0	R/W	
$1772	D15	D14	D13	D12	R/W	
$1773	D11	D10	D9	D8	R/W	
$1774	D7	D6	D5	D4	R/W	FH3R/C: sum cos value of 1477Hz
$1775	D3	D2	D1	D0	R/W	
$1776	D15	D14	D13	D12	R/W	
$1777	D11	D10	D9	D8	R/W	
$1778	D7	D6	D5	D4	R/W	FH4R/S: sum sin value of 1633Hz
$1779	D3	D2	D1	D0	R/W	
$177A	D15	D14	D13	D12	R/W	
$177B	D11	D10	D9	D8	R/W	
$177C	D7	D6	D5	D4	R/W	FH4R/C: sum cos value of 1633Hz
$177D	D3	D2	D1	D0	R/W	
$177E	D15	D14	D13	D12	R/W	
$177F	D11	D10	D9	D8	R/W	
$1780	-	DFTA14	DFTA13	DFTA12	R/W	Digital filter data table start address
$1781	DFTA11	DFTA10	DFTA9	DFTA8	R/W	
$1782	DFTA7	DFTA6	DFTA5	DFTA4	R/W	
$1783	DFTA3	DFTA2	DFTA1	DFTA0	R/W	
$1784	D11	D10	D9	D8	R/W	Sample Dot-number register (12K sample rate)
$1785	D7	D6	D5	D4	R/W	
$1786	D3	D2	D1	D0	R/W	

3. ROM

The ROM can address 24576 Words X 16 bits of program area from $0000 to $5FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $0004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Function
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to $\overline{\text{INT0}}$ service routine (PORTA.0/FSK IN/FSK Generator)
$002	JMP*	Jump to Timer0 service routine
$003	JMP*	Jump to Timer1 service routine
$004	JMP*	Jump to $\overline{\text{INT1}}$ service routine (PORTB, PORTC, PORTD)

*JMP instruction can be replaced by any instruction.

3.2. Table Data Reference

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$22	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$23	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$24	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 16 bit write-only PC address load register (RDT.15- RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first and then low nibble), after one instruction, users can read out the right data from RDT register. (Write lowest nibble of address into $21 will start the data read-out action).

3.3 Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU address space maps to one of the 11 banks (BNK.3 - 0 = $00 - $0A) of the upper 22K of ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space							
	BNK = $00	BNK = $01	BNK = $02	BNK = $03	BNK = $04	BNK = $05	BNK = $06	BNK = $07
$000 - $7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
$800 - $FFF	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)	2000 - 27FF (BANK 4)	2800 - 2FFF (BANK 5)	3000 - 37FF (BANK 6)	3800 - 3FFF (BANK 7)	4000 - 47FF (BANK 8)

CPU Address	ROM Space		
	BNK = $08	BNK = $09	BNK = $0A
$000 - $7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
$800 - $FFF	4800 - 4FFF (BANK 9)	5000 - 57FF (BANK 10)	5800 – 5FFF (BANK 11)

4. Initial State

4.1. System Register State

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset	WDT Reset
$00	IEX0	IET0	IET1	IEP	0000	0000
$01	IRQEX0	IRQT0	IRQT1	IRQP	0000	0000
$02	TM0.3	TM0.2	TM0.1	TM0.0	0000	0000
$03	TM1.3	TM1.2	TM1.1	TM1.0	0000	0000
$04	TL0L.3	TL0L.2	TL0L.1	TL0L.0	0000	0000
	TC0L.3	TC0L.2	TC0L.1	TC0L.0	0000	0000
$05	TL0H.3	TL0H.2	TL0H.1	TL0H.0	0000	0000
	TC0H.3	TC0H.2	TC0H.1	TC0H.0	0000	0000
$06	TL1L.3	TL1L.2	TL1L.1	TL1L.0	0000	0000
	TC1L.3	TC1L.2	TC1L.1	TC1L.0	0000	0000
$07	TL1H.3	TL1H.2	TL1H.1	TL1H.0	0000	0000
	TC1H.3	TC1H.2	TC1H.1	TC1H.0	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	-	PF.2	PF.1	PF.0	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	xxxx
$0F	INX.3	INX.2	INX1	INX.0	xxxx	xxxx
$10	DPL3	DPL2	DPL1	DPL0	xxxx	xxxx
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-xxx
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-xxx
$13	PUMP_ON	LCDON	BIAS	DUTY	0000	0000
$14	LCDM3	LCDM2	LCDM1	LCDM0	0110	0110
$15	PB2 - 0/CID	O/S2	O/S1	O/S0	0000	0000

System Register State (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset	WDT Reset
$16	PA0_PEN	PL/PH	INT0_FSKIN0	INT0_PA0	0000	0000
$17	FSKIN_STAT	IRQ_FSKTX	IRQ_FSKIN	IRQ_PA0	x000	x000
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1D	-	PFCR.2	PFCR.1	PFCR.0	0000	0000
$1E	PPULL	HLM	OXM	OXON	0000	0000
$1F	ROM BNK3	ROM BNK2	ROM BNK1	ROM BNK0	0000	0000
$20	-	RAM BNK2	RAM BNK1	RAM BNK0	0000	0000
$21	RDT.3	RDT.2	RDT.1	RDT.0	0000	0000
$22	RDT.7	RDT.6	RDT.5	RDT.4	0000	0000
$23	RDT.11	RDT.10	RDT.9	RDT.8	0000	0000
$24	RDT.15	RDT.14	RDT.13	RDT.12	0000	0000
$25	DF_F	DC2	DC1	DC0	1000	1000
$26	FSK_ON	FSK_DTMF	TGC_COL	TGC_ROW	0000	0000
$27	ADCC	FSK_MD	FSK_PRE	FSK_TXEN	0000	0000
$28	FSK_D7	FSK_D6	FSK_D5	FSK_D4	0000	0000
$29	FSK_D3/TGD3	FSK_D2/TGD2	FSK_D1/TGD1	FSK_D0/TGD0	0000	0000
$2A	AMP_ON	AGC_ON	DFIL_ON	ADC_ON	0000	0000
$2B	GCD3	GCD2	GCD1	GCD0	1111	1111
	ADCD3	ADCD2	ADCD1	ADCD0	1000	1000
$2C	WDT	WT2	WT1	WT0	0000	u000
$2D	CMPW1	CMPW0	-	O/S3	00 – 0	00 – 0
$2E	-	-	B0	B1	- - 10	- - 10
$2F	CAS/DTMF	-	-	INT0_FSKIN1	0 - -0	0 - -0

System Register State (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset	WDT Reset
$1740	D7	D6	D5	D4	xxxx	xxxx
$1741	D3	D2	D1	D0	xxxx	xxxx
$1742	D15	D14	D13	D12	xxxx	xxxx
$1743	D11	D10	D9	D8	xxxx	xxxx
$1744	D7	D6	D5	D4	xxxx	xxxx
$1745	D3	D2	D1	D0	xxxx	xxxx
$1746	D15	D14	D13	D12	xxxx	xxxx
$1747	D11	D10	D9	D8	xxxx	xxxx
$1748	D7	D6	D5	D4	xxxx	xxxx
$1749	D3	D2	D1	D0	xxxx	xxxx
$174A	D15	D14	D13	D12	xxxx	xxxx
$174B	D11	D10	D9	D8	xxxx	xxxx
$174C	D7	D6	D5	D4	xxxx	xxxx
$174D	D3	D2	D1	D0	xxxx	xxxx
$174E	D15	D14	D13	D12	xxxx	xxxx
$174F	D11	D10	D9	D8	xxxx	xxxx
$1750	D7	D6	D5	D4	xxxx	xxxx
$1751	D3	D2	D1	D0	xxxx	xxxx
$1752	D15	D14	D13	D12	xxxx	xxxx
$1753	D11	D10	D9	D8	xxxx	xxxx
$1754	D7	D6	D5	D4	xxxx	xxxx
$1755	D3	D2	D1	D0	xxxx	xxxx
$1756	D15	D14	D13	D12	xxxx	xxxx
$1A57	D11	D10	D9	D8	xxxx	xxxx
$1758	D7	D6	D5	D4	xxxx	xxxx
$1759	D3	D2	D1	D0	xxxx	xxxx
$175A	D15	D14	D13	D12	xxxx	xxxx
$175B	D11	D10	D9	D8	xxxx	xxxx
$175C	D7	D6	D5	D4	xxxx	xxxx
$175D	D3	D2	D1	D0	xxxx	xxxx
$175E	D15	D14	D13	D12	xxxx	xxxx
$175F	D11	D10	D9	D8	xxxx	xxxx
$1760	D7	D6	D5	D4	xxxx	xxxx
$1761	D3	D2	D1	D0	xxxx	xxxx
$1762	D15	D14	D13	D12	xxxx	xxxx
$1763	D11	D10	D9	D8	xxxx	xxxx
$1764	D7	D6	D5	D4	xxxx	xxxx
$1765	D3	D2	D1	D0	xxxx	xxxx
$1766	D15	D14	D13	D12	xxxx	xxxx
$1767	D11	D10	D9	D8	xxxx	xxxx
$1768	D7	D6	D5	D4	xxxx	xxxx

System Register State (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset	WDT Reset
$1769	D3	D2	D1	D0	xxxx	xxxx
$176A	D15	D14	D13	D12	xxxx	xxxx
$176B	D11	D10	D9	D8	xxxx	xxxx
$176C	D7	D6	D5	D4	xxxx	xxxx
$176D	D3	D2	D1	D0	xxxx	xxxx
$176E	D15	D14	D13	D12	xxxx	xxxx
$176F	D11	D10	D9	D8	xxxx	xxxx
$1770	D7	D6	D5	D4	xxxx	xxxx
$1771	D3	D2	D1	D0	xxxx	xxxx
$1772	D15	D14	D13	D12	xxxx	xxxx
$1773	D11	D10	D9	D8	xxxx	xxxx
$1774	D7	D6	D5	D4	xxxx	xxxx
$1775	D3	D2	D1	D0	xxxx	xxxx
$1776	D15	D14	D13	D12	xxxx	xxxx
$1777	D11	D10	D9	D8	xxxx	xxxx
$1778	D7	D6	D5	D4	xxxx	xxxx
$1779	D3	D2	D1	D0	xxxx	xxxx
$177A	D15	D14	D13	D12	xxxx	xxxx
$177B	D11	D10	D9	D8	xxxx	xxxx
$177C	D7	D6	D5	D4	xxxx	xxxx
$177D	D3	D2	D1	D0	xxxx	xxxx
$177E	D15	D14	D13	D12	xxxx	xxxx
$177F	D11	D10	D9	D8	xxxx	xxxx
$1780	-	DFTA14	DFTA13	DFTA12	0000	0000
$1781	DFTA11	DFTA10	DFTA9	DFTA8	0000	0000
$1782	DFTA7	DFTA6	DFTA5	DFTA4	0000	0000
$1783	DFTA3	DFTA2	DFTA1	DFTA0	0000	0000
$1784	D11	D10	D9	D8	0000	0000
$1785	D7	D6	D5	D4	0000	0000
$1786	D3	D2	D1	D0	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4

5.1. Instruction Cycle Time:

(1) 4/32.768kHz (≈ 122.12μs) for 32.768kHz oscillator.
(2) 4/262kHz(≈ 15.27μs) for 262kHz oscillator.
(3) 4/1.8MHz (≈ 5.56μs) for 1.8MHz oscillator.
(4) 4/3.58MHz (= 1μs) for 3.58MHz oscillator.

5.2. Circuit Configuration

SH67K93 has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ. 32.768kHz) or RC (Typ.262kHz) determined by the code option. This is designed for low frequency operation. OSCX also has two types: ceramic (Typ.3.58MHz) or RC (1.8MHz) determined by code option. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At the starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC clock is automatically selected as the system clock input source.

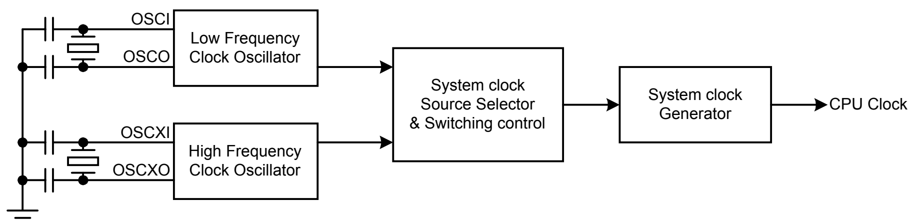


Figure 1. Oscillator Block Diagram

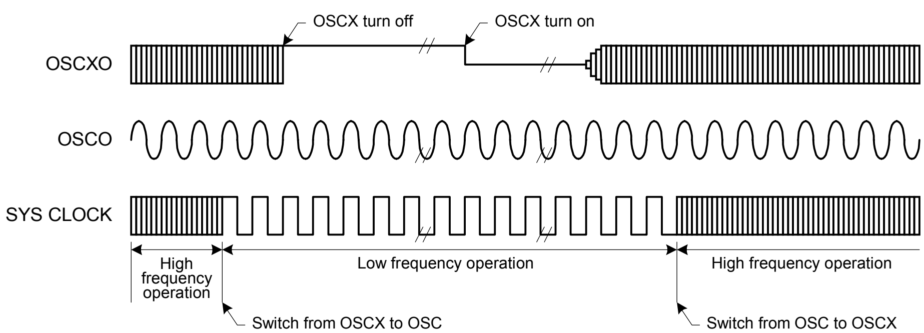
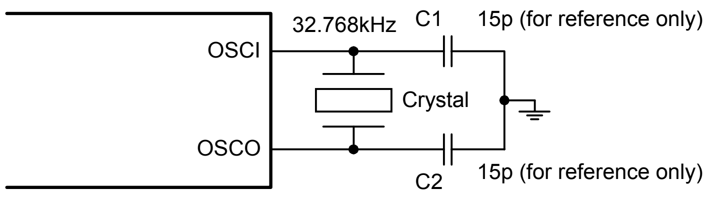


Figure 2. Timing of System Clock Switching

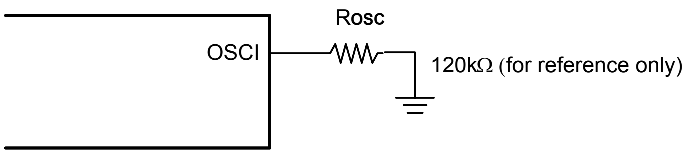
5.3. OSC Oscillation

The OSC generates the basic clock pulses that provide the CPU and peripherals (Timer0, Timer1, LCD) with an operating clock.

(1) OSC Crystal oscillator type



(2) OSC RC oscillator type

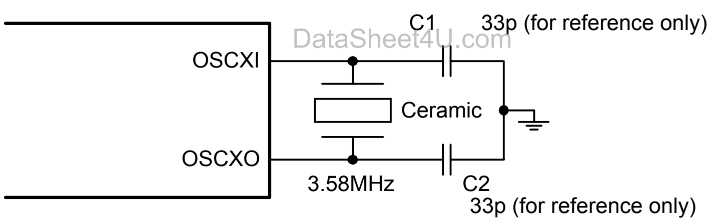


5.4. OSCX Oscillator

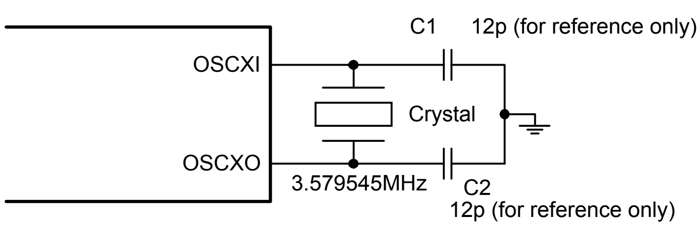
OSCX has two clock oscillators. The code options select the Ceramic/Crystal or RC as the CPU's clock.

If the OSCX is not used, it must be masked to be Ceramic resonator and the OSCXI must be connected to GND.

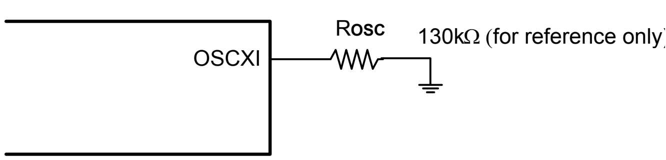
(1) OSCX Ceramic oscillator type



(2) OSCX Crystal oscillator type



(3) OSCX RC oscillator type



5.5. Control of Oscillator

The oscillator control register configuration is shown as blow.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1E	PPULL	HLM	OXM	OXON	R/W	OSCX and System Clock control register

OXON: OSCX oscillation on/off.
0: Turn off OSCX oscillation
1: Turn on OSCX oscillation

OXM: switching system clock.
0: select OSC as system clock
1: select OSCX as system clock

5.6. Programming Notes

It takes at least 5 ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, one must wait a minimum of 5ms till the OSCX oscillation is active. However, the start time varies a lot with respect to oscillator characteristics and operational conditions. Therefore the waiting time depends on applications.

When switching from OSCX to OSC, and turning off OSCX in one instruction, the OSCX turn off control would be delayed for one instruction cycle automatically to prevent CPU operation error.

6. I/O PORT

The MCU provides 24 bi-directional I/O pads. The PORT data put in register $08 - $0D. The PORT control register ($18 - $1E) controls the PORT as input or output. Each I/O port for PORTA [3:1], PORTB, PORTC, PORTD, PORTE, PORTF has an internal pull-high resistor, which is controlled by PPULL of $1E and the data of the port, when the PORT is used as input. PORTA.0 has an internal pull-high resistor and an internal pull-low resistor, which is controlled by PA0_PEN and PL/PH of $16 when the PORT is used as input.

Port I/O mapping address is shown as follows:

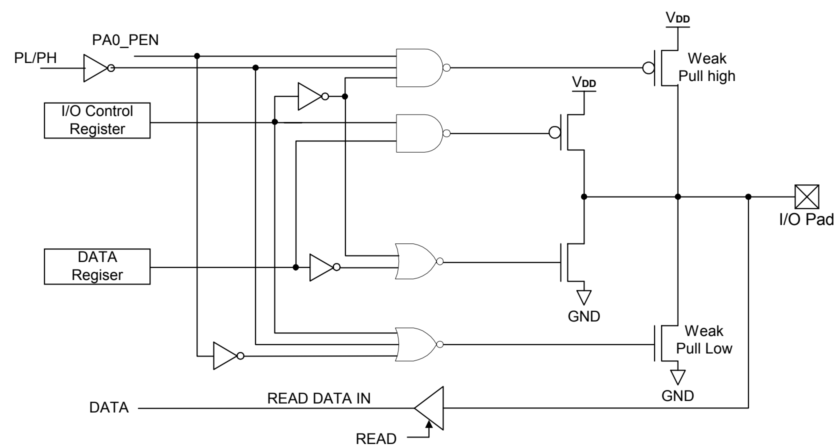
Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data
$0D	-	PF.2	PF.1	PF.0	R/W	PORTF data
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output contro
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control
$1D	-	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control

PA (/B/C/D/E/F) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

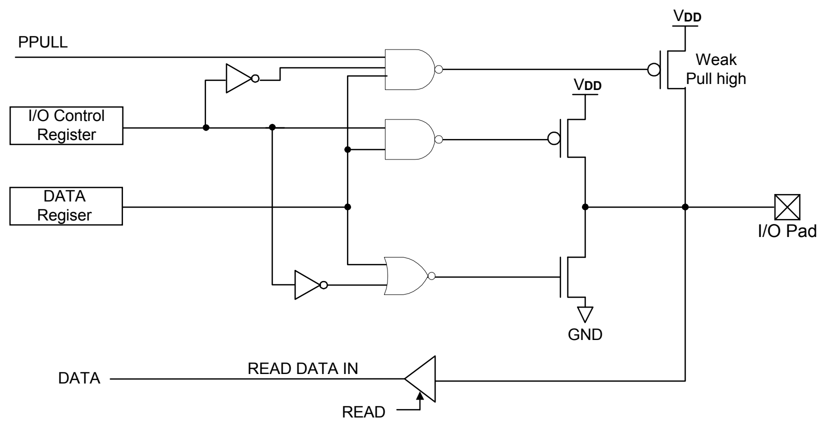
Note:

For PORTA.3 - 1,PORTB, PORTC, PORTD, PORTE, PORTF
When PXCR = 0, Data Register = 1 and PPULL = 1, the Pull-High resistor are enabled, else enabled when one of the above conditions does not match. Turn off the pull-high MOS individually for each port can be done by writing the data register with 0.
For PORTA.0
When PACR.0 = 0, and PA0_PEN = 1, the Pull High/Low resistor is enabled, else enabled when one of the above conditions does not match.

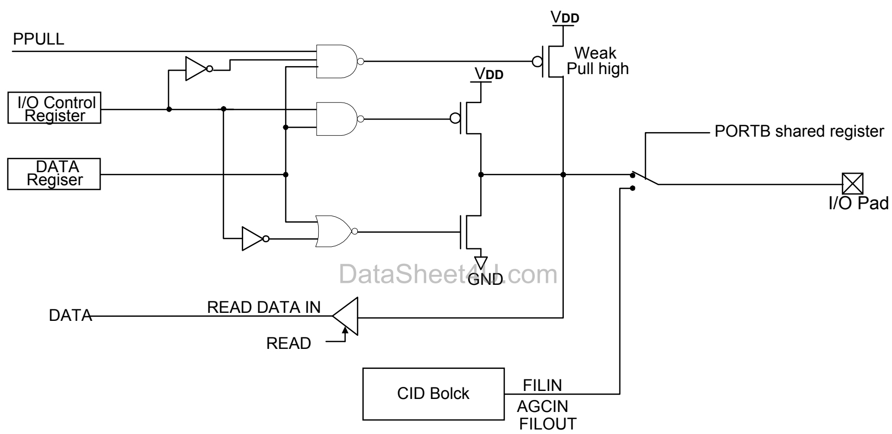
Equivalent Circuit for PORTA, PORTB



PORTA.0

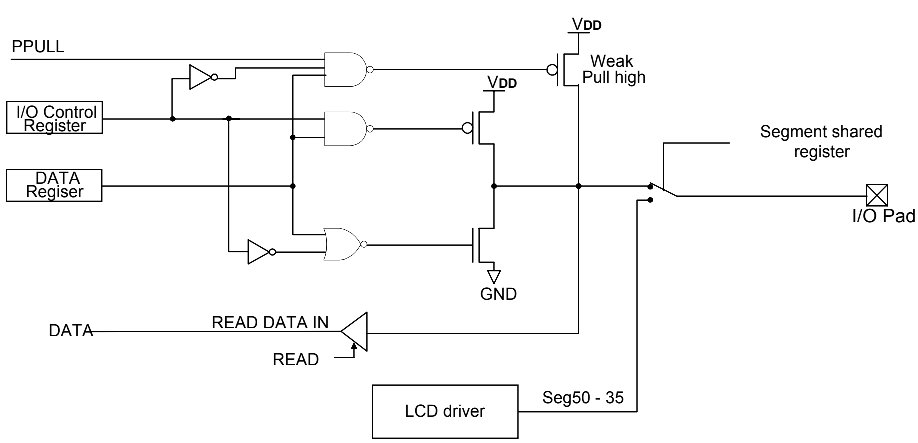


PORTA[3:1], PORTB3



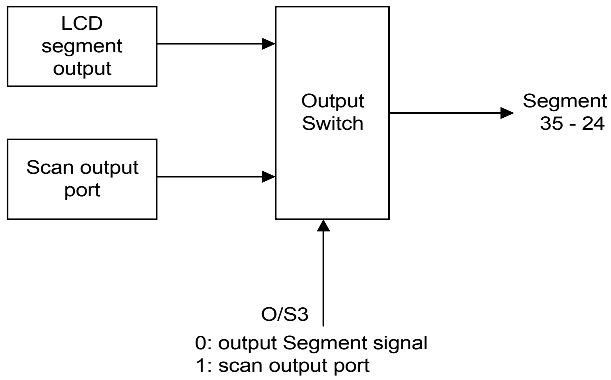
PORTB[2:0]

Equivalent Circuit for PORTC, PORTD, PORTE, PORTF



PORTC, PORTD, PORTE, PORTF

Equivalent Circuit for Scan Output Pads for Segment35 - 24



6.1. System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	PB2 - 0/CID	O/S2	O/S1	O/S0	R/W	Bit2 - 0: Set LCD segment / I/O Port mode Bit3: PortB2 - 0 shared with Caller ID control bit
$16	PA0_PEN	PL/PH	-	-	R/W	PORTA.0 Pull-high/low control register
$1E	PPULL	HLM	OXM	OXON	R/W	Bit3: Port Pull-High resistor control bit for all port except PORTA.0 Bit2: Heavy Load mode
$2D	CMPW1	CMPW0	-	O/S3	R/W	LCD scan output control bit
$3C8	SCAN35	SCAN34	SCAN33	SCAN32	R/W	Scan output data register
$3C9	SCAN31	SCAN30	SCAN29	SCAN28	R/W	
$3CA	SCAN27	SCAN26	SCAN25	SCAN24	R/W	

PA0_PEN: PORTA.0 Pull-high/low resistor control register
1: PORTA.0 pull-high/low resistor enable.
0: PORTA.0 pull-high/low resistor disable

PL/PH: PORTA.0 pull -high or pull-low resistor selection bit
1: select pull-low resistor.
0: select pull-high resistor.

PB2 - 0/CID: PORTB [2:0] share with CID interface control bit
1: PORTB [2:0] set as input/output Port
0: PORTB.2 set as FILIN input pad
PORTB.1 set as FILOUT pad
PORTB.0 set as AGCIN input pad

HLM: Heavy Load Mode control bit
0: Disable
1: Enable

PPULL: The Pull-High resistor control bit for all Ports except PORTA.0
0: Pull-High resistor control disable
1: Pull-High resistor control enable

O/S2 - 0: PORTC/Seg50 - 47, PORTD/Seg46 - 43, PORTE/Seg42 - 39, PORTF/Seg38 - 36 sharing control bit

O/S2	O/S1	O/S0	Seg50 - 47	Seg46 - 43	Seg42 - 39	Seg38 - 36
0	0	0	Seg50 - 47	Seg46 - 43	Seg42 - 39	Seg38 - 36
0	0	1	PortC	Seg46 - 43	Seg42 - 39	Seg38 - 36
0	1	0	PortC	PortD	Seg42 - 39	Seg38 - 36
0	1	1	PortC	PortD	PortE	Seg38 - 36
1	0	0	PortC	PortD	PortE	PortF
1	0	1	Inhibited			
1	1	0				
1	1	1				

O/S3: Segment35 - 24 scan output control bit

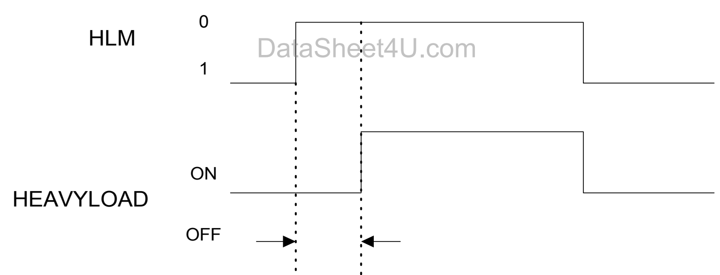
SCAN35 - 24: Segment35 - 24 scan output data register

6.2. Heavy Load Mode (HLM)

The MCU has a heavy load protection circuit when the battery load becomes heavy, such as, when an external buzzer sounds or an external speaker is turned on. In this mode, the crystal oscillator circuit has been backup for high gain. When this mode is set, more power would be provided to an oscillator circuit. Unless it is nessary, be careful not to set this mode with the software since the mode enter would delay for one instruction. Please activate heavy load driving only after setting HLM at least one instruction wait cycle through the software. The following shows the programming setting.

HLM: 0 = Heavy load protection mode is released

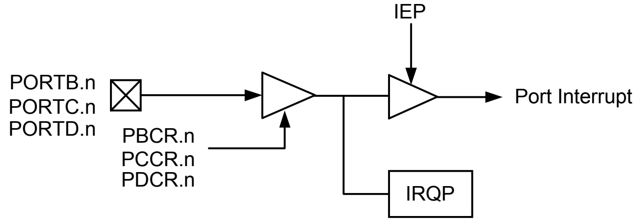
1 = Heavy load protection mode is set.



6.3. Port Interrupt

The PORTB, PORTC and PORTD are used as port interrupt sources.

The following is the port interrupt function block-diagram.



Note: n = 0, 1, 2, 3

Port Interrupt (PBCD INT) Programming Note

If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.

1. Set the port as input port, fill port data register with 1 and avoid port floating.
2. Set the port into Pull-high (Use external pull high resistance or set PPULL to 1).

Any further falling edge transition would not be able to make interrupt request until all of the pads return to V_{DD} in PBCD INT application.

Note:

1. When PORTC and PORTD are shared to segment, user can only generate interrupt on PORTB.
2. The Interrupt function is disable for PORTB2~0 while PORTB.2 - 0 are shared as CID interface.

6.4. External Interrupt ($\overline{\text{INT0}}$)

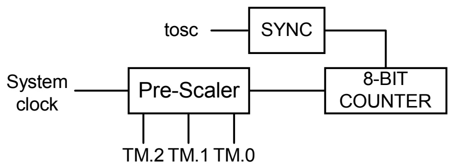
PORTA0 is one of the three external interrupt sources (active low).

7. Timer 0 and 1

SH67K93 has two 8-bit timers.

The timer / counter has the following features:
- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:
- Programmable interval timer function.
- Read counter value.

7.1 TIMER0 and TIMER1 Configurations and Operation

The Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has both low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

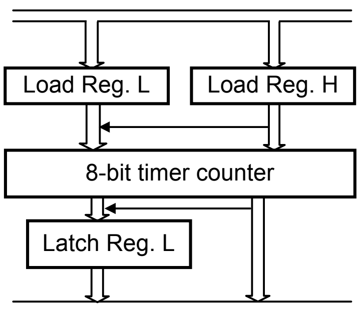
The low-order digit should be written first, and then the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high-order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: The register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:
    Low nibble first
    High nibble to update the counter

Read Operation:
    High nibble first
    Low nibble followed.



7.2. Timer Mode Register (TM0, 1)

The timer can be programmed in several different prescalers by setting Timer Mode register (TM0, TM1).

The 8-bit counter prescaler overflows output pulses. The Timer Mode register (TM0, TM1) is 3-bit register used for the timer control as shown in Table 1. The mode register selects the input pulse sources into the timer. The TM0.3 control bit defines the clock source of timer0. The TM1.3 control bit selects the clock source of timer1.

TM0.3 =0: timer0 clock source = system clock (OSCX/4 or OSC/4) TM0.3 =1: timer0 clock source is generated by OSC/4.

TM1.3 =0: timer1 clock source = system clock (OSCX/4 or OSC/4) TM1.3 =1: timer1 clock source is generated by OSC/4.

Table 1 Timer0, Timer1 Mode registers ($02, $03)

TM1.3/TM0.3	TM1.2/TM0.2	TM1.1/TM0.1	TM1.0/TM0.0	Prescaler	Clock Source
0	0	0	0	/2048	System clock (OSCX/4 or OSC/4)
0	0	0	1	/512	
0	0	1	0	/128	
0	0	1	1	/32	
0	1	0	0	/8	
0	1	0	1	/4	
0	1	1	0	/2	
0	1	1	1	/1	
1	0	0	0	/2048	OSC/4
1	0	0	1	/512	
1	0	1	0	/128	
1	0	1	1	/32	
1	1	0	0	/8	
1	1	0	1	/4	
1	1	1	0	/2	
1	1	1	1	/1	

8. LCD Driver

The LCD driver contains a controller, a voltage generator, 16 common signal pads and 50 segment driver pads. There are 4 different programmable driving modes: 1/16 duty & 1/5 bias, 1/16 duty & 1/4 bias, 1/8 duty & 1/4 bias, 1/8 duty & 1/5 bias. The driving mode is controlled by the system register $13 and the power on initialization status is 1/16 duty, and 1/4 bias. The controller consists of display data RAM and a duty generator.

The LCD SEG50 - 36 can also be used as I/O port (PORTC, PORTD, PORTE and PORTF), which is selected by bit 2 - 0 of the system register $15. LCD RAM could be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the previous value.

When LCD is off, both common and segment output low.

8.1. LCD Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PUMP_ON	LCDON	BIAS	DUTY	R/W	LCD control register0
$15	PB2 - 0/CID	O/S2	O/S1	O/S0	R/W	LCD control register1
$3C8	SCAN35	SCAN34	SCAN33	SCAN32	R/W	Data Register of LCD SEG35 - 32 when SEG35 - 32 shared as output port.
$3C9	SCAN31	SCAN30	SCAN29	SCAN28	R/W	Data Register of LCD SEG31 - 28 when SEG20 - 17 shared as output port.
$3CA	SCAN27	SCAN26	SCAN25	SCAN24	R/W	Data Register of LCD SEG27 - 24 when SEG16 - 13 shared as output port.

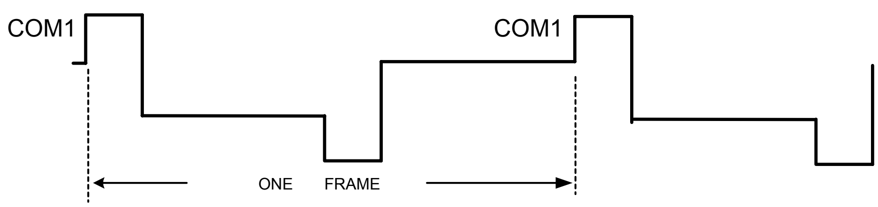
LCD ON/OFF control and LCD driving mode control register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PUMP_ON	LCDON	BIAS	DUTY	R/W	LCD ON/OFF control and LCD driving mode control control
	0	X	X	X		LCD Pump OFF
	1	X	X	X		LCD Pump ON
	X	0	X	X		LCD Display OFF
	X	1	X	X		LCD Display ON
	X	X	0	X		LCD driver = 1/4 bias
	X	X	1	X		LCD driver = 1/5 bias
	X	X	X	0		LCD driver = 1/1 6duty
	X	X	X	1		LCD driver = 1/8duty, COM15 - 8 output low level

LCD Segment shared setting register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PB2~0/CID	O/S2	O/S1	O/S0	R/W	Refer to the description of I/O PORT

The LCD freqence is 64Hz regardless of the OSC is 32.768kHz or 262kHz RC



When the CPU is in STOP mode, the COMx and SEGx are pulled low.

8.2. Configuration of LCD RAM

Segment1- 50, 1/16 duty

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$319	SEG26	SEG26	SEG26	SEG26
$301	SEG2	SEG2	SEG2	SEG2	$31A	SEG27	SEG27	SEG27	SEG27
$302	SEG3	SEG3	SEG3	SEG3	$31B	SEG28	SEG28	SEG28	SEG28
$303	SEG4	SEG4	SEG4	SEG4	$31C	SEG29	SEG29	SEG29	SEG29
$304	SEG5	SEG5	SEG5	SEG5	$31D	SEG30	SEG30	SEG30	SEG30
$305	SEG6	SEG6	SEG6	SEG6	$31E	SEG31	SEG31	SEG31	SEG31
$306	SEG7	SEG7	SEG7	SEG7	$31F	SEG32	SEG32	SEG32	SEG32
$307	SEG8	SEG8	SEG8	SEG8	$320	SEG33	SEG33	SEG33	SEG33
$308	SEG9	SEG9	SEG9	SEG9	$321	SEG34	SEG34	SEG34	SEG34
$309	SEG10	SEG10	SEG10	SEG10	$322	SEG35	SEG35	SEG35	SEG35
$30A	SEG11	SEG11	SEG11	SEG11	$323	SEG36	SEG36	SEG36	SEG36
$30B	SEG12	SEG12	SEG12	SEG12	$324	SEG37	SEG37	SEG37	SEG37
$30C	SEG13	SEG13	SEG13	SEG13	$325	SEG38	SEG38	SEG38	SEG38
$30D	SEG14	SEG14	SEG14	SEG14	$326	SEG39	SEG39	SEG39	SEG39
$30E	SEG15	SEG15	SEG15	SEG15	$327	SEG40	SEG40	SEG40	SEG40
$30F	SEG16	SEG16	SEG16	SEG16	$328	SEG41	SEG41	SEG41	SEG41
$310	SEG17	SEG17	SEG17	SEG17	$329	SEG42	SEG42	SEG42	SEG42
$311	SEG18	SEG18	SEG18	SEG18	$32A	SEG43	SEG43	SEG43	SEG43
$312	SEG19	SEG19	SEG19	SEG19	$32B	SEG44	SEG44	SEG44	SEG44
$313	SEG20	SEG20	SEG20	SEG20	$32C	SEG45	SEG45	SEG45	SEG45
$314	SEG21	SEG21	SEG21	SEG21	$32D	SEG46	SEG46	SEG46	SEG46
$315	SEG22	SEG22	SEG22	SEG22	$32E	SEG47	SEG47	SEG47	SEG47
$316	SEG23	SEG23	SEG23	SEG23	$32F	SEG48	SEG48	SEG48	SEG48
$317	SEG24	SEG24	SEG24	SEG24	$330	SEG49	SEG49	SEG49	SEG49
$318	SEG25	SEG25	SEG25	SEG25	$331	SEG50	SEG50	SEG50	SEG50

Segment1- 50, 1/16 duty (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM8	COM7	COM6	COM5		COM8	COM7	COM6	COM5
$332	SEG1	SEG1	SEG1	SEG1	$34B	SEG26	SEG26	SEG26	SEG26
$333	SEG2	SEG2	SEG2	SEG2	$34C	SEG27	SEG27	SEG27	SEG27
$334	SEG3	SEG3	SEG3	SEG3	$34D	SEG28	SEG28	SEG28	SEG28
$335	SEG4	SEG4	SEG4	SEG4	$34E	SEG29	SEG29	SEG29	SEG29
$336	SEG5	SEG5	SEG5	SEG5	$34F	SEG30	SEG30	SEG30	SEG30
$337	SEG6	SEG6	SEG6	SEG6	$350	SEG31	SEG31	SEG31	SEG31
$338	SEG7	SEG7	SEG7	SEG7	$351	SEG32	SEG32	SEG32	SEG32
$339	SEG8	SEG8	SEG8	SEG8	$352	SEG33	SEG33	SEG33	SEG33
$33A	SEG9	SEG9	SEG9	SEG9	$353	SEG34	SEG34	SEG34	SEG34
$33B	SEG10	SEG10	SEG10	SEG10	$354	SEG35	SEG35	SEG35	SEG35
$33C	SEG11	SEG11	SEG11	SEG11	$355	SEG36	SEG36	SEG36	SEG36
$33D	SEG12	SEG12	SEG12	SEG12	$356	SEG37	SEG37	SEG37	SEG37
$33E	SEG13	SEG13	SEG13	SEG13	$357	SEG38	SEG38	SEG38	SEG38
$33F	SEG14	SEG14	SEG14	SEG14	$358	SEG39	SEG39	SEG39	SEG39
$340	SEG15	SEG15	SEG15	SEG15	$359	SEG40	SEG40	SEG40	SEG40
$341	SEG16	SEG16	SEG16	SEG16	$35A	SEG41	SEG41	SEG41	SEG41
$342	SEG17	SEG17	SEG17	SEG17	$35B	SEG42	SEG42	SEG42	SEG42
$343	SEG18	SEG18	SEG18	SEG18	$35C	SEG43	SEG43	SEG43	SEG43
$344	SEG19	SEG19	SEG19	SEG19	$35D	SEG44	SEG44	SEG44	SEG44
$345	SEG20	SEG20	SEG20	SEG20	$35E	SEG45	SEG45	SEG45	SEG45
$346	SEG21	SEG21	SEG21	SEG21	$35F	SEG46	SEG46	SEG46	SEG46
$347	SEG22	SEG22	SEG22	SEG22	$360	SEG47	SEG47	SEG47	SEG47
$348	SEG23	SEG23	SEG23	SEG23	$361	SEG48	SEG48	SEG48	SEG48
$349	SEG24	SEG24	SEG24	SEG24	$362	SEG49	SEG49	SEG49	SEG49
$34A	SEG25	SEG25	SEG25	SEG25	$363	SEG50	SEG50	SEG50	SEG50

Segment1- 50, 1/16 duty (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM12	COM11	COM10	COM9		COM12	COM11	COM10	COM9
$364	SEG1	SEG1	SEG1	SEG1	$37D	SEG26	SEG26	SEG26	SEG26
$365	SEG2	SEG2	SEG2	SEG2	$37E	SEG27	SEG27	SEG27	SEG27
$366	SEG3	SEG3	SEG3	SEG3	$37F	SEG28	SEG28	SEG28	SEG28
$367	SEG4	SEG4	SEG4	SEG4	$380	SEG29	SEG29	SEG29	SEG29
$368	SEG5	SEG5	SEG5	SEG5	$381	SEG30	SEG30	SEG30	SEG30
$369	SEG6	SEG6	SEG6	SEG6	$382	SEG31	SEG31	SEG31	SEG31
$36A	SEG7	SEG7	SEG7	SEG7	$383	SEG32	SEG32	SEG32	SEG32
$36B	SEG8	SEG8	SEG8	SEG8	$384	SEG33	SEG33	SEG33	SEG33
$36C	SEG9	SEG9	SEG9	SEG9	$385	SEG34	SEG34	SEG34	SEG34
$36D	SEG10	SEG10	SEG10	SEG10	$386	SEG35	SEG35	SEG35	SEG35
$36E	SEG11	SEG11	SEG11	SEG11	$387	SEG36	SEG36	SEG36	SEG36
$36F	SEG12	SEG12	SEG12	SEG12	$388	SEG37	SEG37	SEG37	SEG37
$370	SEG13	SEG13	SEG13	SEG13	$389	SEG38	SEG38	SEG38	SEG38
$371	SEG14	SEG14	SEG14	SEG14	$38A	SEG39	SEG39	SEG39	SEG39
$372	SEG15	SEG15	SEG15	SEG15	$38B	SEG40	SEG40	SEG40	SEG40
$373	SEG16	SEG16	SEG16	SEG16	$38C	SEG41	SEG41	SEG41	SEG41
$374	SEG17	SEG17	SEG17	SEG17	$38D	SEG42	SEG42	SEG42	SEG42
$375	SEG18	SEG18	SEG18	SEG18	$38E	SEG43	SEG43	SEG43	SEG43
$376	SEG19	SEG19	SEG19	SEG19	$38F	SEG44	SEG44	SEG44	SEG44
$377	SEG20	SEG20	SEG20	SEG20	$390	SEG45	SEG45	SEG45	SEG45
$378	SEG21	SEG21	SEG21	SEG21	$391	SEG46	SEG46	SEG46	SEG46
$379	SEG22	SEG22	SEG22	SEG22	$392	SEG47	SEG47	SEG47	SEG47
$37A	SEG23	SEG23	SEG23	SEG23	$393	SEG48	SEG48	SEG48	SEG48
$37B	SEG24	SEG24	SEG24	SEG24	$394	SEG49	SEG49	SEG49	SEG49
$37C	SEG25	SEG25	SEG25	SEG25	$395	SEG50	SEG50	SEG50	SEG50

Segment1- 50, 1/16 duty (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM16	COM15	COM14	COM13		COM16	COM15	COM14	COM13
$396	SEG1	SEG1	SEG1	SEG1	$3AF	SEG26	SEG26	SEG26	SEG26
$397	SEG2	SEG2	SEG2	SEG2	$3B0	SEG27	SEG27	SEG27	SEG27
$398	SEG3	SEG3	SEG3	SEG3	$3B1	SEG28	SEG28	SEG28	SEG28
$399	SEG4	SEG4	SEG4	SEG4	$3B2	SEG29	SEG29	SEG29	SEG29
$39A	SEG5	SEG5	SEG5	SEG5	$3B3	SEG30	SEG30	SEG30	SEG30
$39B	SEG6	SEG6	SEG6	SEG6	$3B4	SEG31	SEG31	SEG31	SEG31
$39C	SEG7	SEG7	SEG7	SEG7	$3B5	SEG32	SEG32	SEG32	SEG32
$39D	SEG8	SEG8	SEG8	SEG8	$3B6	SEG33	SEG33	SEG33	SEG33
$39E	SEG9	SEG9	SEG9	SEG9	$3B7	SEG34	SEG34	SEG34	SEG34
$39F	SEG10	SEG10	SEG10	SEG10	$3B8	SEG35	SEG35	SEG35	SEG35
$3A0	SEG11	SEG11	SEG11	SEG11	$3B9	SEG36	SEG36	SEG36	SEG36
$3A1	SEG12	SEG12	SEG12	SEG12	$3BA	SEG37	SEG37	SEG37	SEG37
$3A2	SEG13	SEG13	SEG13	SEG13	$3BB	SEG38	SEG38	SEG38	SEG38
$3A3	SEG14	SEG14	SEG14	SEG14	$3BC	SEG39	SEG39	SEG39	SEG39
$3A4	SEG15	SEG15	SEG15	SEG15	$3BD	SEG40	SEG40	SEG40	SEG40
$3A5	SEG16	SEG16	SEG16	SEG16	$3BE	SEG41	SEG41	SEG41	SEG41
$3A6	SEG17	SEG17	SEG17	SEG17	$3BF	SEG42	SEG42	SEG42	SEG42
$3A7	SEG18	SEG18	SEG18	SEG18	$3C0	SEG43	SEG43	SEG43	SEG43
$3A8	SEG19	SEG19	SEG19	SEG19	$3C1	SEG44	SEG44	SEG44	SEG44
$3A9	SEG20	SEG20	SEG20	SEG20	$3C2	SEG45	SEG45	SEG45	SEG45
$3AA	SEG21	SEG21	SEG21	SEG21	$3C3	SEG46	SEG46	SEG46	SEG46
$3AB	SEG22	SEG22	SEG22	SEG22	$3C4	SEG47	SEG47	SEG47	SEG47
$3AC	SEG23	SEG23	SEG23	SEG23	$3C5	SEG48	SEG48	SEG48	SEG48
$3AD	SEG24	SEG24	SEG24	SEG24	$3C6	SEG49	SEG49	SEG49	SEG49
$3AE	SEG25	SEG25	SEG25	SEG25	$3C7	SEG50	SEG50	SEG50	SEG50

Segment1 - 50, 1/8 duty

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$319	SEG26	SEG26	SEG26	SEG26
$301	SEG2	SEG2	SEG2	SEG2	$31A	SEG27	SEG27	SEG27	SEG27
$302	SEG3	SEG3	SEG3	SEG3	$31B	SEG28	SEG28	SEG28	SEG28
$303	SEG4	SEG4	SEG4	SEG4	$31C	SEG29	SEG29	SEG29	SEG29
$304	SEG5	SEG5	SEG5	SEG5	$31D	SEG30	SEG30	SEG30	SEG30
$305	SEG6	SEG6	SEG6	SEG6	$31E	SEG31	SEG31	SEG31	SEG31
$306	SEG7	SEG7	SEG7	SEG7	$31F	SEG32	SEG32	SEG32	SEG32
$307	SEG8	SEG8	SEG8	SEG8	$320	SEG33	SEG33	SEG33	SEG33
$308	SEG9	SEG9	SEG9	SEG9	$321	SEG34	SEG34	SEG34	SEG34
$309	SEG10	SEG10	SEG10	SEG10	$322	SEG35	SEG35	SEG35	SEG35
$30A	SEG11	SEG11	SEG11	SEG11	$323	SEG36	SEG36	SEG36	SEG36
$30B	SEG12	SEG12	SEG12	SEG12	$324	SEG37	SEG37	SEG37	SEG37
$30C	SEG13	SEG13	SEG13	SEG13	$325	SEG38	SEG38	SEG38	SEG38
$30D	SEG14	SEG14	SEG14	SEG14	$326	SEG39	SEG39	SEG39	SEG39
$30E	SEG15	SEG15	SEG15	SEG15	$327	SEG40	SEG40	SEG40	SEG40
$30F	SEG16	SEG16	SEG16	SEG16	$328	SEG41	SEG41	SEG41	SEG41
$310	SEG17	SEG17	SEG17	SEG17	$329	SEG42	SEG42	SEG42	SEG42
$311	SEG18	SEG18	SEG18	SEG18	$32A	SEG43	SEG43	SEG43	SEG43
$312	SEG19	SEG19	SEG19	SEG19	$32B	SEG44	SEG44	SEG44	SEG44
$313	SEG20	SEG20	SEG20	SEG20	$32C	SEG45	SEG45	SEG45	SEG45
$314	SEG21	SEG21	SEG21	SEG21	$32D	SEG46	SEG46	SEG46	SEG46
$315	SEG22	SEG22	SEG22	SEG22	$32E	SEG47	SEG47	SEG47	SEG47
$316	SEG23	SEG23	SEG23	SEG23	$32F	SEG48	SEG48	SEG48	SEG48
$317	SEG24	SEG24	SEG24	SEG24	$330	SEG49	SEG49	SEG49	SEG49
$318	SEG25	SEG25	SEG25	SEG25	$331	SEG50	SEG50	SEG50	SEG50

Segment1 - 50, 1/8 duty (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM8	COM7	COM6	COM5		COM8	COM7	COM6	COM5
$332	SEG1	SEG1	SEG1	SEG1	$34B	SEG26	SEG26	SEG26	SEG26
$333	SEG2	SEG2	SEG2	SEG2	$34C	SEG27	SEG27	SEG27	SEG27
$334	SEG3	SEG3	SEG3	SEG3	$34D	SEG28	SEG28	SEG28	SEG28
$335	SEG4	SEG4	SEG4	SEG4	$34E	SEG29	SEG29	SEG29	SEG29
$336	SEG5	SEG5	SEG5	SEG5	$34F	SEG30	SEG30	SEG30	SEG30
$337	SEG6	SEG6	SEG6	SEG6	$350	SEG31	SEG31	SEG31	SEG31
$338	SEG7	SEG7	SEG7	SEG7	$351	SEG32	SEG32	SEG32	SEG32
$339	SEG8	SEG8	SEG8	SEG8	$352	SEG33	SEG33	SEG33	SEG33
$33A	SEG9	SEG9	SEG9	SEG9	$353	SEG34	SEG34	SEG34	SEG34
$33B	SEG10	SEG10	SEG10	SEG10	$354	SEG35	SEG35	SEG35	SEG35
$33C	SEG11	SEG11	SEG11	SEG11	$355	SEG36	SEG36	SEG36	SEG36
$33D	SEG12	SEG12	SEG12	SEG12	$356	SEG37	SEG37	SEG37	SEG37
$33E	SEG13	SEG13	SEG13	SEG13	$357	SEG38	SEG38	SEG38	SEG38
$33F	SEG14	SEG14	SEG14	SEG14	$358	SEG39	SEG39	SEG39	SEG39
$340	SEG15	SEG15	SEG15	SEG15	$359	SEG40	SEG40	SEG40	SEG40
$341	SEG16	SEG16	SEG16	SEG16	$35A	SEG41	SEG41	SEG41	SEG41
$342	SEG17	SEG17	SEG17	SEG17	$35B	SEG42	SEG42	SEG42	SEG42
$343	SEG18	SEG18	SEG18	SEG18	$35C	SEG43	SEG43	SEG43	SEG43
$344	SEG19	SEG19	SEG19	SEG19	$35D	SEG44	SEG44	SEG44	SEG44
$345	SEG20	SEG20	SEG20	SEG20	$35E	SEG45	SEG45	SEG45	SEG45
$346	SEG21	SEG21	SEG21	SEG21	$35F	SEG46	SEG46	SEG46	SEG46
$347	SEG22	SEG22	SEG22	SEG22	$360	SEG47	SEG47	SEG47	SEG47
$348	SEG23	SEG23	SEG23	SEG23	$361	SEG48	SEG48	SEG48	SEG48
$349	SEG24	SEG24	SEG24	SEG24	$362	SEG49	SEG49	SEG49	SEG49
$34A	SEG25	SEG25	SEG25	SEG25	$363	SEG50	SEG50	SEG50	SEG50

8.3. LCD Power

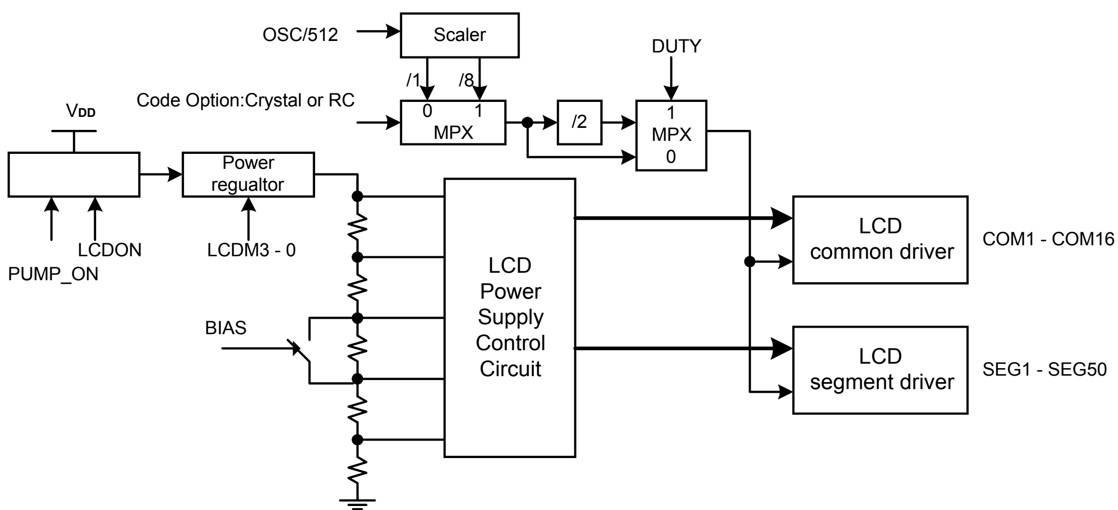


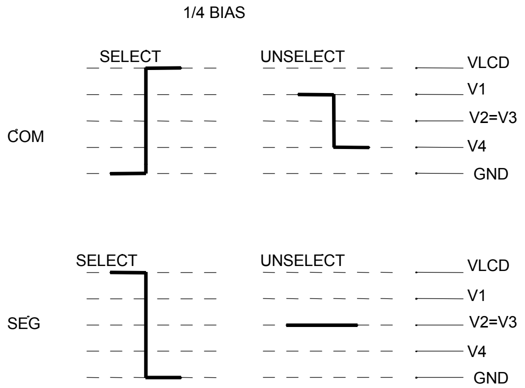
Figure 3. LCD block diagram for reference only

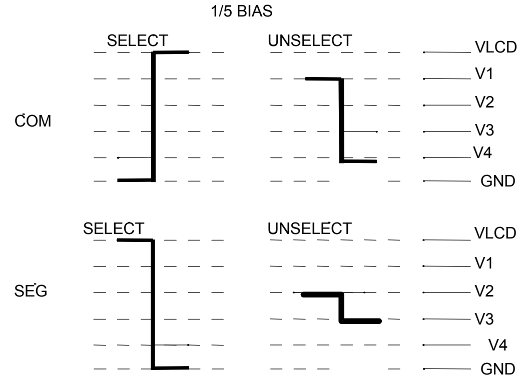
The contrast control register can adjust the contrast of LCD.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	LCDM3	LCDM2	LCDM1	LCDM0	R/W	LCD contrast adjustment register

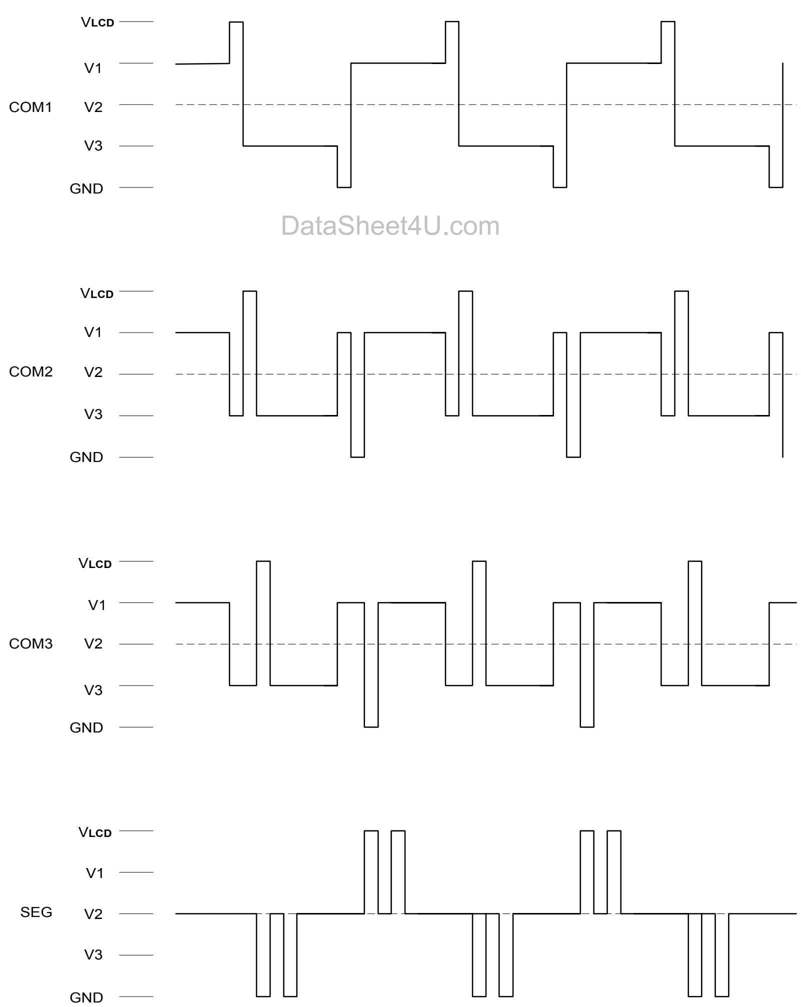
LCDM3	LCDM2	LCDM1	LCDM0	VLCD (V) (V_{DD} = 3.0V)			
				PUMP_ON = 1 (Bit3 of $13)		PUMP_ON = 0 (Bit3 of $13)	
				1/4 Bias	1/5 Bias	1/4 Bias	1/5 Bias
0	0	0	0	2.77	3.00	1.85	2.00
0	0	0	1	2.84	3.07	1.89	2.05
0	0	1	0	2.92	3.14	1.95	2.09
0	0	1	1	3.00	3.21	2.00	2.14
0	1	0	0	3.09	3.29	2.06	2.19
0	1	0	1	3.18	3.37	2.12	2.25
0	1	1	0	3.27 (default)	3.46 (default)	2.18 (default)	2.31 (default)
0	1	1	1	3.37	3.55	2.25	2.37
1	0	0	0	3.48	3.65	2.32	2.43
1	0	0	1	3.60	3.75	2.40	2.50
1	0	1	0	3.72	3.86	2.48	2.57
1	0	1	1	3.86	3.97	2.57	2.65
1	1	0	0	4.00	4.09	2.67	2.73
1	1	0	1	4.15	4.22	2.77	2.81
1	1	1	0	4.32	4.35	2.88	2.90
1	1	1	1	4.50	4.50	3.00	3.00

8.4. LCD Waveform





Example: 1/8 duty, 1/4 bias



9. Watchdog Timer (WDT)

The watchdog timer is a countdown counter, and its clock source is an independent built-in RC oscillator, so that it will always run even in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($2C bit2 - bit0) are used to select different overflow frequency. The watchdog timer overflow flag ($2C bit3) will be automatically set to "1" by hardware when the watchdog timer overflows. By reading or writing the system register $2C, the watchdog timer should re-count before the overflow happens.

System Register $2C: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2C	WDT	WT2	WT1	WT0	W R	Bit2 - Bit0: Watchdog timer control bits Bit3: Watchdog timer overflow flag (read only)
	X	0	0	0	W	Watchdog timer overflow period is about 1433.6ms
	X	0	0	1	W	Watchdog timer overflow period is about 358.4ms
	X	0	1	0	W	Watchdog timer overflow period is about 89.6ms
	X	0	1	1	W	Watchdog timer overflow period is about 44.8ms
	X	1	0	0	W	Watchdog timer overflow period is about 22.4ms
	X	1	0	1	W	Watchdog timer overflow period is about 11.2ms
	X	1	1	0	W	Watchdog timer overflow period is about 2.8ms
	X	1	1	1	W	Watchdog timer overflow period is about 0.7ms
	0	X	X	X	R	No watchdog timer overflow resets
	1	X	X	X	R	Watchdog timer overflows, WDT reset happens

10. Interrupt

Four interrupt sources are available on SH67K93:

- External interrupt ($\overline{INT0}$)
- Timer0 interrupt
- Timer1 interrupt
- Port's falling edge detection interrupt ($\overline{INT1}$)

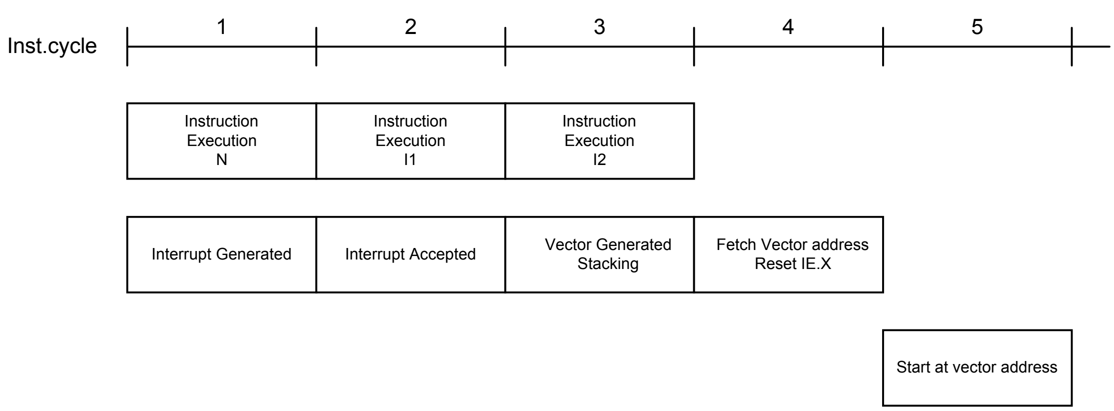
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to "0" at initialization by the chip reset.

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Reamrks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt Control Regiser 1: Enable/0: Disable
$01	IRQEX0	IRQT0	IRQT1	IRQP	R/W	Interrupt Flag Regiser 1: Request/0: No request
$16	PA0_PEN	PL/PH	INT0_FSKN0	INT0_PA0	R/W	FSK receiver and PORTA0 interrupt mode control register
$17	FSKIN_STAT	IRQ_FSKTX	IRQ_FSKIN	IRQ_PA0	R/W	FSKIN status register FSK generator/FSK receiver/PORTA0 Interrupt Flag Regiser
$2F	CAS/DTMF	-	-	INT0_FSKIN1	R/W	FSK receiver interrupt mode control register

When IEx is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are cleared to "0" automatically, so when IRQx is 1 and IEx is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

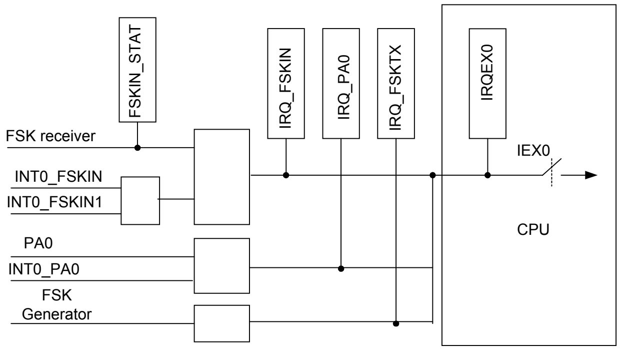
During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt ($\overline{\text{INT0}}$)

External Interrupt 0 is shared with the PORTA.0, the FSK receiver and FSK Generator output, falling or rising edge active. When the bit 3 of the register $0 (IEX) is set to "1", the interrupt0 is enabled. For PORTA.0, the interrupt will occur only at INPUT mode.

When an interrupt0 occurred, one must read the IRQPA0, IRQ_FSKIN and IRQ_FSKTX first to judge whether the interrupt source is from PORTA.0, the FSK receiver or from the FSK Generator output.

IEX:	Interrupt0 on/off switch. 0: disable.	 1: Enable
IRQEX0:	Interrupt0 interrupt request 0: No request	 1: Request
IRQ_PA0:	PA0 interrupt request 0: No request	 1: Request
IRQ_FSKIN:	FSK receiver interrupt request 0: No request	 1: Request
IRQ_FSKTX:	FSK Generator interrupt request 0: the transmission is not completed 1: the transmission is completed	
INT0_FSKIN0:	edge trigger type control bit of FSK receiver (one source of Interrupt0) while INT0_FSKIN1 = 0 0: falling edge type	 1: rising edge type
INT0_FSKIN1:	edge trigger type of FSK receiver (one source of Interrupt0) 0: edge type is set by INT0_FSKIN0 1: Dual edges interrupt type (falling/rising) regardless of INT0_FSKIN0	
INT0_PA0:	edge trigger type of PORTA.0 (one source of Interrupt0) 0: falling edge type	 1: rising edge type
FSKIN_STAT:	the status bit of FSKIN level (output of FSK receiver) 1: the source of FSKIN is high level 0: the source of FSKIN is low level	



Timer Interrupt

The input clocks of Timer0 and Timer1 are based on system clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1 = 1), If the interrupt enable flag is enabled (IET0 or IET1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

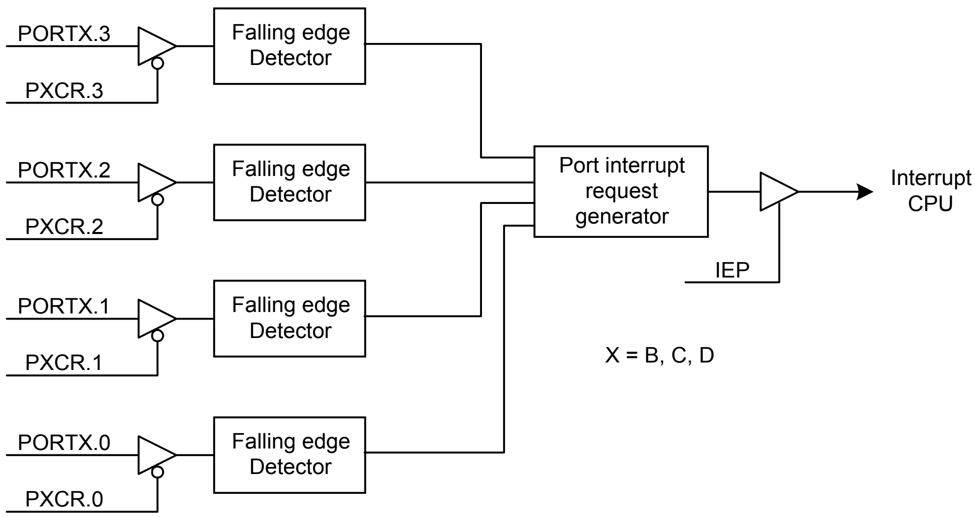
Port Falling Edge Interrupt ($\overline{\text{INT1}}$)

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

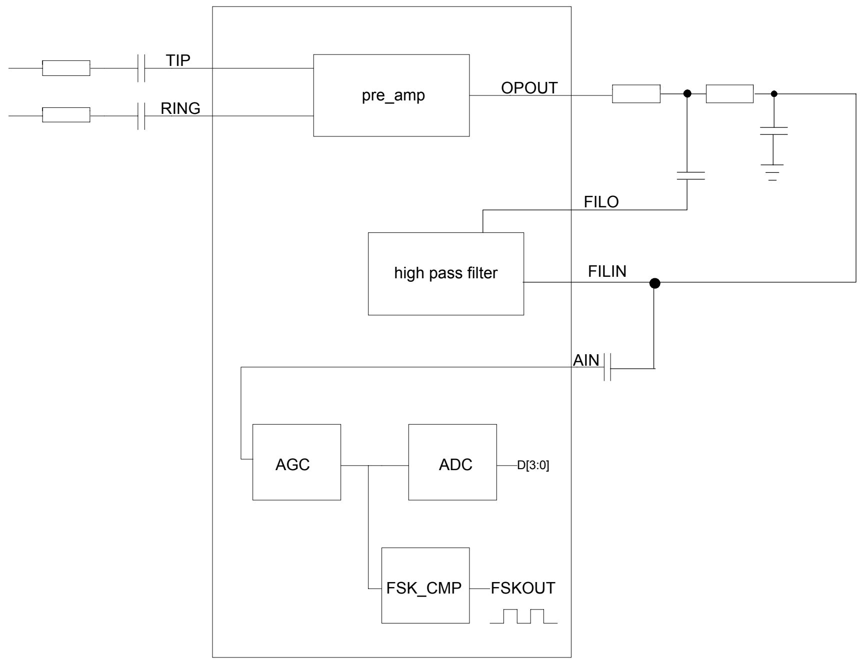
Any one of PORTB, PORTC and PORTD input pad transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pads have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

When the PORTB shared as Caller ID interface, the PORTB interrupt will be disabled.

When the PORTC, PORTD shared as segment output, the PORTC, PORTD interrupt will be disabled.



11. CID Interface



11.1. DTMF/FSKGenerator (Using Condition: System Clock is 3.579545MHz Crystal)

DTMF Generator

The SH67K93 has a built-in DTMF generator.

The DTMF Generator control register and data register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$26	FSK_ON	FSK/DTMF	TONE_COL	TONE_ROW	R/W	DTMF/FSK Generator control register
$29	FSK_D3/TGD3	FSK_D2/TGD2	FSK_D1/TGD1	FSK_D0/TGD0	R/W	Low nibble data of FSK Generator Data of DTMF Generator

FSK_ON: DTMF/FSK Generator power on/off switch
0: DTMF/FSK Generator power off 1: DTMF/FSK Generator power on

FSK/DTMF: DTMF/FSK Generator select bit
0: DTMF Generator Enable, FSK Generator disable
1: DTMF Generator disable, FSK Generator Enable

TONE_COL: Column signal output control
0: disable 1: Enable

TONE_ROW: ROW signal output control
0: disable 1: Enable

TGD3 - 0: DTMF Generator Data register

This chip provides a dual tone multi-frequency (DTMF) tone generation circuit. The DTMF signal consists of two sine waves with which to access the switching system. The following table shows the relationship between the key pressed and its dual tone frequencies.

COL ROW	1209Hz	1336Hz	1477Hz	1633Hz
697Hz	1	2	3	A
770Hz	4	5	6	B
852Hz	7	8	9	C
941Hz	#	0	∗	D

The DTMF generator employs two D/A converters, which can generate two separated single-tone signals, low-frequency group for Row and high-frequency group for Column. These two signals would finally mix together to produce a Dual Tone Multi Frequency Signal. Each single-tone signal consists of 32-level waveform that guarantees low distortion signal quality.

A write-only DTMF Generator control register controls DTMF generator, and the signal data would be prepared in this register. The row and column frequency of DTMF corresponding to each keypad and digits are listed in the following table. The output DTMF frequency is controlled by the tone generator data bit TGD3 - TGD0 in DTMF data register. The relationship between TGD bit and output DTMF frequency are also listed in the following table.

DTMF Generator data Register: DTMF_data “1”

TGD3	TGD2	TGD1	TGD0	Output Frequency	Digit
0	1	1	1	941 + 1336Hz	“0”
0	0	0	0	697 + 1209Hz	“1”
0	1	0	0	697 + 1336Hz	“2”
1	0	0	0	697 + 1477Hz	“3”
0	0	0	1	770 + 1209Hz	“4”
0	1	0	1	770 + 1336Hz	“5”
1	0	0	1	770 + 1477Hz	“6”
0	0	1	0	852 + 1209Hz	“7”
0	1	1	0	852 + 1336Hz	“8”
1	0	1	0	852 + 1477Hz	“9”
0	0	1	1	941 + 1209Hz	“*”
1	0	1	1	941 + 1477Hz	“#”
1	1	0	0	697 + 1633Hz	“A”
1	1	0	1	770 + 1633Hz	“B”
1	1	1	0	852 + 1633Hz	“C”
1	1	1	1	941 + 1633Hz	“D”

FSK Generator

The SH67K93 has a built-in FSK generator.

The FSK Generator control register and data register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$26	FSK_ON	FSK/DTMF	TONE_COL	TONE_ROW	R/W	FSK/DTMF Generator control register
$27	ADCC	FSK_MD	FSK_PRE	FSK_TXEN	R/W	FSK Generator mode control register
$28	FSK_D7	FSK_D6	FSK_D5	FSK_D4	R/W	FSK/DTMF Generator data register
$29	FSK_D3/TGD3	FSK_D2/TGD2	FSK_D1/TGD1	FSK_D0/TGD0		

FSK_MD: FSK standard select bit
1: Select Bell 202 standard
0: Select V.23 standard

FSK_PRE: 1: Indicate FSK_DATA is preamble data
0: Indicate FSK_DATA is message data

FSK_TXEN: 1: Start transmiting FSK signal after FSK_DATA is ready
0: unused

FSK_D7 - 0: FSK data to be transmitied

The SH67K93 provides a programmable FSK generator that satisfies the standard of Bell202 and V.23. Setting the FSK_MD bit in FSK control register chooses Bell202 mode as well as clear of this bit chooses V.23 mode.

	Mark ‘1’	Space ‘0’
Bell202	1200 Hz	2200 Hz
V.23	1300 Hz	2100 Hz

In these two standards, FSK baud rate is 1200 baud. The baud rate clocks automatically enabled before transmiting FSK signal.

The transmitted data is stored in FSK_TXDATA register. Then set FSK_TXEN bit to start to transmit the 8 bit data. After all the 8 bit data are transmitted, the FSK Generator will generate an interrupt if IEX0 in IE register is set, IRQ_FSKTX, to indicate it is ready for transmiting next byte data. Before next FSK_TXEN bit is set, the FSK modulator will transmit mark signal or the data stored in FSK_TXDATA register repeatedly until FSK Generator is disabled or next FSK data is ready to be transmitted. The FSK_PRE bit in FSK_CTRL register indicates whether the data in FSK_TXDATA register is preamble or real data. If FSK_PRE bit is set to 1, the data stored in FSK_TXDATA register is preamble and the FSK modulator will transmit FSK_TXDATA repeatedly. If this bit is clear to 0, the mark signal will be transmitted during two FSK data. The FSK_PRE bit also serves another function that it can control the insertion of start and stop bit in transmiting FSK signal. If the preamble FSK signal is transmitted, the FSK modulator will not insert the start and stop bit. While the FSK modulator will insert start and stop bit automatically when FSK_PRE bit is clear.

Before FSK_ON is set, please make sure that the FSK_TXEN is cleared, and FSK_PRE is already set correctly.

11.2. Amplifier, ADC and Digital Filter

The SH67K93 has a built-in Amplifier, ADC and Digital filter.
The Amplifier, ADC and Digital filter control register and data register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$25	DF_F	DC2	DC1	DC0	R/W	Digital Filter control register
$27	ADCC	FSK_MD	FSK_PRE	FSK_TXEN	R/W	ADC conversion complete flag
$2A	AMP_ON	AGC_ON	DFIL_ON	ADC_ON	R/W	AMP/AGC/DF/ADC control register
$2B	GCD3	GCD2	GCD1	GCD0	W	GAIN register
	ADCD3	ADCD2	ADCD1	ADCD0	R	ADC conversion result
$2D	CMPW1	CMPW0	-	O/S3	R/W	Comparator voltage window control register
$1780	-	DFTA14	DFT113	DFTA12	R/W	DF table start address register
$1781	DFTA11	DFTA10	DFTA9	DFTA8		
$1782	DFTA7	DFTA6	DFTA5	DFTA4		
$1783	DFTA3	DFTA2	DFTA1	DFTA0		
$1784	D11	D10	D9	D8	R/W	Sample Dot-number register
$1785	D7	D6	D5	D4		
$1786	D3	D2	D1	D0		

AMP_ON: Pre-Amplifier, filter, AGC, FSK comparator power on/off switch
0: power OFF 1: power ON

AGC_ON: AGC mode control
0: manual mode 1: Auto mode

DFIL_ON: Digital filter control
0: Digital filter OFF
1: Digital filter ON, the digital filter will calculate the input data (output by ADC) when internal sample rate timer overflows.

DF_F: Digital filter calculation is finished flag bit
0: Digital filter calculation is complete
1: Digital filter calculation is in process

DC2 - 0: the number of frequence of Digital filter
If Digital filter calculation is for DTMF, please write 07H
If Digital filter calculation is for CAS, please write 03H

D11 - 0: the number of sample dots for Digital filter

CMPW1, CMPW0: The voltage window of schemitt-trigger of FSK comparator control bits

DFTA14 - 0: Digital filter data table start address

ADCON: 1: 4-bit ADC enable;
0: 4-bit ADC disable

ADCC: 1: ADCC is set each time when a conversion is completed.
0: ADCC is cleared by reading the result data register or writing the status/control register.

Differential Input Amplifier gain Control Register table:

GCR3	GCR2	GCR1	GCR0	dBm	Gain
0	0	0	0	3	1
0	0	0	1	0	1.5
0	0	1	0	-3	2
0	0	1	1	-6	3
0	1	0	0	-9	4
0	1	0	1	-12	6
0	1	1	0	-15	8
0	1	1	1	-18	12
1	0	0	0	-21	16
1	0	0	1	-24	24
1	0	1	0	-27	32
1	0	1	1	-30	48
1	1	0	0	-33	64
1	1	0	1	-36	96
1	1	1	0	-39	128
1	1	1	1	-42	192

Schemitt-trigger voltage windows control table:

CMPW1	CMPW0	Voltage Window
0	0	0mV
0	1	20mV
1	0	50mV
1	1	200mV

12. HALT and STOP Mode

After the execution of HALT instruction, SH67K93 will enter HALT mode.
In HALT mode, CPU will stop operating. But peripheral circuit (Timer, Base timer, DAC, AGC, ADC, FSK CMP) will keep the status.

After the execution of STOP instruction, SH67K93 will enter STOP mode.

In STOP mode, the whole chip (including oscillator) will stop operating.

In HALT mode, SH67K93 can be waked up if any interrupt occurs.

In STOP mode, SH67K93 can be waked up if port interrupt occurs (exclude the FSKIN and FSK generator interrupt).

When CPU is awaked from the HALT/STOP by any initial source, it will execute the relevant initial serve subroutine first and then the instruction next to HALT/STOP will be executed.

13. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

13.1 Power-on Reset

Warm-up time interval:
(1)In RC oscillator mode, the warm-up counter prescaler divide ratio is $/2^7$ (128).
(2)In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $/2^{12}$ (4096).

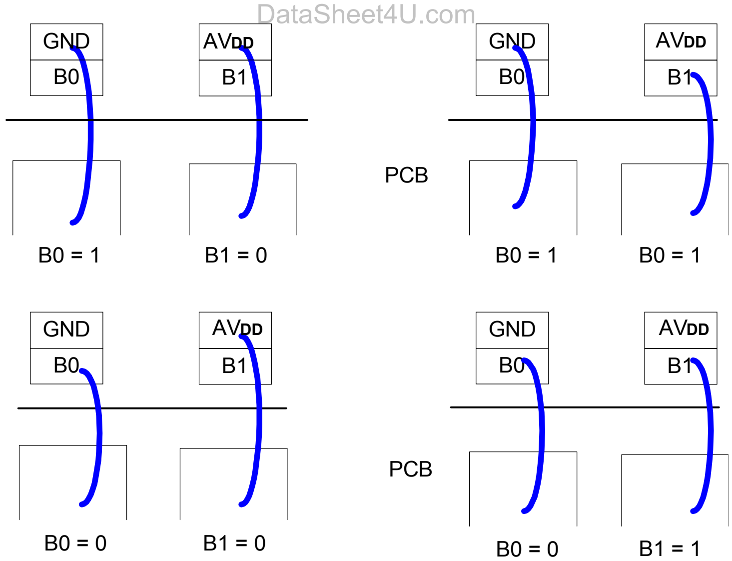
13.2. Wake-up from STOP Mode

Warm-up time interval:
(1)In RC oscillator mode, the warm-up counter prescaler divide ratio is $/2^{12}$ (4096).
(2)In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $/2^{12}$ (4096).
The clock source of warm-up timer is system clock.
System clock is unchanged when system returns from STOP mode.

14. Bonding Option

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	-	-	B0	B1	R	B0, B1: bonding option
	X	X	0	1	R	B0 bond to GND & B1 bond to AV_{DD}
	X	X	0	0	R	B0 bond to GND
	X	X	1	1	R	B1 bond to AV_{DD}
	X	X	1	0	R	Default bonding option



Up to 4 different bonding options are possible for user's needs. The chip's program has 4 different program flows that vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

15. Code Option

C: OSC clock source
0: 32.768kHz crystal
1: 262kHz RC

L: OSCX clock source
0: 3.58MHz ceramic/3.579545MHz crystal
1: 1.8MHz RC

WD: Watchdog control bit
00: WDT disable
01: WDT Enable and stop in STOP mode
10: WDT Enable and stop in STOP mode
11: WDT Enable and no stop in STOP mode

K: LCD voltage Pump clock frequency select
0: 4kHz (default)
1: 8kHz

T: CAS function control option
0: Enable (default)
1: Disable

16. Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

16.1. Arithmetic and Logical Instruction

16.1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC[3], AC[0] -> CY; AC shift right one bit	CY

16.1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

16.1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub	CY

16.2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

16.3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC +1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- lll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Rating*

DC Supply Voltage . . . . -0.3V to +3.6V

Input Voltage . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -10℃ to +70℃

Storage Temperature . . . . -55℃ to +125℃

*Comments

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, fosc = 32.768kHz, OSCX is turned off, unless otherwise specified)

Parameter	Symbol	Min.	Type	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.4	3	3.6	V	
Operating Current	I_{OP}	-	10	20	μA	All output pads unload execute NOP instruction exclude LCD bias current, LPD off, WDT off AGC/ADC/FSK_CMP/Pre-amplifier OFF
Standby Current	I_{SB1}	-	3	6	μA	All output pads unload (HALT mode) exclude LCD Bias current, LPD off WDT off AGC, ADC, FSK_CMP, Pre-amplifier OFF
Sleep Current	I_{SB2}	-	-	1	μA	All output pads unload (STOP mode), LCD off, LPD off WDT off, AGC, ADC, FSK_CMP, Pre-amplifier OFF
WDT current	I_{WDT}	-	10	13	μA	WDT current
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD} + 0.3	V	PORTA.3 - 1, PORTB - PORTF
Input Low Voltage	V_{IL1}	-0.3	-	0.3 X V_{DD}	V	PORTA.3 - 1, PORTB - PORTF
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$ (Schmitt trigger input)
Input Low Voltage	V_{IL2}	-0.3		0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$ (Schmitt trigger input)
Output high voltage	V_{OH1}	0.7 X V_{DD}	-	-	V	PORTA.3 - 0, PORTB (I_{OH} = -2mA)
Output low voltage	V_{OL1}	-	-	0.8	V	PORTA.2 - 0, PORTB (I_{OL} = 2mA)
Output high voltage	V_{OH2}	V_{DD} - 0.6	-	-	V	PORTC, PORTD, PORTE, PORTF (I_{OH} = -1mA)
Output low voltage	V_{OL2}	-	-	0.8	V	PORTC, PORTD, PORTE, PORTF (I_{OH} = 1mA)
Output low voltage	V_{OL3}	-	-	0.4	V	PORTA.3 (I_{OL} = 10mA)
LCD Voltage Divider Resistor	R_{LCD}	-	275	-	kΩ	
LCD Driving on resistor	R_{ON}	-	5	-	kΩ	LCD COM1 - 16, LCD SEG1 - 50, the voltage variation of V1, V2, V3, V4 is less than 0.2V
Pull high resistance	R_{OH}	-	200	-	kΩ	PORTA - F (I_{OH} = -10μA)
Pull low resistance	R_{OL}	-	200	-	kΩ	PORTA.0 (I_{OH} = 10μA)
LCD lighting	I_{DD}	-	30	40	μA	V_{DD} = 3V, LCD Pump Enable, no glass load, exclude CPU core operation current

Analog Electrical Characteristics (T_A = -10 to 70°C, V_{DD} = 3.0V, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Single Row Tone Output Amplitude	V_{OR}	590	660	730	mVp-p	With 100kΩ pull-high resistor
Single Column Tone Output Amplitude	V_{OC}	795	870	945	mVp-p	With 100kΩ pull-high resistor
DTMF output distortion	DIS%		2	5	%	With 100kΩ pull-high resistor
DTMF pre-emphasis	Twist	1	2	3	dB	With 100kΩ pull-high resistor
Tip/Ring input impedance	R_{IN1}	400	500	600	kΩ	Input frequency = 0
Input sensitivity of Tip and Ring	PSIG	-46			dBm	SNR = 15dB, GCR = 1110
Signal reject level	SRL	-51			dBm	GCR = 1110
DTMF sensitivity	SD	-38		+1	dBm	
CAS sensitivity	SC	-38		-11	dBm	
Frequency response of the Band Pass Filter			-54 -3 0 0 -2		dB	≤60Hz 550Hz 1200Hz 2200Hz 3300Hz

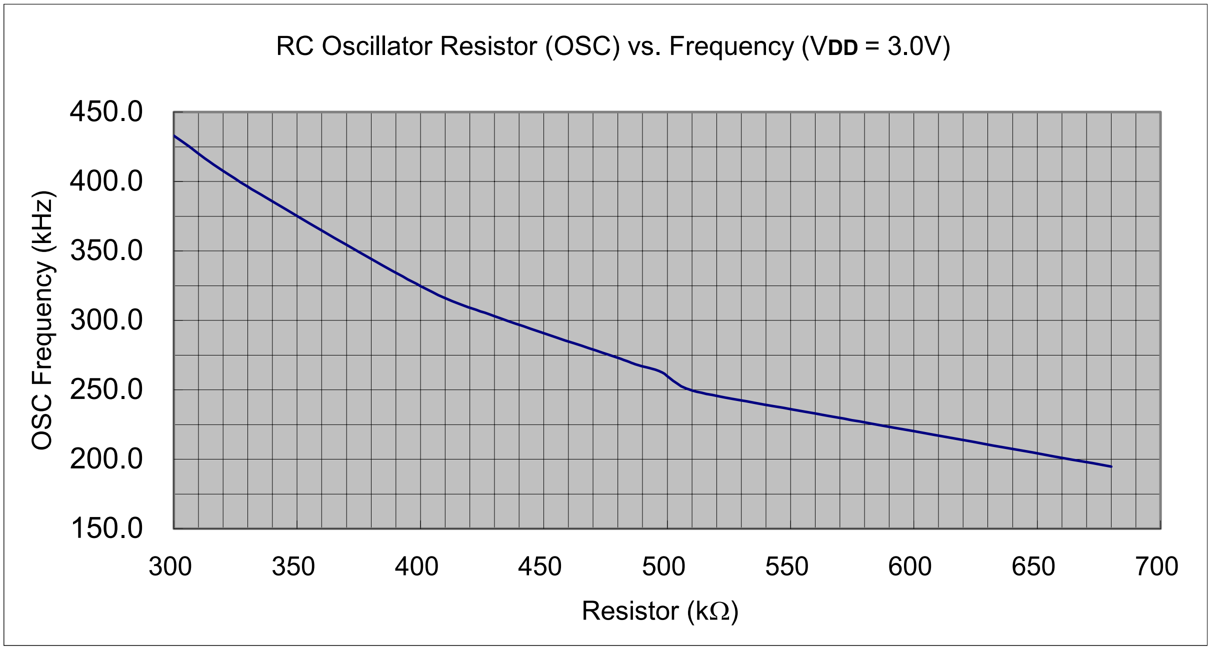
AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, **fosc** = 32.768kHz, unless otherwise specified)

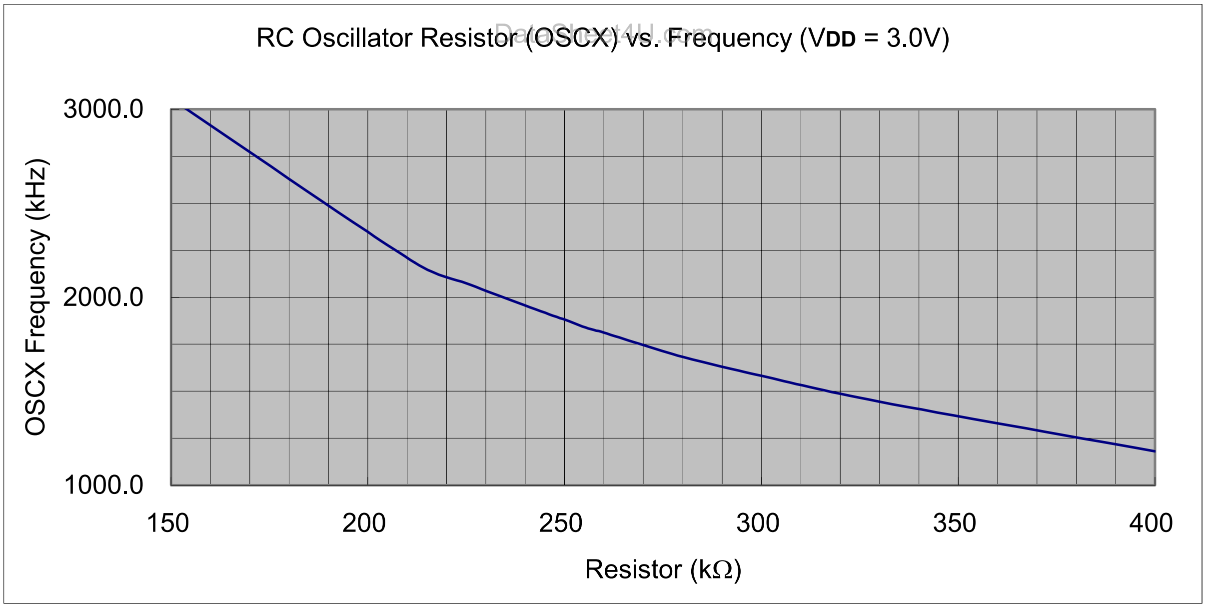
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	2	5	s	32.768kHz Crystal Oscillator
Frequency Stability	|Δf|/f	-	-	1	PPM	[f(3.0) - f(2.5)]/f(3.0), 32.768kHz Crystal Oscillator

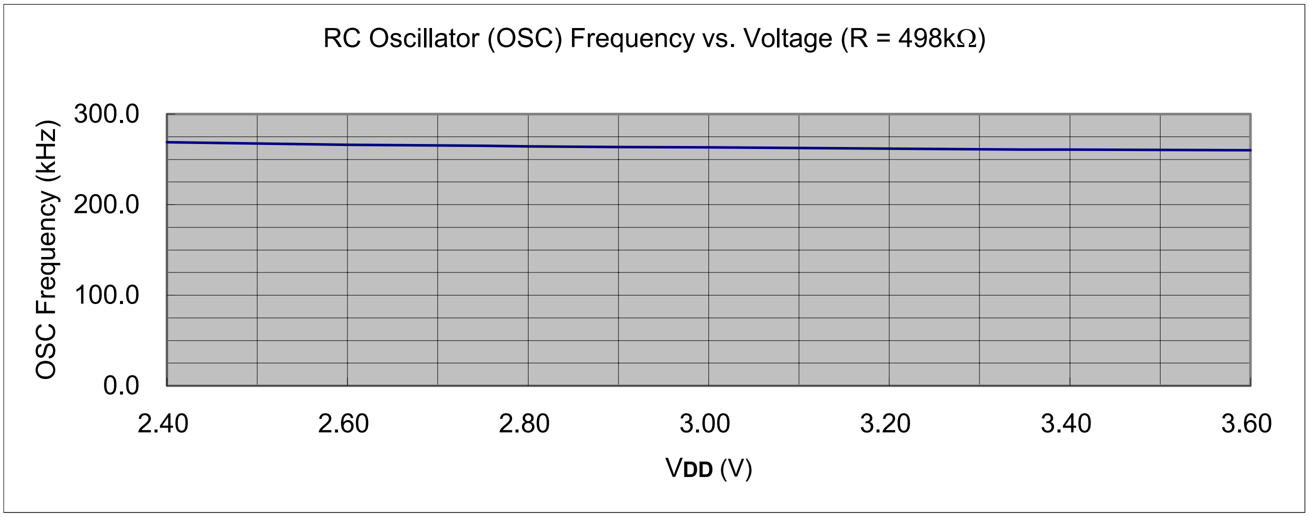
AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, **fosc** = 262kHz, **foscx** stop, unless otherwise specified)

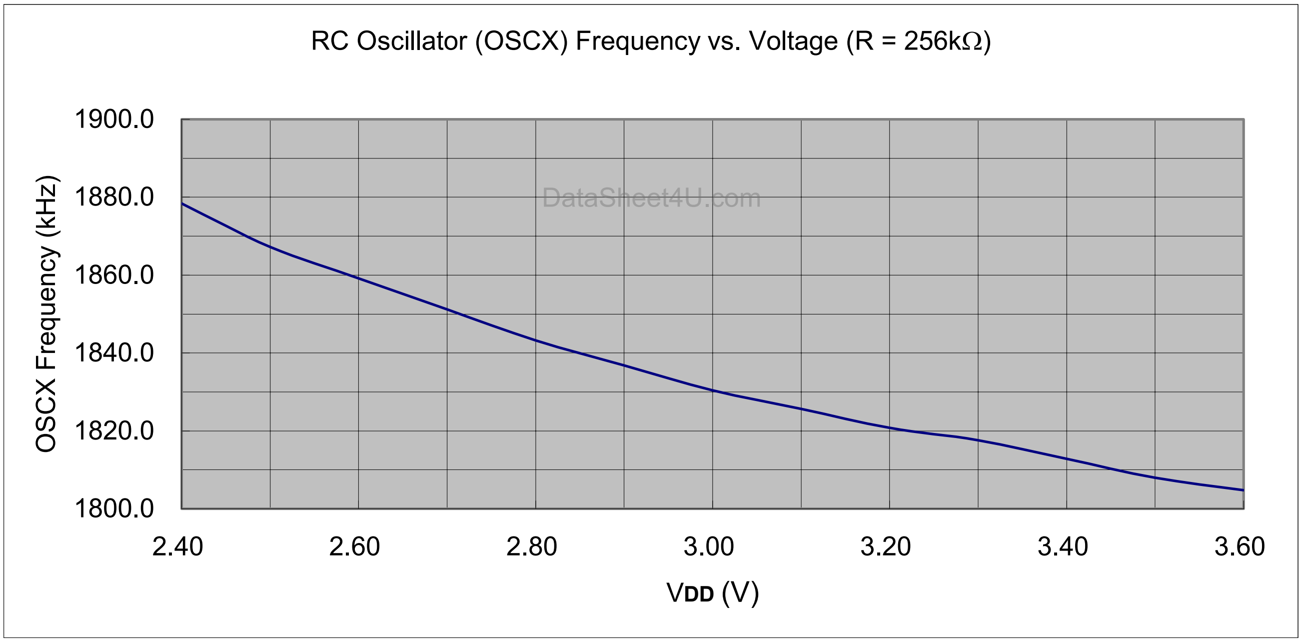
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	-	100	μs	262kHz RC Oscillator
Frequency Stability	|Δf|/f	-	-	10	%	[f(3.0) - f(2.5)]/f(3.0), Bias resistance accuracy within 1%

RC Oscillator Characteristics Graphs (for reference only)

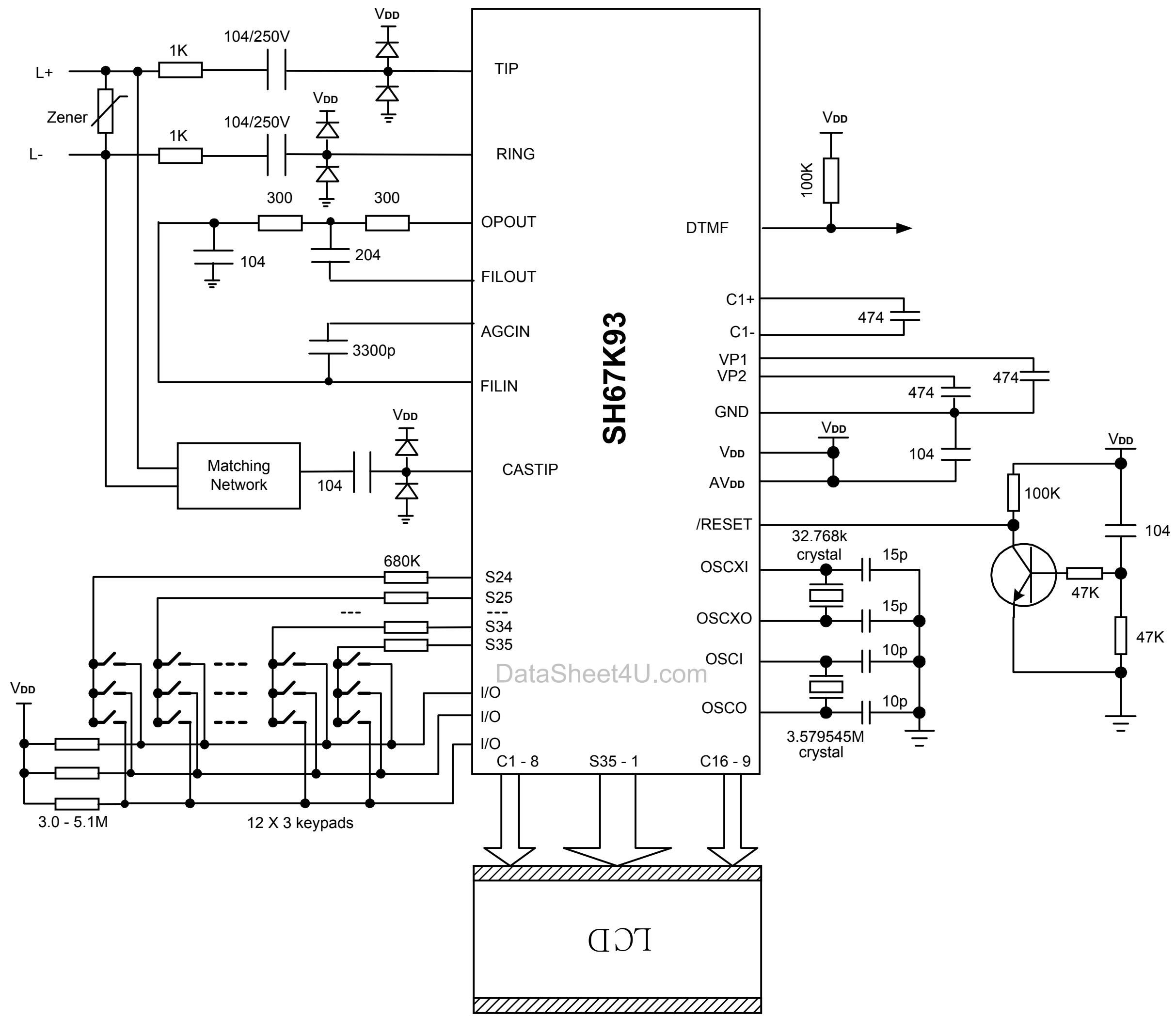




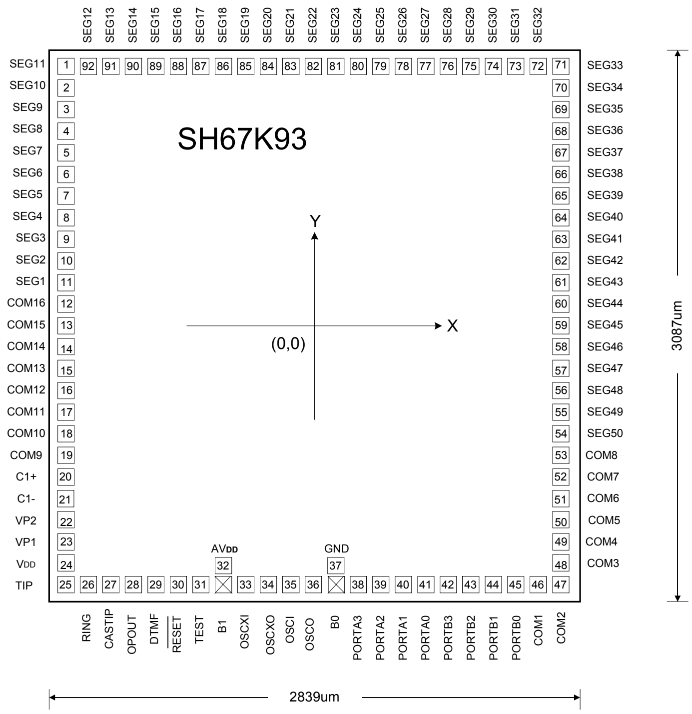

RC Oscillator (OSC) Frequency vs. Voltage (R = 498kΩ)
OSC Frequency (kHz)
300.0
200.0
100.0
0.0
2.40
2.60
2.80
3.00
3.20
3.40
3.60
VDD (V)


RC Oscillator (OSCX) Frequency vs. Voltage (R = 256kΩ)
OSCX Frequency (kHz)
1900.0
1880.0
1860.0
1840.0
1820.0
1800.0
2.40
2.60
2.80
3.00
3.20
3.40
3.60
VDD (V)

Application Circuit (for reference only)



Bonding Diagram



Pad Location

unit:μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG11	-1285.4	1410	21	C1-	-1285.4	-900
2	SEG10	-1285.4	1280	22	VP2	-1285.4	-1020
3	SEG9	-1285.4	1150	23	VP1	-1285.4	-1150
4	SEG8	-1285.4	1020	24	VDD	-1285.4	-1280
5	SEG7	-1285.4	900	25	TIP	-1285.4	-1410
6	SEG6	-1285.4	780	26	RING	-1155.4	-1410
7	SEG5	-1285.4	660	27	CASTIP	-1025.4	-1410
8	SEG4	-1285.4	550	28	OPOUT	-905.4	-1410
9	SEG3	-1285.4	440	29	DTMF	-785.4	-1410
10	SEG2	-1285.4	330	30	$\overline{\text{RESET}}$	-665.4	-1410
11	SEG1	-1285.4	220	31	TEST	-555.4	-1410
12	COM16	-1285.4	110	Bonding Option	B1	-440	-1410
13	COM15	-1285.4	0	32	AVDD	-440	-1314
14	COM14	-1285.4	-110	33	OSCXI	-330	-1410
15	COM13	-1285.4	-220	34	OSCXO	-220	-1410
16	COM12	-1285.4	-330	35	OSCI	-110	-1410
17	COM11	-1285.4	-440	36	OSCO	0	-1410
18	COM10	-1285.4	-550	Bonding Option	B0	110	-1410
19	COM9	-1285.4	-660	37	GND	110	-1314
20	C1+	-1285.4	-780	38	PORTA3	225.4	-1410

Pad Location (Continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
39	PORTA2	335.4	-1410	66	SEG38	1285.4	779.65
40	PORTA1	445.4	-1410	67	SEG37	1285.4	900
41	PORTA0	555.4	-1410	68	SEG36	1285.4	1020
42	PORTB3	665.4	-1410	69	SEG35	1285.4	1150
43	PORTB2	785.4	-1410	70	SEG34	1285.4	1280
44	PORTB1	905.4	-1410	71	SEG33	1285.4	1410
45	PORTB0	1025.4	-1410	72	SEG32	1155.4	1410
46	COM1	1155.4	-1410	73	SEG31	1025.4	1410
47	COM2	1285.4	-1410	74	SEG30	905.4	1410
48	COM3	1285.4	-1280	75	SEG29	785.4	1410
49	COM4	1285.4	-1150	76	SEG28	660	1410
50	COM5	1285.4	-1020	77	SEG27	550	1410
51	COM6	1285.4	-900	78	SEG26	440	1410
52	COM7	1285.4	-780	79	SEG25	330	1410
53	COM8	1285.4	-660	80	SEG24	220	1410
54	SEG50	1285.4	-549.7	81	SEG23	110	1410
55	SEG49	1285.4	-440	82	SEG22	0	1410
56	SEG48	1285.4	-330	83	SEG21	-110	1410
57	SEG47	1285.4	-220	84	SEG20	-220	1410
58	SEG46	1285.4	-110	85	SEG19	-330	1410
59	SEG45	1285.4	0	86	SEG18	-440	1410
60	SEG44	1285.4	110	87	SEG17	-550	1410
61	SEG43	1285.4	220	88	SEG16	-665.4	1410
62	SEG42	1285.4	330	89	SEG15	-785.4	1410
63	SEG41	1285.4	440	90	SEG14	-905.4	1410
64	SEG40	1285.4	550	91	SEG13	-1025.4	1410
65	SEG39	1285.4	660	92	SEG12	-1155.4	1410

Ordering Information

Part No.	Package
SH67K93	CHIP

Data Sheet Revision History

Version	Content	Date
1.0	Original	Dec. 2004