1:8 Time Division Demultiplexer

Serial to Parallel Converter • 1 Gbit/s NRZ Data Rate

10G PicoLogic™ Family

FEATURES

- Complete single chip demultiplexer system
- DC to 1 Gbit/s operation
- 1:8 and 1:4 operating modes
- On-chip frame synchronization circuitry
- Parallel or ripple data output modes
- Programmable 8-phase clock ÷ 8 output
- 10G PicoLogic™ and ECL compatible
- Cascadable to 1:16, 1:32, 1:64, and beyond with on chip synchronization circuitry
- Fully compatible with companion 10G040A 8:1 multiplexer and 16G040 clock recovery circuit
- High speed differential input stage
- Available in 40 pin C-leaded or leadless chip carriers or in die form

APPLICATIONS

- High data rate fiber optic and microwave receivers/ transmitters and drop-and-insert systems
- High capacity local area networks
- Digital RF memory
- Board-to-board or computer-to-peripheral data communications
- High speed test equipment response vector deserialization

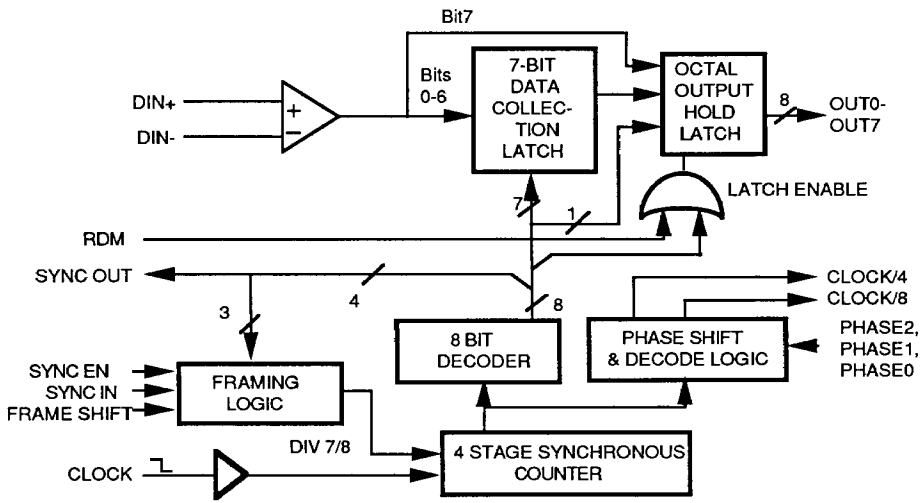
FUNCTIONAL DESCRIPTION

Together with its companion 10G040A 8:1 multiplexer, the 10G041A Time Division Demultiplexer extends fiber optic digital data transmission speeds to 1 Gbps NRZ. The device is capable of serial-to-parallel data deserialization at rates extending from DC to 1 Gbps, with maximum power dissipation of 1.9 W. The 10G041A is a complete, single-chip demultiplexing subsystem containing on-chip frame synchronization circuitry which simplifies fiber optic receiver design while minimizing high speed parts count. It features a CLOCK/8 output with digitally programmable phase which provides easy synchronization between the 10G041A and logic connected to its 8 outputs. It can be operated in a 1:4 mode and can be cascaded to higher order DEMUX ratios of 1:16, 1:32 or 1:64.

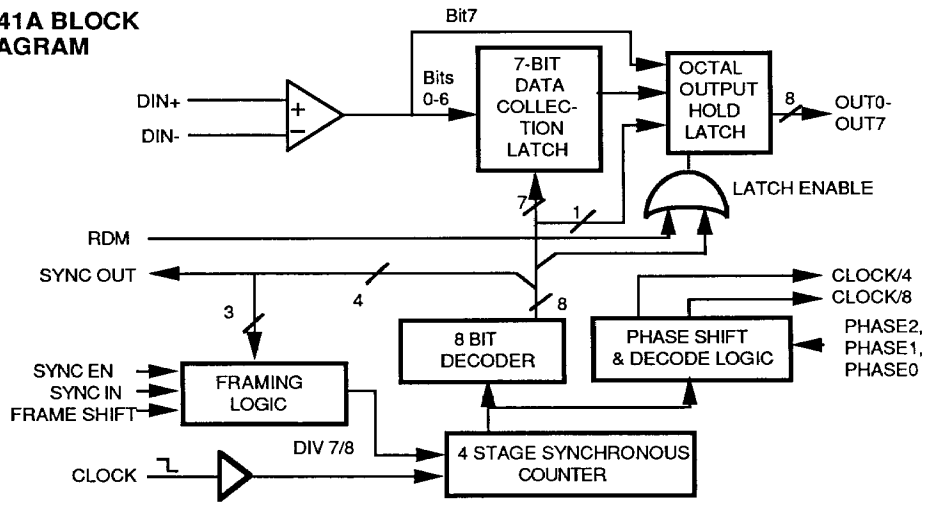
10G041A ORDERING INFORMATION

PACKAGE TYPE	SPEED	
	1.0 GHz	750 MHz
Leadless CC	10G041A-3L	10G041A-4L
C- Leaded CC	10G041A-3C	10G041A-4C
Dice		10G041A-4X

10G041A BLOCK DIAGRAM



10G041A BLOCK DIAGRAM



PIN DESCRIPTIONS

Signal Pins

OUT0 through OUT7
Demultiplexer data output pins.

DIN+, DIN-
Complementary, high speed differential input pins. These inputs should either be driven from differential signals or the unused input must be tied to reference threshold from driving device (nominally -1.3 volts)

SYNC OUT
This output pin is used when cascading multiple 10G041As for higher order DEMUX ratios. In combination with the SYNC IN input pin, SYNC OUT is used to acheive automatic synchronization among a group of cascaded demultiplexers. SYNC OUT provides a positive sync pulse of one CLOCK period duration during the time that data on output pin OUT1 is valid.

SYNC IN
This input pin is used to receive the SYNC OUT pulse from another 10G041A when multiple demultiplexers are cascaded. Tie low (to VSS) when not used.

FRAME SHIFT
Each time a low-to-high transition is applied to FRAME SHIFT, the 10G041A's internal counter will divide by seven instead of eight for one clock period, effectively shifting frame timing by one bit. Tie low (to VSS) when not used.

CLOCK
This is the high speed external clock input pin. The clock signal on this pin drives the 10G041A's internal sequencing counter. The input sampling rate on the DIN+ and DIN- inputs is equal to the CLOCK frequency.

CLOCK/4
This output pin provides a clock output equal to one quarter of the master CLOCK frequency. CLOCK/4 is used when cascading 10G041A's to achieve higher order demultiplexing ratios.

CLOCK/8
CLOCK/8 is an output clock equal to one eighth of the master CLOCK frequency. CLOCK/8 will normally be used to clock external logic accepting data from the OUT0 to OUT7 output pins. The phase of CLOCK/8, with respect to output data timing, is digitally adjustable via the PHASE0,1,2 control pins.

Control Pins

RDM
The RDM (Ripple Data Mode) input pin selects whether the 10G041A provides output data on pins OUT0 through OUT7 in parallel or ripple data format. RDM = 0 (tied low to VSS) selects parallel mode; RDM = 1 (tied high to VDDL) selects ripple mode.

PHASE0, PHASE1, PHASE2
These three input pins are used to select one of 8 phases of the CLOCK/8 output.

SYNC EN
This input pin enables or disables the SYNC IN signal input. The SYNC IN pin is enabled when SYNC EN is tied high (to VDDL); SYNC IN is disabled when SYNC EN is tied low (to VSS). When not used, SYNC EN must be tied low or SYNC IN must be tied high. SYNC EN can also be used to shift frame timing in a manner similar to the FRAME SHIFT input (see text).

VBB
Reference input to the 10G041A's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G041A from ECL. Connect to the VBBS pin when the 10G041A is driven from PicoLogic. This pin may not be left unconnected.

VBBS
PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic.

Power Supply Pins

VDDO, VDDL
These pins are the ground (0V) connections for the output driver and internal logic circuitry, respectively.

VSS
-3.4V power supply.

VEE
-5.2V power supply.

VTTC
AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.

Functional Description, cont.

1.DATA INPUT (PINS DIN+, DIN-)
High speed serial data is sampled by the 10G041A on the differential input pins DIN+ and DIN-. The data is demultiplexed and output on the 8 output pins OUT0 through OUT7. Input data is sampled under control of an on-chip counter, which is incremented on each high-to-low transition of the CLOCK input. The rate at which data is output is therefore equal to one eighth of the CLOCK frequency. Data is always sampled and output in sequential order OUT0,OUT1, OUT2...OUT7, OUT0...
The DIN+ and DIN- inputs may be differentially driven, or if either is connected to -1.3V (or VBBS), the other may be driven from an ECL or PicoLogic compatible source.

2. DATA OUTPUT (PINS RDM and OUT0-OUT7)
Two output data modes, called parallel and ripple data modes, are supported by the 10G041A. Input pin RDM (Ripple Data Mode) selects the output mode. When RDM is tied high (to VDDL), ripple mode is enabled. For RDM tied low (to VSS), parallel mode is selected. In normal 1:8 operation, parallel mode is easiest to use since the outputs arrive simultaneously and remain stable for nearly seven bit times. The CLOCK/8 output of the DEMUX can be used to clock the interfacing ECL logic. Through adjustment of the CLOCK/8 phase using the control pins PHASE0, PHASE1 and PHASE2, it is possible to compensate for external logic and interconnect delays and guarantee maximum timing margin between the output data valid time of the DEMUX and the ECL input sample period. In some applications, ripple mode may be more appropriate such as when it is necessary to retain all demultiplexed bits except the bit being swallowed during a ÷7 "swallow" operation. Ripple mode is also required to achieve maximum data rate operation of a 1:4 demultiplexer.

In parallel mode, the 10G041A's counter and decode logic causes bits 0-6 to be loaded in successive positions of the seven bit data collection latch. When the counter reaches a count of seven, (the eighth count) indicating a full byte of data has been assembled in the data collection latch, the output hold latch is made transparent, and data from the data collection latch flows through the output hold latch to OUT0-OUT6. Simultaneously, the input data for bit 7 is being sampled by the demultiplexer and is passed around the data collection latch, and through the transparent hold latch, to OUT7 directly.

When the next high-to-low CLOCK edge is received, the output hold latch is made non-transparent, holding the data on all eight OUT pins constant until a new byte is assembled in the data collection latch. Because the output hold latch is updated during counter state 7 (bit time 7), output data should not be sampled during this time.

In ripple mode, the output hold latch is always in the transparent state. As bits received on the DIN pins are written into the data collection latch, the OUT pins are immediately updated. As a result, in ripple mode the outputs are staggered in time.

3. SUBMULTIPLE CLOCK OUTPUTS AND CONTROL PINS (CLOCK/8, CLOCK/4 AND PINS PHASE0,1,2)
The 10G041A provides CLOCK/4 and CLOCK/8 outputs to provide synchronous clocking to interfacing ECL output circuitry. In addition, they can be used in conjunction with a PLL to provide a stable, synthesized master CLOCK from an ECL clock. The output phase of the CLOCK/8 output is digitally programmable to any one of eight phases, each differing by one high speed CLOCK period in time. When the CLOCK/8 output is used to control interfacing data output logic, the user generally will program the CLOCK/8 phase necessary to achieve synchronization between the Demux and interfacing logic. This is accomplished by providing a 3-bit static code to input pins PHASE0, PHASE1 and PHASE2 and changing this code as necessary to achieve sync.

4. FRAME SYNCHRONIZATION AND TIMING
The 10G041A features a +7/+8 counter controlled by on-chip synchronization logic with FRAME SHIFT, SYNC EN and SYNC IN control inputs. Any of these three inputs can put the dual modulus counter into the +7 mode causing the device to effectively "swallow" one counter state or clock pulse. The swallowed clock pulse always corresponds to bit time 7 (counter state 7) meaning that the data bit ordinarily sampled and output during bit time 7 will be swallowed, or ignored. Also, in parallel mode, bit time 7 is the time during which the command to update the output holding latch with the contents (bits 0-6) of the data collection latch, is generated. Therefore, not only will bit 7 be swallowed when the counter is in the +7 mode, but bits 0-6 will also be lost since the hold latch update command is also swallowed. The result is that, in parallel mode only, a complete byte of input data is swallowed (output data is not updated) and the last byte of data stored in the holding latch is replayed at the output. The data output will not be updated until the counter is returned to the +8 mode. Therefore, in parallel mode, if it is necessary to determine from the output whether or not frame timing (frame synchronization) is correct, then the control input causing the +7 counter mode must be alternately inhibited. In ripple data mode, when a +7 operation occurs, due to any of the three controlling inputs, bit time 7 is still swallowed but input bits 0-6 are updated at the output because the output holding latch is always transparent in this mode. There are timing differences between the manner in which FRAME SHIFT, SYNC EN and SYNC IN cause the counter to switch to the +7 mode. SYNC IN should be used when multiple 10G041As are cascaded to increase the width. In this case, the SYNC OUT pulse from device A (called the master) is driven into the SYNC IN input of cascaded device B (termed the slave). The timing between the received SYNC OUT pulse from the master and the internal SYNC OUT pulse of the slave is compared by the slave and used to determine whether or not a +7 counter mode should be initiated in the slave. In this manner, multiple cascaded devices are automatically synchronized (see section on Cascading and SYNC OUT/SYNC IN Timing for examples).

The FRAME SHIFT and SYNC EN controls are also used to shift frame timing or position. In particular, SYNC EN is quite useful in alternating +7 and +8 modes as a means of controlling the frame synchronization process. When the FRAME SHIFT pin is pulsed with a rising edge anytime between Clock0 to slightly after Clock 5 during the time in which Byte A data is input, Bit7 (Clock7) of the SECOND following output data byte will be swallowed or lost. In ripple mode, this means that Bit7 of output Byte C is lost. In parallel mode, Bit7 of a repeated Byte B is swallowed. Byte B is repeated during the time at which Byte C would normally appear at the output because the output latch does not capture Byte C (recall that the holding latch update command is also swallowed). Refer to the Switching Waveforms Summary drawing which makes this operation clear.

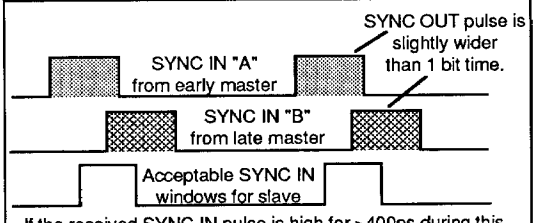
Compared with the FRAME SHIFT command, SYNC EN operates identically except that it is an active high level signal and its effect occurs on the IMMEDIATELY following data byte. When SYNC EN is brought high during the time interval when data Byte A is input, following the example above, data bytes will appear at the output in the order AACD and not ABBD as is the case for the FRAME SHIFT command example. In both cases, the last bit of the repeated byte (Bit7) is swallowed. Note that Byte A , not Byte B is repeated in response to SYNC EN, illustrating its more immediate affect on the output. SYNC EN, when used to shift frame timing, must meet minimum specified high time requirements and must go high anytime following Clock7 up to Clock5 in order for Bit7 of the IMMEDIATELY following byte to be swallowed.

5. SYNC OUT / SYNC IN TIMING; SYNCHRONIZATION OF CASCADED 10G041As

The 10G041A is designed to be cascaded to provide the ability to form wider word size demultiplexers and to achieve higher data rates than is possible with a single device. Cascaded devices are automatically synchronized via use of the SYNC OUT signal and SYNC IN input as explained in the previous section. Devices are configured for auto sync as follows:

1. Tie the SYNC EN pins of all slaves high (to VDDL) and that of the master low (to VSS);
2. Connect the SYNC OUT signal, delayed 600ps, of the master to the SYNC IN pins of all slaves.

Each slave now has its internal phase detection circuitry enabled to compare the amount of overlap between the received SYNC OUT pulse from the master and its own internally generated SYNC OUT pulse. There is, however a possible difficulty with this type of operation since the slave may potentially be sync'ed to either of two possible states of the master. This is due to the fact that the slave senses the level of the SYNC IN from the master during its internal sync time, and only requires this to be in the high state for 400ps. This results in the potential for redundant sync'ing as described below.



If the received SYNC IN pulse is high for >400ps during this window the master and slave will be in sync and the slave will count to 8; otherwise the slave will attempt to sync itself by dividing by 7 and swallowing a count.

In the sketch above, BOTH SYNC-IN "A" and "B" timing meet the requirement for the master and slave to be in sync; hence the slave will not swallow a count and will not resynchronize. To avoid this possible redundant sync state, the following scheme will assure that only the SYNC-IN "A" state will exist. The master device should be given a FRAME SHIFT after the parts have been turned on long enough to stabilize. If the slave was initially sync'ed to SYNC-IN A (early master) the FRAME SHIFT pulse will cause SYNC IN A to occur earlier in time and move in front of the acceptable window. As a result, the Slave will swallow a pulse and the SYNC-IN A condition will be re-established. If the slave is initially sync'ed to SYNC-IN B, the application of a FRAME SHIFT to the master will advance the master's SYNC OUT pulse to the SYNC-IN A condition, which is the desired in-sync state. It is also necessary to assure that the CLOCK and SYNC-OUT/SYNC-IN path delays match sufficiently such that >400 ps of overlap occur. Marginal overlap could result in initial syncing per the SYNC-IN A timing which might slip due to temperature, noise, etc. causing a slave to swallow a count and arrive at the SYNC-IN B condition.

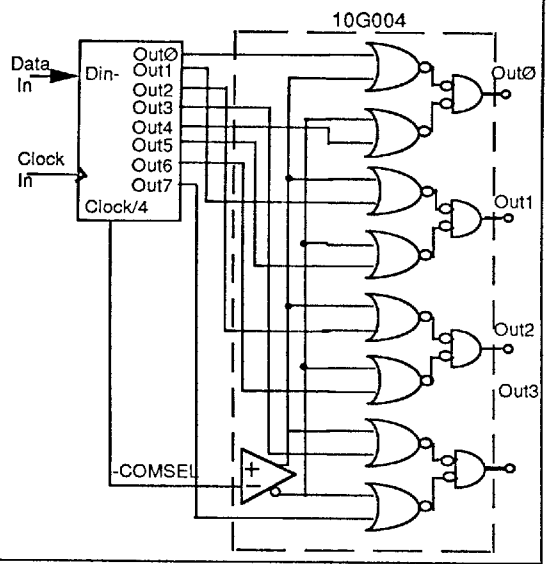
Since the clock delay internal to the slave exceeds the SYNC-IN delay by approximately 600 ps, it is necessary to delay the SYNC-OUT pulse from the master by approximately 600 ps before passing it to the SYNC-IN of the slave device. This is approximately the delay of most common combinatorial PicoLogic parts except for the NOR gates which have only a single stage. Hence, it is possible to achieve this delay by buffering the SYNC OUT pulse with devices such as the 10G002, 004, or 010. The10G010 fanout buffer might be used where several slave devices are required. When it is required to double the input speed of the 10G041A, two devices are driven with clocks 180° out of phase to form a single stage, high speed 1:16 demux.

The circuit drawings which follow show how the 10G041A is configured to create 1:4, 1:16 (double speed), and 1:64 demultiplexers. In order to assure the proper timing relationship between SYNC OUT and SYNC IN when cascading, the following circuit layout rules should be followed with the double speed 1:16 demultiplexer used for illustration:

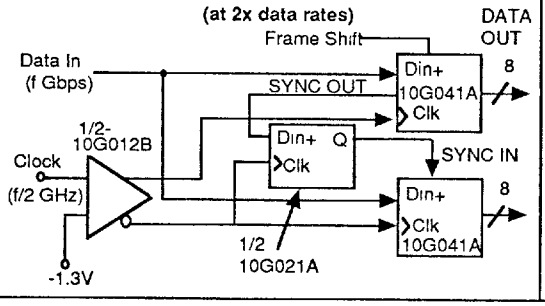
1. The incoming clock is converted to a bi-phase clock by the 10G012B, with the in-phase clock feeding the master and the out of phase clock feeding the slave. The inputs of the two multiplexers will therefore load their respective data collection latches on opposite phases of the clock permitting data to change during each half period of the clock.
2. SYNC OUT from the master must be delayed 600ps plus one half clock period before being sent to the SYNC IN input of the slave. The 10G021A is used to achieve this. Since the 10G021A clocks on the negative edge of the clock it is clocked from the non-inverted clock. For a fixed freq. of operation the flipflop could be eliminated and replaced with a delay line of a half period plus 600 ps.
3. The data input delays should be equalized for the two paths, otherwise additional clock delays and SYNC delays must be matched to the data delays.
4. Either CLK/8 output can be used as the handshake signal to the interfacing logic family since the output resister is stable during more than 6 of the possible 8 bit times. However it must be recognized that at a 2GBit/s data rate, all 16 outputs will be updated every 8ns.

CASCADING MULTIPLE 10G041A's (Note 2)

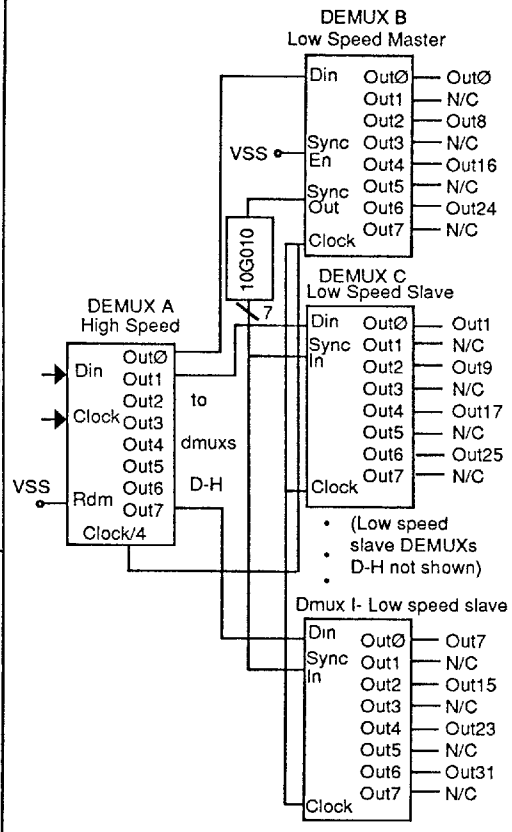
1:4 DEMULTIPLEXING



1:16 DEMULTIPLEXING (at 2x data rates)



1:32/1:64 DEMULTIPLEXING (Note 1)



NOTES

1. This block diagram shows the connections for 1:32 demultiplexing. Connections for 1:64 demultiplexing are identical, except that CLOCK/8 instead of CLOCK/4 is used and all 64 low speed outputs carry data.
2. In order to ensure the proper timing relationship between SYNC OUT and SYNC IN when cascading, the following circuit layout rules should be followed:
   (a). The CLOCK/4 (or CLOCK/8) signal from the high speed DEMUX (DEMUX A above) must be fed first to the CLOCK input of the master (DEMUX B) and then daisy-chained from the master to the low speed slaves. Similarly, SYNC OUT from the master must be connected in a daisy chain to the slaves.
   (b). The interconnect distance between the master's CLOCK connection and any slaves's CLOCK connection must equal the interconnect distance beteween the master's SYNC OUT connection and the SYNC IN connection to the same slave.
   (c). The interconnect distance between each OUT pin of the high speed DEMUX (A) and the DIN pin of each low speed DEMUX must equal the interconnect length of the corresponding connection between DEMUX A's CLOCK output and the low speed DEMUX's CLOCK input.

DC CHARACTERISTICS

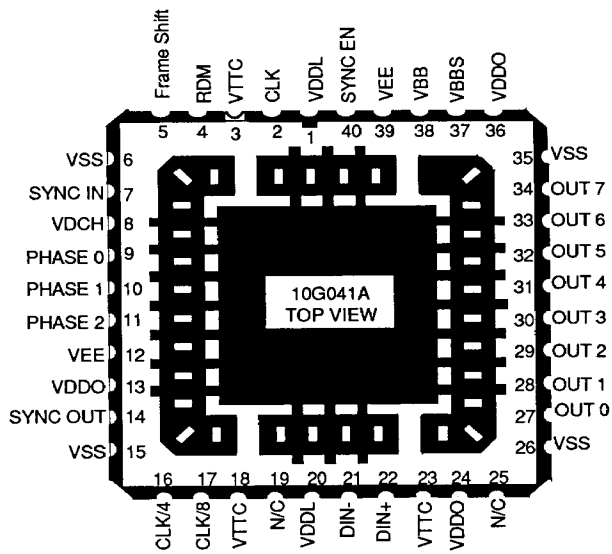
Tc =0°C to 85°C, VSS = -3.6V to -3.4V, VEE = -5.5V to -5.1V, VDDL=VDDO =Gnd, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Notes
IBB	Reference Input Current		450	600	µA	VBB = -1.3 V	
ISS	VSS power supply current		400	500	mA		
IEE	VEE power supply current		50	75	mA		
PD	Power dissipation		1.6	2.2	W		

Note:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

PIN FUNCTIONS - 40 PIN PACKAGE TYPES "C" AND "L"



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

AC CHARACTERISTICS (NOTES 1,2,3,4)

10G041A-3

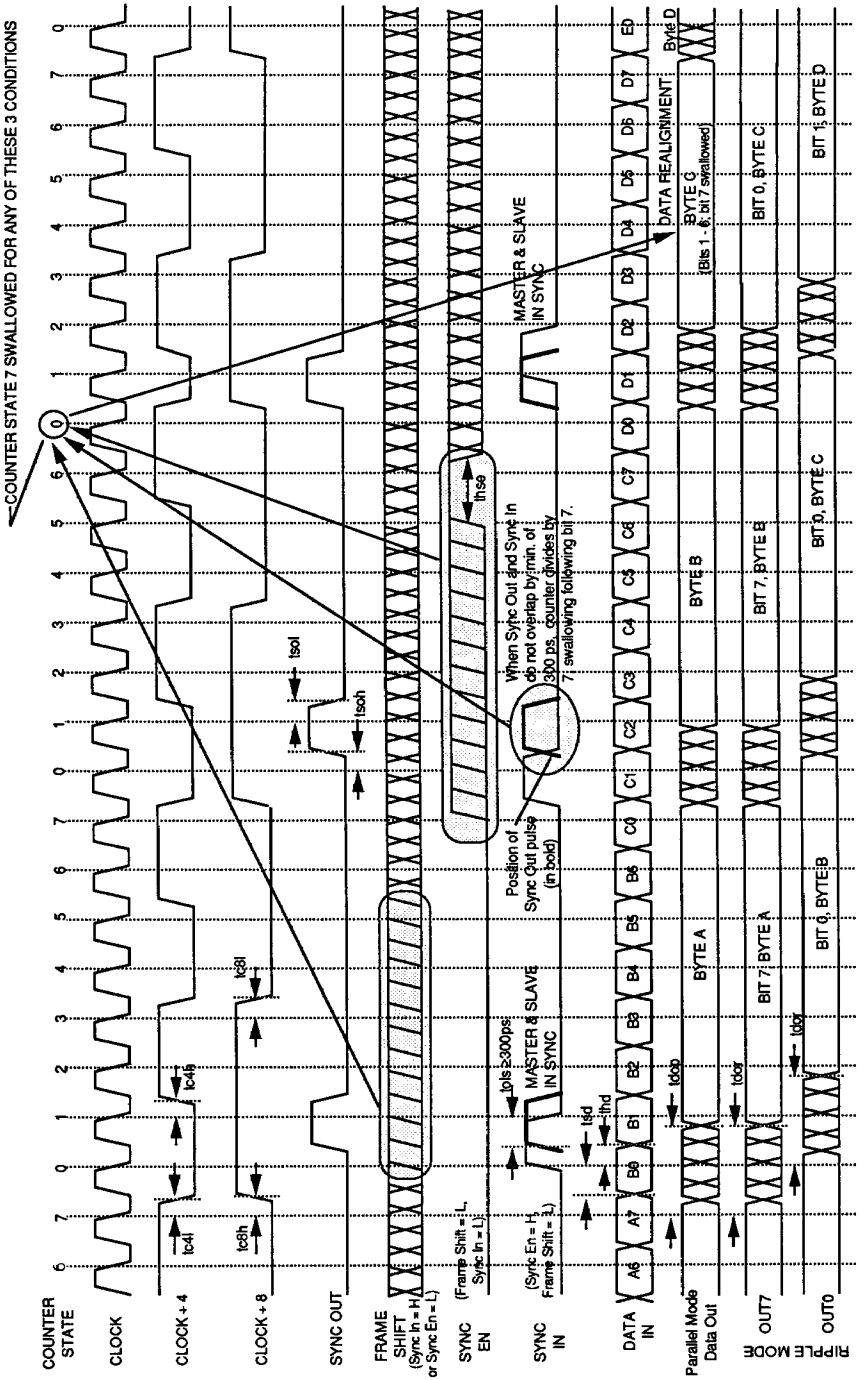
SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency	1.00		1.00	1.20		1.05		GHz
tsoh	CLK0 to sync out high	1250	1650		1450		1250	1650	ps
tsol	CLK1 to sync out low	1350	1750		1550		1350	1750	ps
tc4h	CLK1 to CLK/4 high	1250	1650		1450		1250	1650	ps
tc4l	CLK7 to CLK/4 low	1500	1900		1700		1500	1900	ps
tc8h	CLK7 to CLK/8 high	1550	1950		1750		1550	1950	ps
tc8l	CLK3 to CLK/8 low	1350	1750		1550		1350	1750	ps
tdop	CLK7 to parallel data output	1900	2300		2100		1900	2300	ps
tdor	CLKn to ripple data output	1900	2300		2100		1900	2300	ps
thse	SYNC EN high time	500		500			500		ps
tsd	Data to CLK0 setup time	-300		-300	-400		-300		ps
thd	CLK0 to data hold time	850		850	700		850		ps
tr,f	Output rise and fall times		200		150	200		200	ps

10G041A-4

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/T	Clock Frequency	0.75		0.75	0.90		0.75		GHz
tsoh	CLK0 to sync out high	1250	1750		1500		1250	1750	ps
tsol	CLK1 to sync out low	1350	1950		1600		1350	1950	ps
tc4h	CLK1 to CLK/4 high	1250	1750		1500		1250	1750	ps
tc4l	CLK7 to CLK/4 low	1400	2000		1750		1400	2000	ps
tc8h	CLK7 to CLK/8 high	1550	2050		1800		1550	2050	ps
tc8l	CLK3 to CLK/8 low	1350	1850		1600		1350	1850	ps
tdop	CLK7 to parallel data output	1900	2400		2150		1900	2400	ps
tdor	CLKn to ripple data output	1900	2400		2150		1900	2400	ps
thse	SYNC EN high time	500		500			500		ps
tsd	Data to CLK0 setup time	-300		-300	-400		-300		ps
thd	CLK0 to data hold time	850		850	700		850		ps
tr,f	Output rise and fall times		250		200	250		250	ps

1. Test conditions (unless otherwise noted): VBB = -1.3V, VTT = -2.0V, VTTC = Vtt, Rload = 50Ω to VTT, Vdch = Vddo, Vih = -0.5V, Vil = -1.9V, Voh≥ -0.7V, Vol ≤ -1.7V. Input signal rise and fall times ≤ 200ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.
3. This applies when phase 0 = Phase 1 = Phase 2 = low.
4. Clock input = 1.5Vp-p, -1.3V DC offset.

10G041A SWITCHING WAVEFORMS AND TIMING CHARACTERISTICS SUMMARY



NOTES:
1. CLOCK + 8 IS SHOWN WITH PHASE 0 = PHASE 1 = PHASE 2 = LOW.
2. The falling edge of Clock7 causes the output hold latch to become transparent; the Clock0 falling edge causes the output hold latch to hold data.
3. Clock0 initiates the generation of the SYNC OUT pulse. Therefore, SYNC OUT delays are referenced to Clock0.