Specification

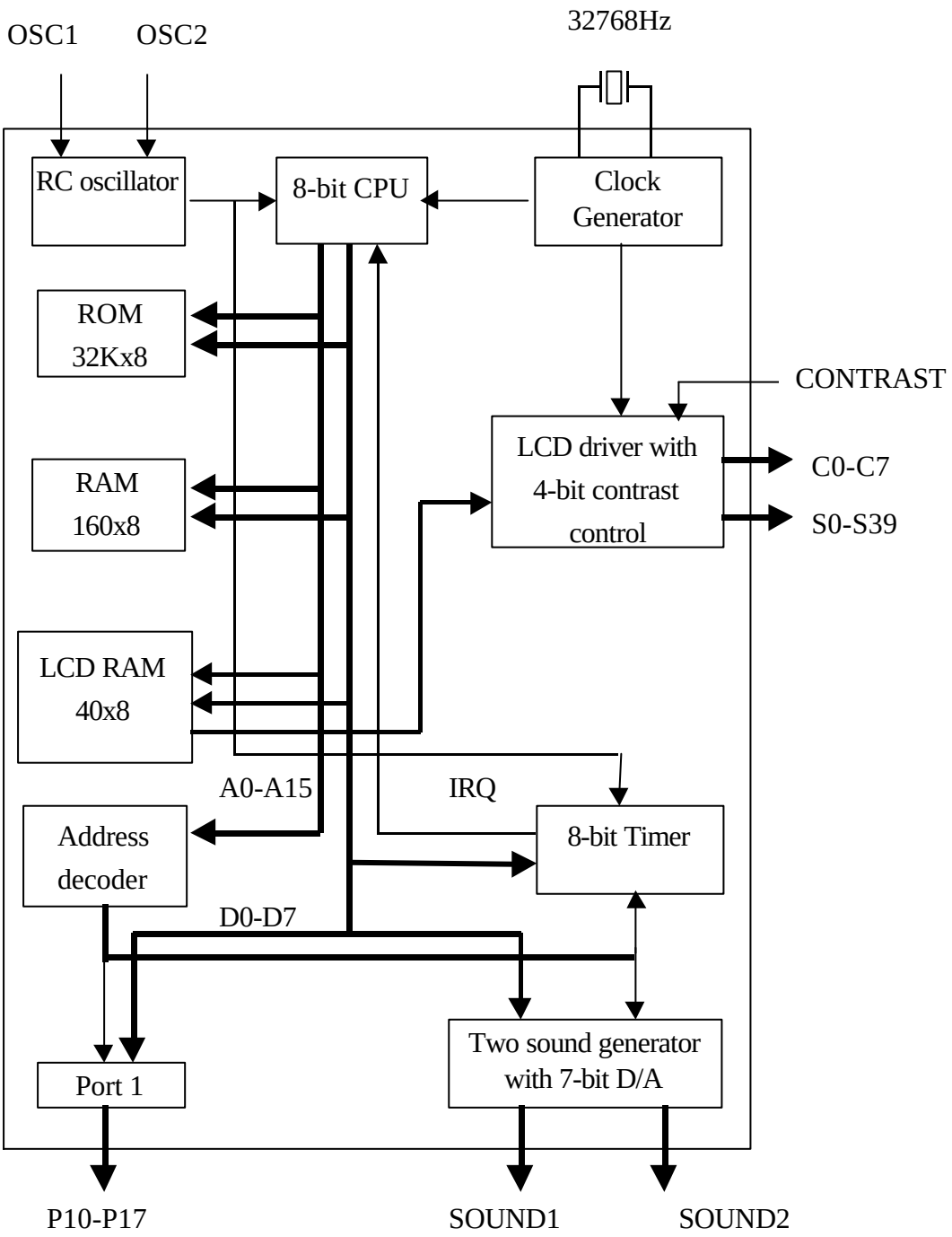
1. FEATURES :

* Operating voltage : 2.5V – 5.5 V.
* Maximum CPU operating frequency : 2MHz at 2.7V
* Dual oscillators :
  - RC or 32.768 KHz crystal oscillator for LCD display and watch timer.
  - RC oscillator for system clock.
* 40 segments and 8 commons output for LCD driver.
  - 1/4 bias, 1/8 duty and 64Hz frame frequency.
  - 16 levels contrast control.
* I/O port.
  - 8 I/O pins with selectable wake up interrupt.
  - Two output pins. These two pins can be set as sound channel DAC outputs.
* Built in 160 bytes data RAM and 40 bytes display RAM.
* Built in 32K bytes ROM for program.
* One 8-bit timer with 8 predefined input clock.
* Two sound generators with 7-bit D/A output.
* Four interrupt sources :
  NMI - 64 Hz interrupt
  IRQ1 - Fix-time timer interrupt
  IRQ2 - Timer interrupt
  IRQ3 - External interrupt
* Code option :
  - Built-in 150K OHM pull-up resistors for I/O port.
  - RC or 32768Hz crystal oscillation for LCD driver.

2. APPLICATION :

* Calculator
* Hand-held game
* Small instrument
* Toy

3. BLOCK DIAGRAM :



4. PIN DESCRIPTION : (Total 66 pads)

Pin name	I/O	Function description
COM0-COM7	O	LCD common output pins
SEG0-SEG39	O	LCD segment output pins
P10-P17	I/O	8-bit I/O pins for port 1
OSC1	I	Main system oscillator input pin for chip
OSC2	O	Main system oscillator output pin for resistor
XOSC1	I	32.768K Hz crystal oscillator input
XOSC2	O	32.768K Hz crystal oscillator output
SOUND1	O	Sound channel 1 output with volume control. This pin is CMOS output when sound channel is disabled.
SOUND2	O	Sound channel 2 output with volume control. This pin is CMOS output when sound channel is disabled.
/RES	I	System reset pin with 150K pull-up resistor.
CONTRAST	I	Bias voltage input pin. Add a resistor to Vdd can change the LCD contrast.
VDD		Power input
VSS		Signal ground

5. ADDRESS ARRANGEMENT

1) RAM

0000-003C for LCD output data storage. The memory address which are not specified in the table are not implemented

Memory address	Pin for 1/8 duty
0000-0004	COM0
0008-000C	COM1
0010-0014	COM2
0018-001C	COM3
0020-0024	COM4
0028-002C	COM5
0030-0034	COM6
0038-003C	COM7

The LSB of low byte – SEG0.

The MSB of high byte – SEG39.

The middle bits are in the order.

0040-00DF for zero page area.
0100-01DF for stacks. This area is overlapped with 0000-00DF.

2) ROM

8000-FFFF for program area.
FFFF, FFFE - IRQ vector.
FFFD, FFFC - RES vector.
FFFB, FFFA - NMI vector.

3) Others

1000 To enter stand-by mode. Write only.
* Write this address, the CPU will be hold with LCD state no change.
* When in stand-by mode, the NMI and IRQ will wake up the CPU.

1001 To enter sleep mode. Write only.
Bit 0 = 1 Sleep mode 1
1 = 1 Sleep mode 2
In sleep mode 1, both of the main system oscillator and 32.768KHz sub-system oscillator will be stopped. So, all functions are stopped and only external interrupt can wake up this chip. The LCD display will be turn off while getting into sleep mode 1. If the LCD is turned on after wake-up immediately, then some garbage may display on the LCD. It is better to turn off the LCD by software before enter sleep mode 1. After wake up, the software has to delay several ms before turn on the LCD because the crystal will take several mS to stable.
In sleep mode 2, only main system oscillator will be stopped. So, the following functions will still keep working.
* The LCD will be kept on.
* The fix-time timer will keep going.
* The NMI, port 1, and fix-time timer interrupt will wake up this chip.
* CPU will keep working if clock source is 32.768K Hz.

1002 Watch timer control register. Write only.
Bit 1 : = 0 Set fix-time timer interrupt at 2 Hz
= 1 Set fix-time timer interrupt at 1 Hz

4 : = 0 CPU clock is system clock.
= 1 CPU clock is 32.768K Hz.
7-5 : Reserved.
The default values for each bit is zero.

1003 IRQ flag register. Read & write.

Read function :
Bit 0 : = 1 Fix-time timer interrupt, IRQ1.
1 : = 1 Timer interrupt, IRQ2.
2 : = 1 External interrupt, IRQ3.
Write function :
Bit 0 : = 0 Clear fix-time timer interrupt.
1 : = 0 Clear timer interrupt.
2 : = 0 Clear external interrupt.

* Before firmware exits the interrupt routine, the interrupt flag must be cleared. Otherwise, the IC will get into interrupt again.
* Write 0 to clear the corresponding IRQ but do not use ' STZ $1003' to clear all interrupts at the same time. Following instructions are recommended

```
LDA     $1003
STA     IRQBuff
EOR     #0FFH
STA     $1003       ;Clear all active interrupts at the same time
LDA     IRQBuff
AND     #1
BEQ     next_irq
```

* Do NOT use TRB to test and clear this register. Following instructions are recommended.

```
LDA     $1003
AND     #1          ;Check IRQ 1
BEQ     next_irq
STA     $1003       ;Clear the active interrupt.
```

1004 Port 1 data. Read & write.

1005 Set port 1 bit function. Write only.

* An '1' in this register will set the corresponding pin of port 1 as an output pin.
* The default values for each bit is zero. A pull-up resistor can be added to the pin by code option.

But the pull-up resistor will be disabled if this pin is set as output.

1008 Volume control for sound channel 1. Write only.

Bit 7-1 : Volume for sound channel 1. $FF is the maximum volume. If bit 1 of $1013 is zero, then bit 1 will output to SOUND 1 pin.

1009 Volume control for sound channel 2. Write only.

Bit 7-1 : Volume for sound channel 2. $FF is the maximum volume. If bit 3 of $1013 is zero, then bit 1 will output to SOUND 2 pin.

100C Set port 1 bit interrupt function. Write only.

* An '1' in this register will set the interrupt function of the corresponding pin of port 1 to be enable. That is, an interrupt will be generated if a low level is detected in the pin.
* If port 1 are used as key inputs, there are several interrupts will be generated during key pressing or release. This is caused by key bounce. It is suggested to disable the port1 interrupt after port 1 interrupt is detected and enable the port 1 interrupt after key released. Or enable port 1 interrupt before entering sleep or standby mode and disable port 1 interrupt after IC wakeup.
* The default values for each bit is zero.

100D Timer 1 data. Read & write.

* Before writing $100D, the program should select timer clock ($100E) first.
* After timer 1 been enabled, the timer will start to count down. When timer counts to zero, the timer will count from the initial value and IRQ2 will happen.
* Valid values are from 1 to 255. Zero is prohibited.
* If CPU read this register, the value will be 1 to 255. Please note that the CPU will never read a zero from timer.
* The time elapse = ($100D)/timer clock

100E Timer 1 clock select and contrast setting. Write only.

Bit 2-0 : = 000 System clock/2
= 001 System clock/4
= 010 System clock/8
= 011 System clock/16
= 100 System clock/32
= 101 System clock/64
= 110 System clock/128
= 111 System clock/256

3 : Reserved

7-4 : LCD contrast control. The minimum contrast value is zero and the maximum contrast value is 0FH. The default state is maximum contrast.

The default values of bit 3-0 are unknown.

100F Control register. Write only.

Bit 1 : = 0 Disable timer 1 interrupt.
= 1 Enable timer 1 interrupt.

2 : = 0 Disable NMI.
= 1 Enable NMI.

3 : = 0 Disable timer 1.
= 1 Enable timer 1.

4 : = 0 LCD off.
= 1 LCD on.

6 : = 0 Disable fix-time timer interrupt.
= 1 Enable fix-time timer interrupt.

* The default values for each bit is zero.

1010 Sound generator clock select. Write only.

Bit 2-0 : Sound generator 1 clock select.

6-4 : Sound generator 2 clock select.
= 000 System clock/2
= 001 System clock/4
= 010 System clock/8
= 011 System clock/16
= 100 System clock/32
= 101 System clock/64
= 110 System clock/128
= 111 System clock/256

7&3 : Reserved

The default value is unknown.

1011 Sound generator 1 data. Write only.

* Before writing $1011, the program should select timer clock ($1010) first.
* After sound generator is enabled, it will start to count down. When it counts to zero, the it will count from the initial value again.
* Valid values are from 1 to 255. Zero is prohibited.

* The time elapse = ($1011)/timer clock/2

1012 Sound generator 2 data. Write only.

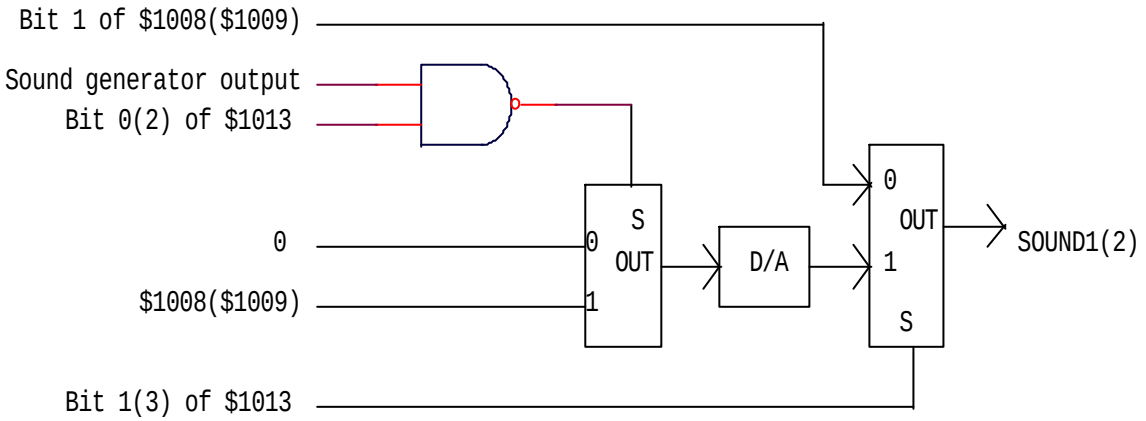
* Before writing $1012, the program should select timer clock ($1010) first.
* After sound generator is enabled, it will start to count down. When it counts to zero, it will count from the initial value again.
* Valid values are from 1 to 255. Zero is prohibited.
* The time elapse = ($1012)/timer clock/2

1013 Sound channel control register. Write only.

Bit 0 : = 0 Disable sound generator 1.
= 1 Enable sound generator 1.
1 : = 0 Set SOUND 1 to CMOS output pin.
= 1 Set SOUND 1 to sound channel 1 DAC output.
2 : = 0 Disable sound generator 2.
= 1 Enable sound generator 2.
3 : = 0 Set SOUND 2 to CMOS output pin.
= 1 Set SOUND 2 to sound channel 2 DAC output.

The default values for each bit is zero.

Please follow the item 6.4 for sound channel operation.



6. FUNCTION DESCRIPTION

6.1 The reset state of control registers:

Address	Value after reset
$1002	XXX00000
$1003	XXXXX000

$1004	XXH
$1005	00H
$1008	XXXXXX0X
$1009	XXXXXX0X
$100C	00H
$100D	XXH
$100E	FXH
$100F	00H
$1010	XXH
$1011	XXH
$1012	XXH
$1013	00H

6.2 The reset status of CPU

If the /RES is keep low more than two system clocks, then the CPU will be reset. After reset, the interrupt mask flag is set, the decimal mode is cleared and the program counter will be loaded with the reset vector from address $FFFC and $FFFD. So, **after initial procedure the firmware should do a ' CLI' instruction**. Otherwise, the CPU will not acknowledge any interrupt.

6.3 Interrupt Sources

* There are five interrupt sources :
  NMI - 64 Hz interrupt.
  IRQ1 - Fix-time timer interrupt.
  IRQ2 - Timer interrupt.
  IRQ3 - Port 1 interrupt.
* All interrupts will wake up CPU from standby mode.
* NMI, IRQ1 and IRQ3 will wake up CPU from sleep mode 2.
* Only IRQ3 will wake up CPU from sleep mode 1.
* When port 1 is in input mode and pin interrupt enable, a low signal from pin will generate IRQ3.
* When the CPU acknowledge the interrupt, following things will be done:
  a) The interrupt mask flag will be set by CPU
  b) The return address and status register will be pushed to stack.
* When the CPU return from interrupt routine by RTI instruction following things will be done:
  a) The return address and status register will be pulled from stack.
  b) The interrupt mask flag will be cleared.

* I**t is not necessary to add SEI and CLI instructions in interrupt routine**. If a CLI instruction is added in the interrupt routine, then another interrupt may be inserted during current interrupt routine and may cause stack overflow.

6.4 Sound channel operation :

6.4.1 If two sound channels are used and the SOUND1 and SOUND2 are tied together, then please follow below instructions to make two sound channels work.

1). All channels off.
   a. Set $1013 to zero.
   b. Set $1008 and $1009 to zero .

2). Channel 1 output tone and channel 2 output voice or turn off .
   a. Set $1013 to 0BH.
   b. Set $1009 to zero to turn off or set the volume according to the voice data.
   c. Set $1008 to the desired volume.
   d. Set sound generator to the desired frequency.

3). Channel 2 output tone and channel 1 output voice or turn off.
   a. Set $1013 to 0EH.
   b. Set $1008 to zero to turn off or set the volume according to the voice data.
   c. Set $1009 to the desired volume.
   d. Set sound generator to the desired frequency.

4). Channel 1 output voice or turns off and channel 2 output voice or turns off.
   a. Set $1013 to 0AH.
   b. Set $1009 to zero to turn off or set the volume according to the voice data..
   c. Set $1008 to zero to turn off or set the volume according to the voice data.
   Note : If both of these two channels are off, then $1013 should be set to zero. (see item 1)

5). Two channels output tone.
   a. Set $1013 to 0FH.
   b. Set $1008 and $1009 to the desired volumes.
   c. Set sound generators to the desired frequency.

6.4.2 If only one channel is used or two channels are used but they are not tied together, then follow below instructions.

1). Channel off.
   a. Set SOUND output to CMOS output (bit 1 or bit 3 of $1013 to zero).
   b. Set volume to zero ($1008 or $1009).

2). Channel output tone.
   a. Set SOUND output to DAC output (bit 1 or bit 3 of $1013 to one).
   b. Set sound generator to the desired frequency.
   c. Set the channel volume ($1008 or $1009).
   d. Enable sound generator (bit 0 or bit 2 of $1013 to one).

3). Channel output voice.
   a. Set SOUND output to DAC output (bit 1 or bit 3 of $1013 to one).
   b. Disable sound generator (bit 0 or bit 2 of $1013 to zero).

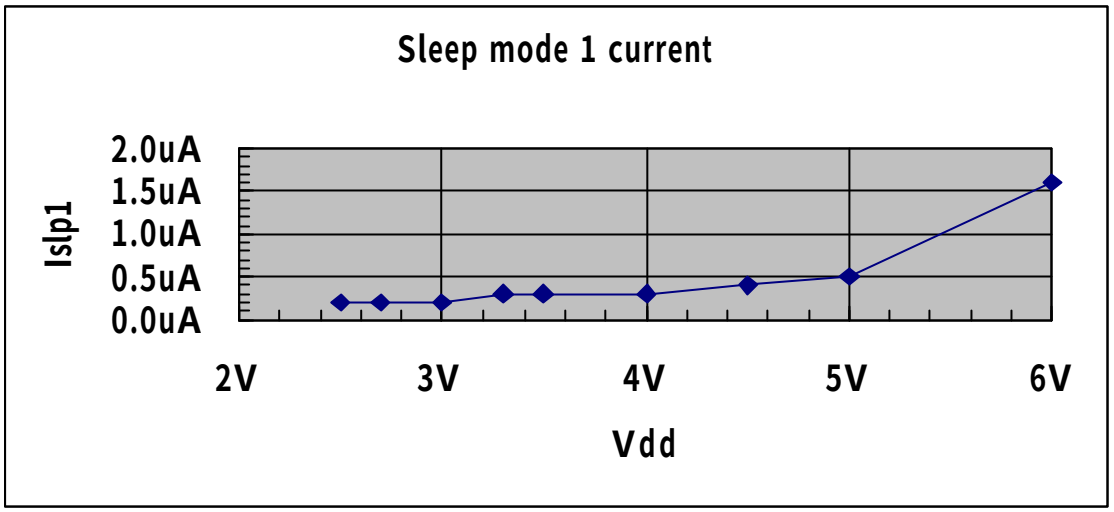
c. Set the volume according to the voice data ($1008 or $1009).

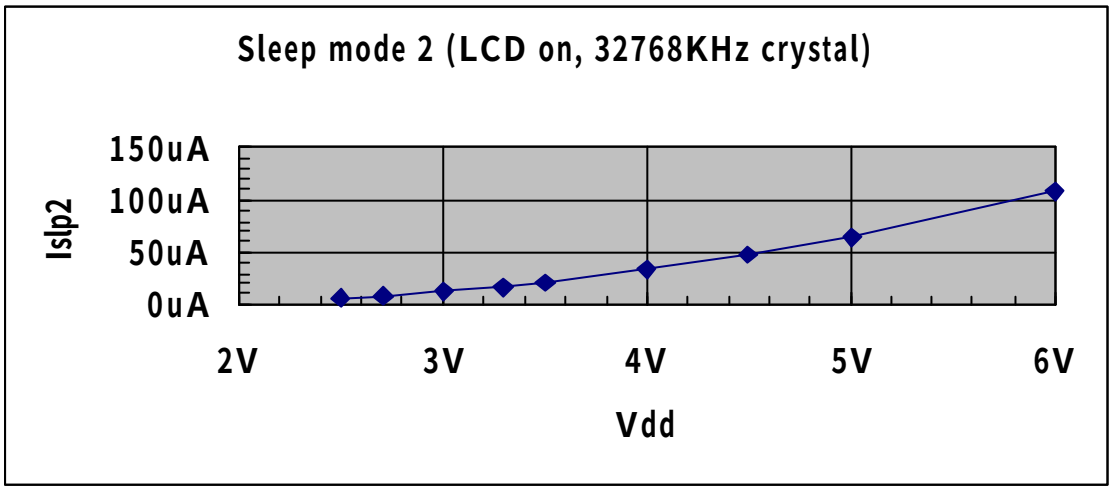
7. ABSOLUTE MAXIMUM RATINGS

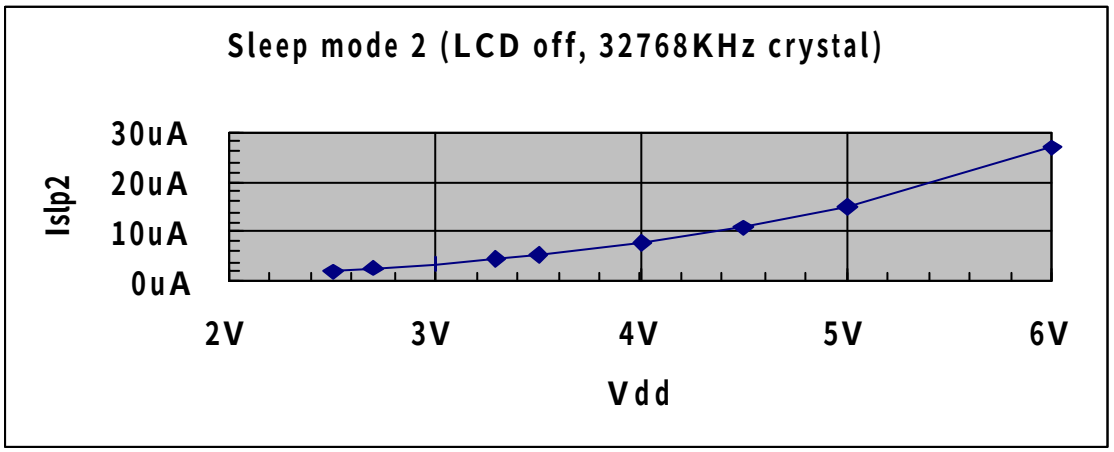
Operating temperature ..... 0 to 70 ℃
Storage temperature ..... -65 to 150 ℃
Supply voltage ..... 7 V
Input voltage ..... -0.6 to Vdd+0.6 V

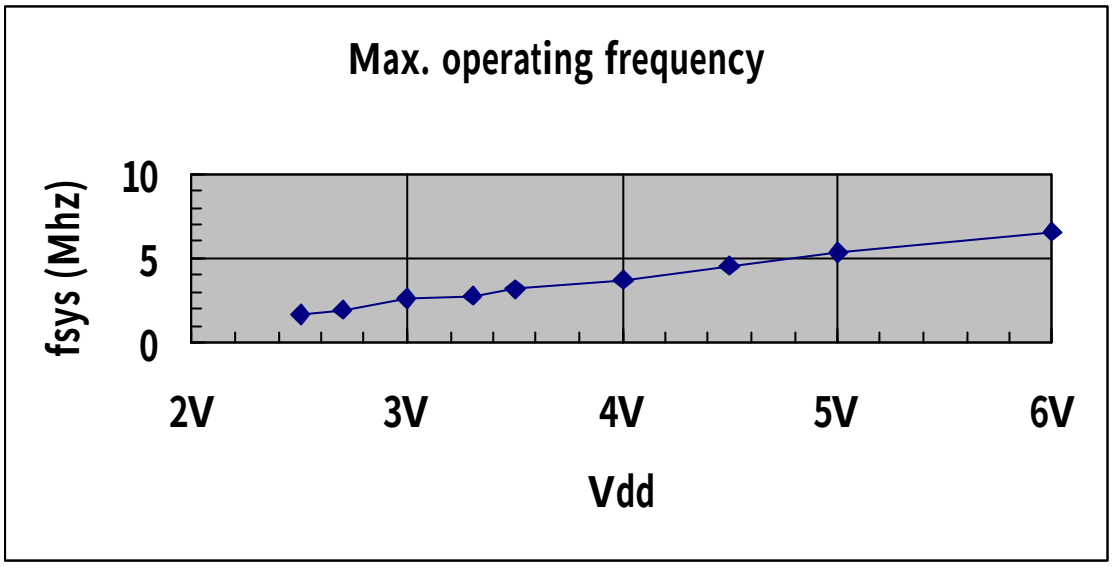
8. ELECTRICAL CHARACTERISTIC :

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	Vdd		2.5	3.0	5.5	V
Main system frequency	∅sys	Vdd=2.7V	0.1	1	2	MHz
Crystal frequency	∅cry			32768		Hz
Operating current	Idd	Vdd=3V,∅sys=120Khz Vdd=3V,∅sys=1Mhz		120 1		μA mA
Sleep mode 1 current	Islp1	Vdd=3V, LCD off Vdd=5V, LCD off		0.2 0.5		μA μA
Sleep mode2 current (32768KHz using crystal)	Islp2	Vdd=3V,LCD on Vdd=3V,LCD off Vdd=5V, LCD on Vdd=5V, LCD off		15 4 65 15		μA μA μA μA
Sleep mode2 current (32768KHz using RC)	Islp2	Vdd=3V,LCD on Vdd=3V,LCD off Vdd=5V,LCD on Vdd=5V,LCD off		25 8 87 31		μA μA μA μA
Input high voltage	Vih	Vdd=5.0V	2.0			V
Input low voltage	Vil	Vdd=5.0V	-0.6		0.8	V
Input high leakage current	Iih	Vih=Vdd			-1	μA
Input low leakage current	Iil	Vil=0V			1	μA
Output high voltage (For SEGx and COMx)	Voh1	Ioh=-30μA	Vlcd -0.2		Vlcd	V
Output low voltage (for SEGx and COMx)	Vol1	Iol=40μA	0		0.2	V
Output high voltage (for other pins)	Voh2	Ioh=-2mA	Vdd- 0.4		Vdd	V
Output low voltage (for other pins)	Vol2	Iol=2mA	0		0.4	V

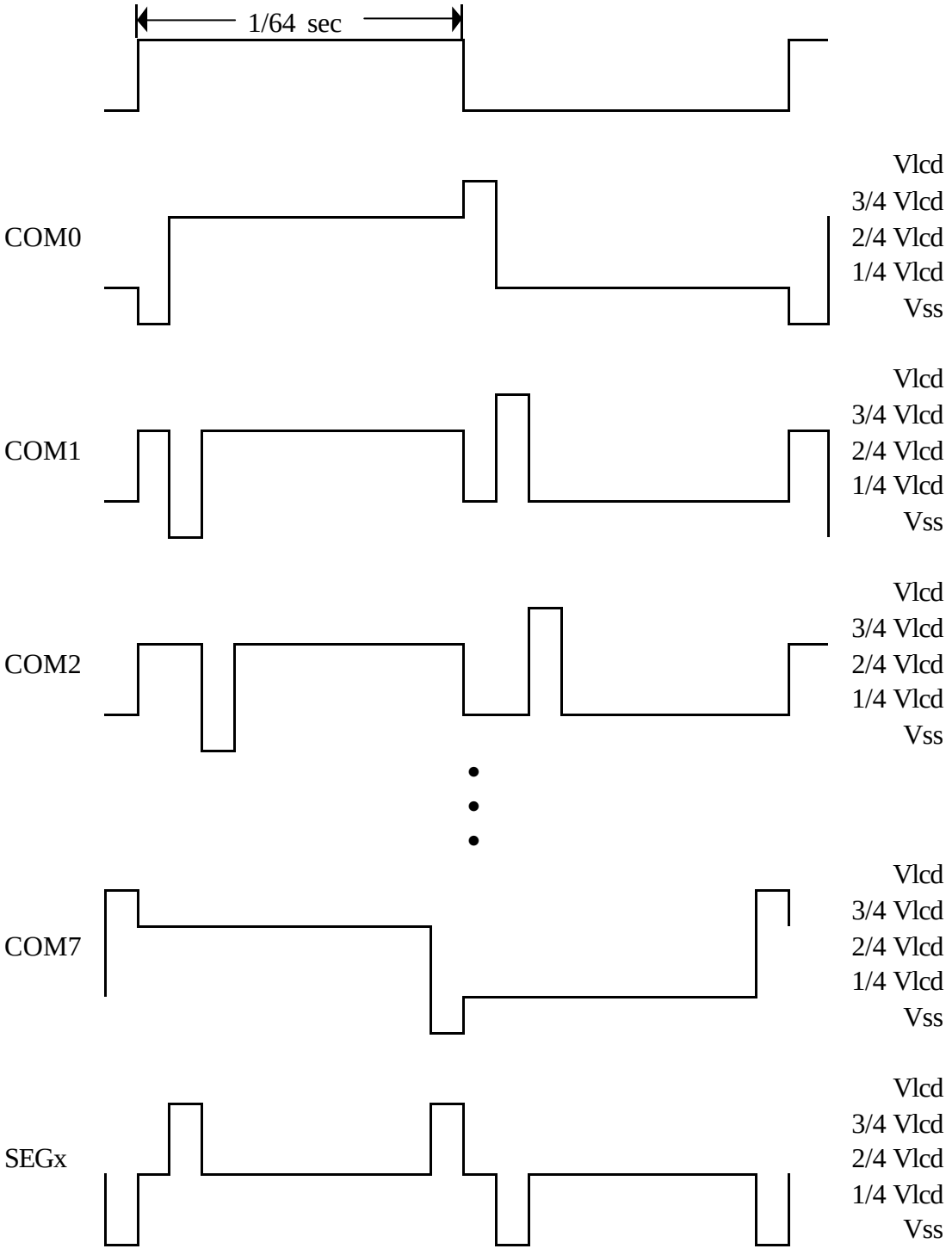

Sleep mode 1 current
Islp1
2.0uA
1.5uA
1.0uA
0.5uA
0.0uA
2V
3V
4V
5V
6V
Vdd


Sleep mode 2 (LCD on, 32768KHz crystal)
Islp2
150uA
100uA
50uA
0uA
2V
3V
4V
5V
6V
Vdd


Sleep mode 2 (LCD off, 32768KHz crystal)
Islp2
30uA
20uA
10uA
0uA
2V
3V
4V
5V
6V
Vdd

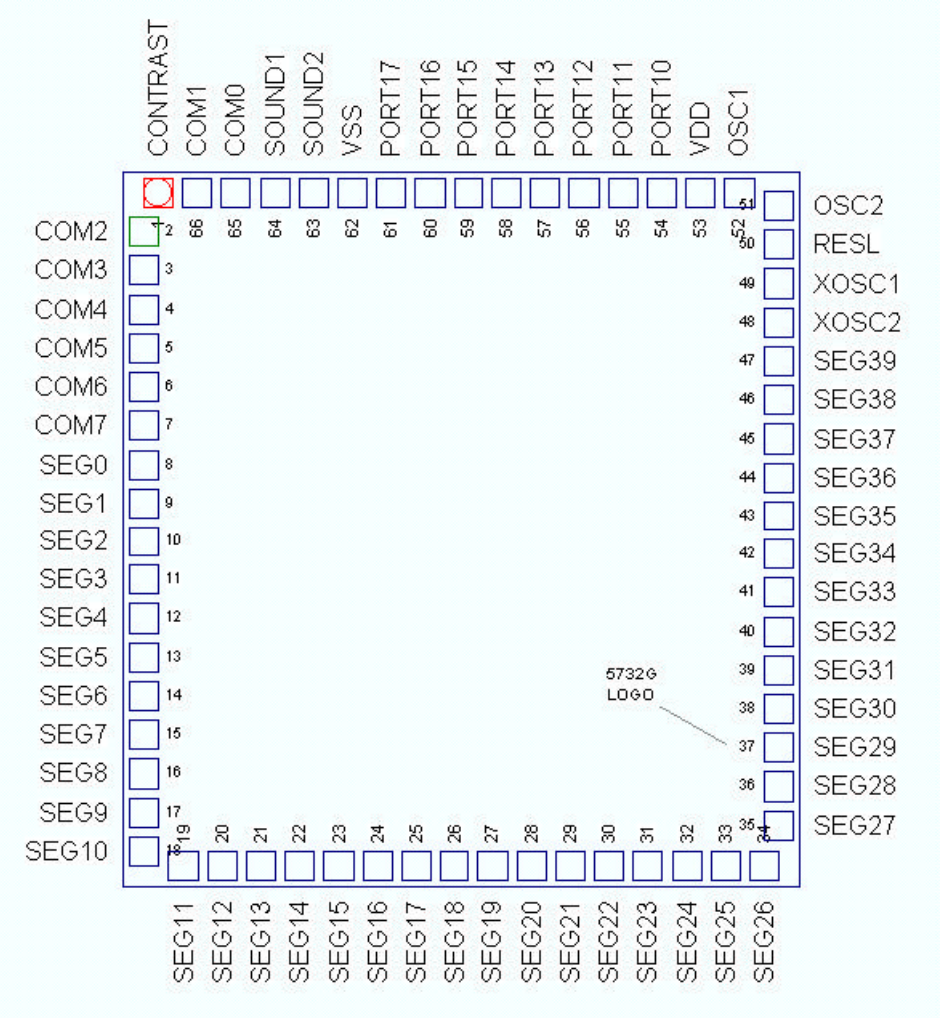

Max. operating frequency
fsys (Mhz)
10
5
0
2V
3V
4V
5V
6V
Vdd

9. LCD WAVEFORM :



There are two LCD matrix DOTs active at (SEGx,COM1) and (SEGx,COM7)

10. PAD LOCATION :

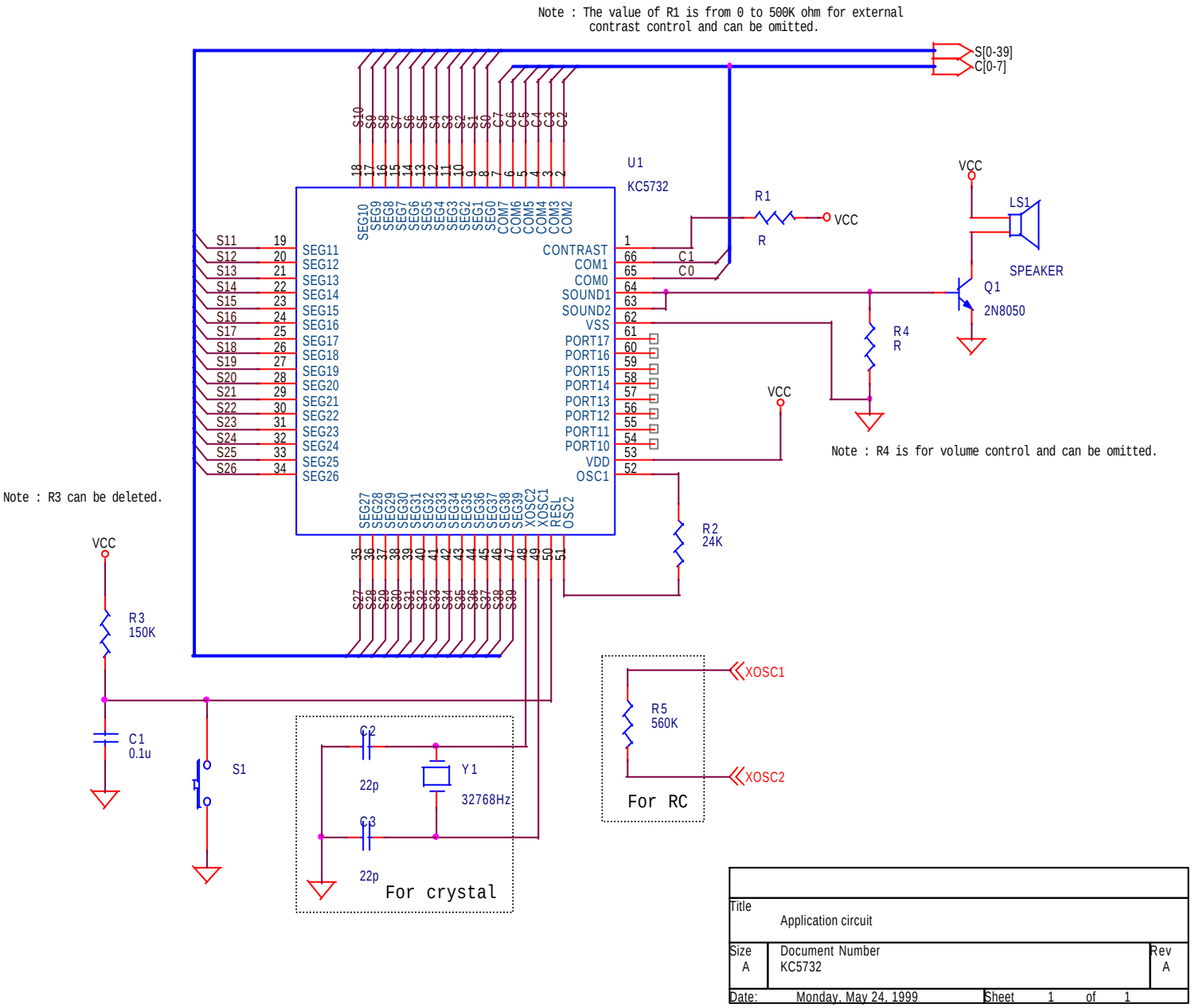


Chip size : 2090 x 2210 Unit : µM

PAD-No	Name	X	Y	PAD-No	Name	X	Y
1	CONTRAST	106.37	2147.50	34	SEG26	1983.64	62.50
2	COM2	63.64	2027.50	35	SEG27	2026.37	187.50
3	COM3	63.64	1907.50	36	SEG28	2026.37	307.50
4	COM4	63.64	1787.50	37	SEG29	2026.37	427.50
5	COM5	63.64	1667.50	38	SEG30	2026.37	547.50
6	COM6	63.64	1547.50	39	SEG31	2026.37	667.50

PAD-No	Name	X	Y	PAD-No	Name	X	Y
7	COM7	63.64	1427.50	40	SEG32	2026.37	787.50
8	SEG0	63.64	1307.50	41	SEG33	2026.37	907.50
9	SEG1	63.64	1187.50	42	SEG34	2026.37	1027.50
10	SEG2	63.64	1067.50	43	SEG35	2026.37	1147.50
11	SEG3	63.64	947.50	44	SEG36	2026.37	1267.50
12	SEG4	63.64	827.50	45	SEG37	2026.37	1387.50
13	SEG5	63.64	707.50	46	SEG38	2026.37	1507.50
14	SEG6	63.64	587.50	47	SEG39	2026.37	1627.50
15	SEG7	63.64	467.50	48	XOSC2	2026.37	1747.50
16	SEG8	63.64	347.50	49	XOSC1	2026.37	1867.50
17	SEG9	63.64	227.50	50	RESL	2026.37	1987.50
18	SEG10	63.64	107.50	51	OSC2	2026.37	2107.50
19	SEG11	183.64	62.50	52	OSC1	1906.37	2147.50
20	SEG12	303.64	62.50	53	VDD	1786.37	2147.50
21	SEG13	423.64	62.50	54	PORT10	1666.37	2147.50
22	SEG14	543.64	62.50	55	PORT11	1546.37	2147.50
23	SEG15	663.64	62.50	56	PORT12	1426.37	2147.50
24	SEG16	783.64	62.50	57	PORT13	1306.37	2147.50
25	SEG17	903.64	62.50	58	PORT14	1186.37	2147.50
26	SEG18	1023.64	62.50	59	PORT15	1066.37	2147.50
27	SEG19	1143.64	62.50	60	PORT16	946.37	2147.50
28	SEG20	1263.64	62.50	61	PORT17	826.37	2147.50
29	SEG21	1383.64	62.50	62	VSS	706.37	2147.50
30	SEG22	1503.64	62.50	63	SOUND2	586.37	2147.50
31	SEG23	1623.64	62.50	64	SOUND1	466.37	2147.50
32	SEG24	1743.64	62.50	65	COM0	346.37	2147.50
33	SEG25	1863.64	62.50	66	COM1	226.37	2147.50

1. APPLICATION CIRCUIT :



User guide for STK55C322/324 emulator

1. Connectors :

1.1 J1 is a phone jack connector. Please connect to a voltage adapter with 7 Vdc output.

1.2 JP1 and JP2 should be connected to external LCD panel or LCD simulator.

1.3 JP3 is I/O port connector.

1.4 JP4 is for external speaker.

2. Switch setting :

2.1 S1 set the CPU compatible to standard CPU or KC5713 CPU.

2.2 S2 select internal CPU or external CPU.

INT. CPU – In this mode, the internal CPU is enabled. The external CPU or ICE should be removed.

EXT. CPU – In this mode, the internal CPU is disabled. An external CPU or ICE should be installed in U1.

2.3 S3 is power switch for EV chip.

IC ON – The Vcc is connected to the KC5731 IC.

IC OFF -- The Power pin of KC5731 IC is floating. The IC operating current can be measured by connecting a current meter between the two points of TP2 or between J7 and J8.

2.4 S4 is oscillator selection switch.

XTAL -- Use 32768HZ crystal oscillator.

RC -- Use RC oscillator. R3 will decide the oscillation frequency. In this mode, the Y1 crystal should be removed. The frequency can be checked at XOSC2.

2.5 S5 is reset switch.

2.6 S6 is speaker selection switch.

INT. SPK -- On board speaker is selected.

EXT. SPK -- External speaker is selected. The customer' s speaker can be add between J9 and J11.

2.7 S7 is power switch.

EXT. PWR -- Add DC power from J2 (GND) and J3 (Vdd). The voltage range is

from 2.2V to 5.5V.

REG. PWR -- Add an adapter to J1. The system power is through the LM7805 voltage regulator.

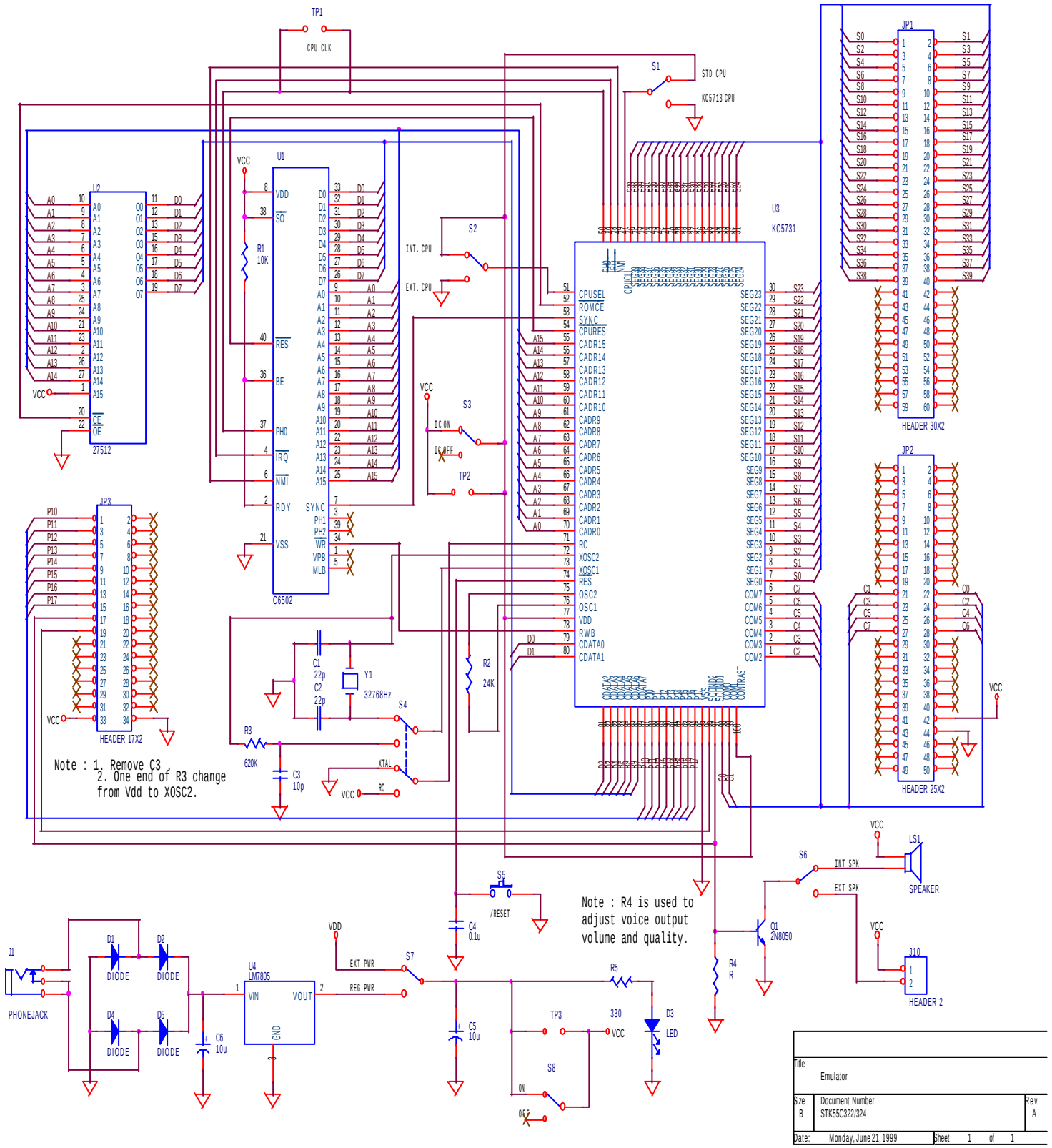
2.8 S8 is power switch for the emulator.
ON -- Normal operation.
OFF -- Add a current meter between TP3 or between J5 and J6 to measure the current of whole system.

3. Others :

3.1 TP1 – The CPU clock. The R2 will decide the CPU operating frequency. A small value will get a higher frequency.
3.2 The user program EPROM should be installed in U2.
3.3 The user program area is from 8000H-FFFFH.
3.4 The pull-up resistors should be added externally. The resistance of pull-up should be greater than 200K ohm.
3.5 SOUND1 is used to drive speaker. If SOUND1 pin is used as an output, then please cut the trace between U3-97 and the base of Q1. Then add a jumper wire from U3-97 to JP3-17.

4. Rework instructions for KP-2027 PCB.

4.1 Remove C3.
4.2 Isolate the left end of R3 from Vcc and add a jumper wire from the left end of R3 to XOSC2.
4.3 Add a jumper wire from J7 to U3-77.
4.4 Add a jumper wire from U3-96 to JP3-19.
4.5 Add a jumper wire from U3-97 to JP3-17.


TP1
CPU CLK
S1
STD CPU
KC5713 CPU
U1
U2
U3
KC5731
C6502
27512
S2
INT. CPU
EXT. CPU
S3
IC ON
IC OFF
TP2
JP1
HEADER 30X2
JP2
HEADER 25X2
JP3
HEADER 17X2
R1
10K
R2
24K
R3
620K
C1
22p
C2
22p
Y1
32768Hz
S4
XTAL
RC
C3
10p
Note : 1. Remove C3 .
2. One end of R3 change from Vdd to XOSC2.
S5
/RESET
C4
0.1u
Note : R4 is used to adjust voice output volume and quality.
S6
INT SPK
EXT SPK
LS1
SPEAKER
Q1
2N8050
R4
R
J10
HEADER 2
J1
PHONEJACK
D1
DIODE
D2
DIODE
D4
DIODE
D5
DIODE
C6
10u
U4
LM7805
VIN
VOUT
GND
VDD
EXT PWR
REG PWR
S7
C5
10u
R5
330
D3
LED
TP3
S8
ON
OFF
Title
Emulator
Size
B
Document Number
STK55C322/324
Rev
A
Date:
Monday, June 21, 1999
Sheet
1
of
1

Customer Information Sheet for STK55C322/324 990524

1. Customer's Name : _____

2. Project title : _____

3. Syntek part number : _____ (will be filled by Syntek.)

4. Package ---------- ( ) Chip ( ) QFP

5. Options :

LCD display clock ---------- ( ) RC ( ) 32768Hz crystal

	Port 1							
	7	6	5	4	3	2	1	0
Pull-up								

6. Customer code :

Code form ---------- ( ) EPROM ( ) file _____

Checksum ---------- 8000-9FFF _____H

A000-BFFF _____H

C000-DFFF _____H

E000-FFFF _____H

8000-FFFF _____H

7. Operating conditions :

All the operating conditions listed below are for Syntek reference. Syntek will not guaranty on these values. Please refer to data book or contact Syntek for the guaranty values.

Operating voltage : _____-_____ V

Operating current : _____ mA Operating frequency : _____ Hz

Sleep current :

Mode 1 : _____ µA (LCD off)

Mode 2 : _____ µA (LCD on), _____ µA (LCD off)

Customer : _____ Salesman : _____Date : __/__/__

Check List before release the code to mask

Item	YES	NO	Check item	Action
1			No problem is found in internal CPU mode.	Set S2 to INT. CPU and run the program.
2			The operating current is acceptable	Set S3 off. Measure the current on TP2.
3			The sleep current is acceptable.	Same as item 2.
4			The CPU frequency is correct.	Check TP1.
5			The 32768Hz frequency is correct	Check XOSC2.
6			The pull-up resistance is greater than 200K ohm.	