HM6789 Series — Maintenance Only

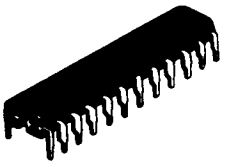
Refer to HM6789HA Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

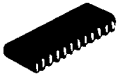
- Super Fast Access Time: . . . . . 25/30 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 230 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789P Series



(DP-24NC)

HM6789JP Series

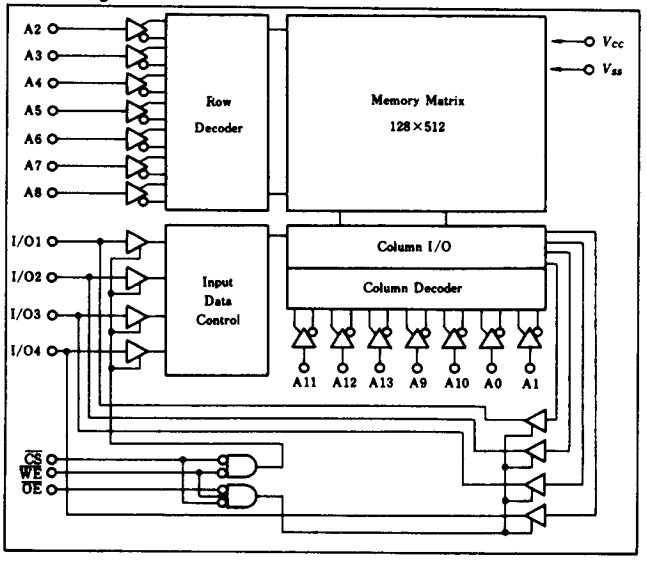


(CP-24D)

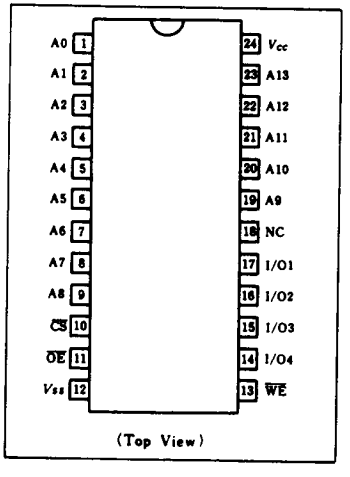
Ordering Information

Type No.	Access Time	Package
HM6789P-25 HM6789P-30	25ns 30ns	300 mil 24 pin plastic DIP
HM6789JP-25 HM6789JP-30	25ns 30ns	300 mil 24 pin Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns.

Function Table

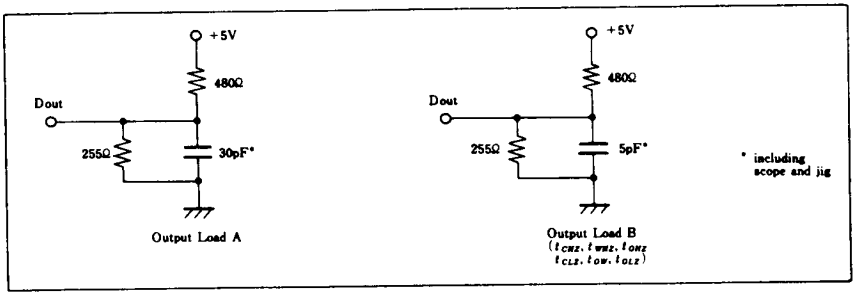
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Din	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} – 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	0	–	0	–	ns
Output Enable to Output Valid	t_{OE}	0	15	0	15	ns
Output Enable to Output in Low Z	t_{OLZ}*1	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Input Voltage Rise/Fall Time	t_T*2	–	150	–	150	ns

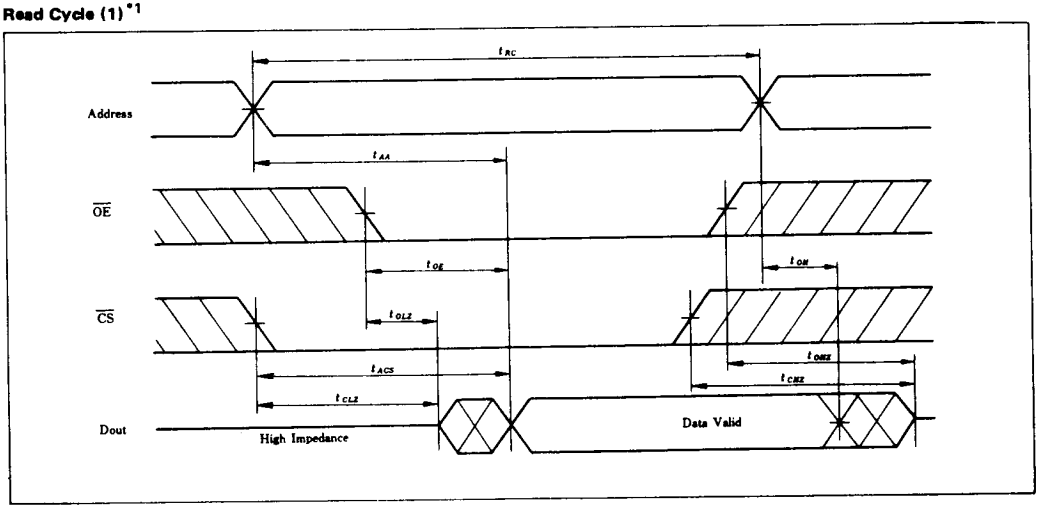
Write Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	30	–	ns
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	20	–	25	–	ns
Write Pulse Width	t_{WP}	20	–	25	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}*1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	–	20	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Output Disable to Output in Hihg Z	t_{OHZ}*1	0	10	0	10	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

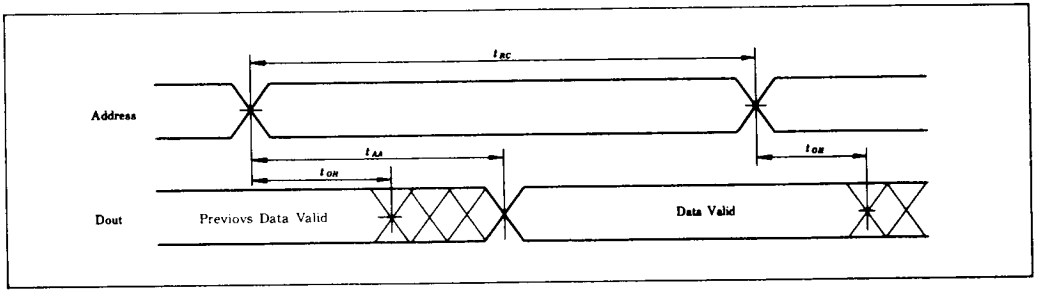
Notes) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.
*2. If t_T becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi Sales Dept. regarding specification.

Timing Waveform

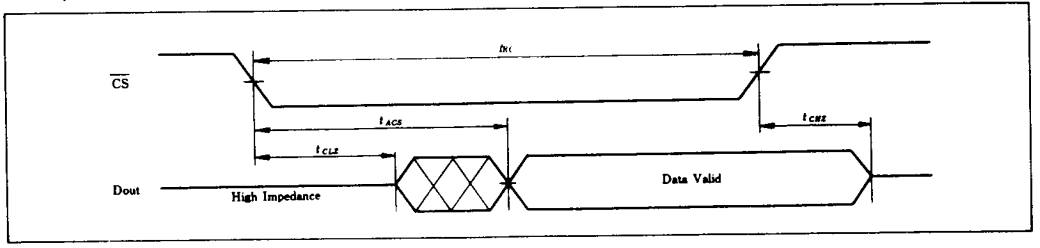
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

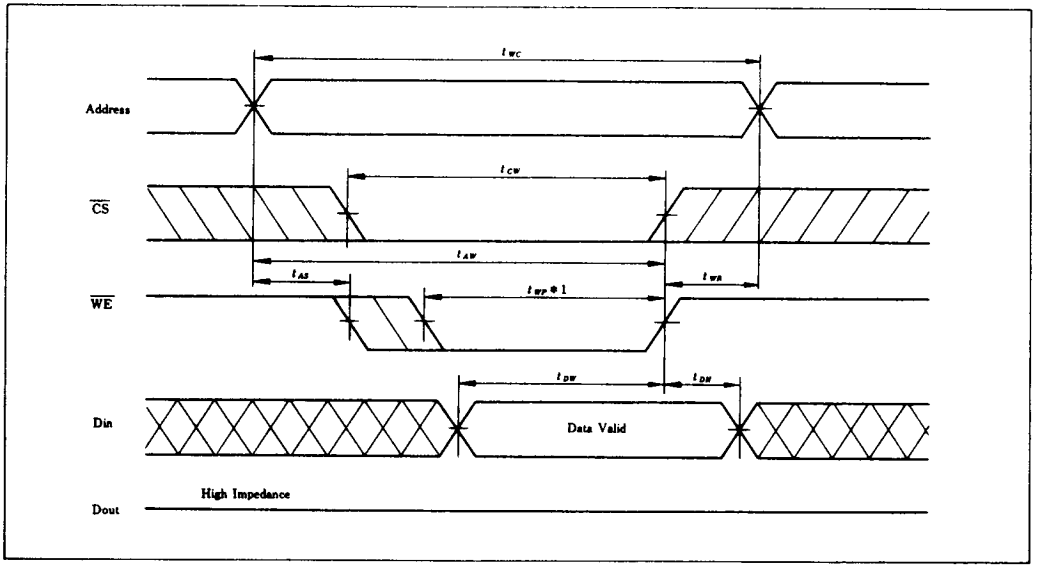


Read Cycle (3) *1, *3, *4

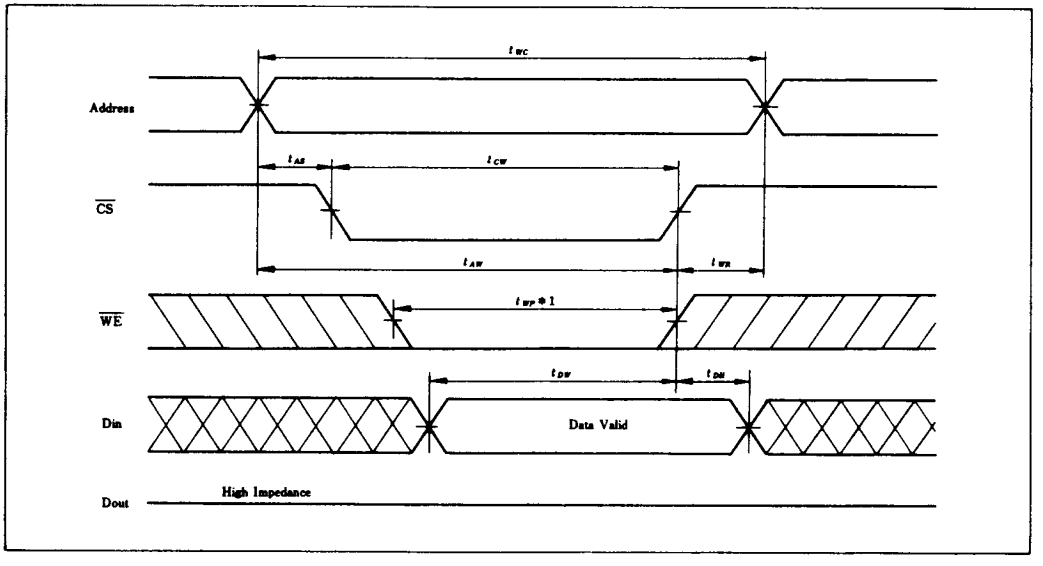


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

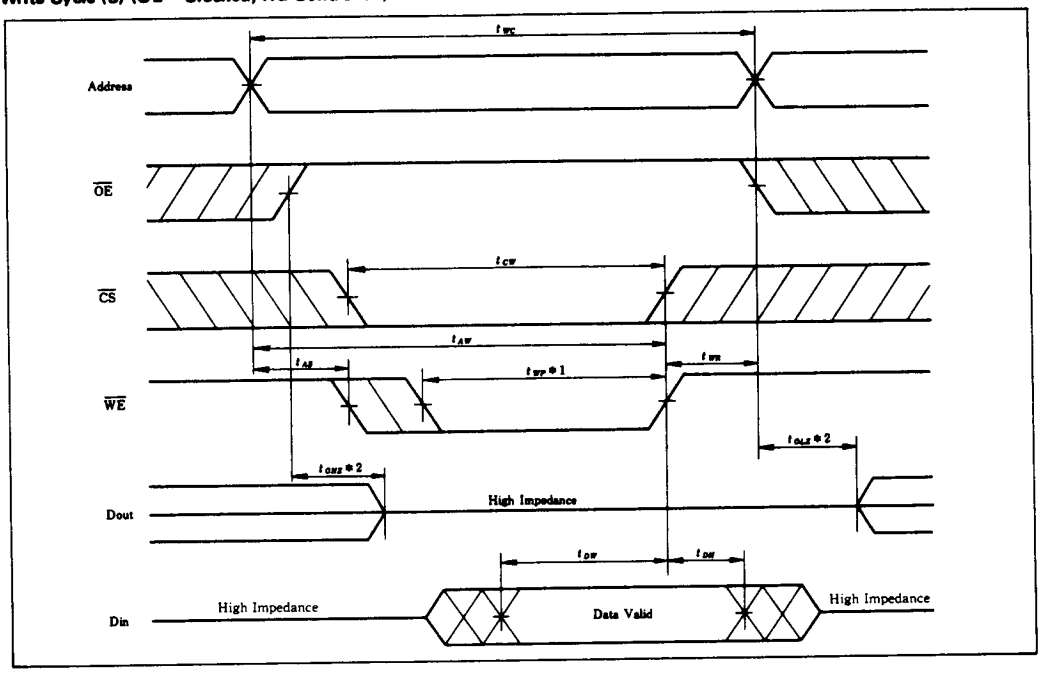
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



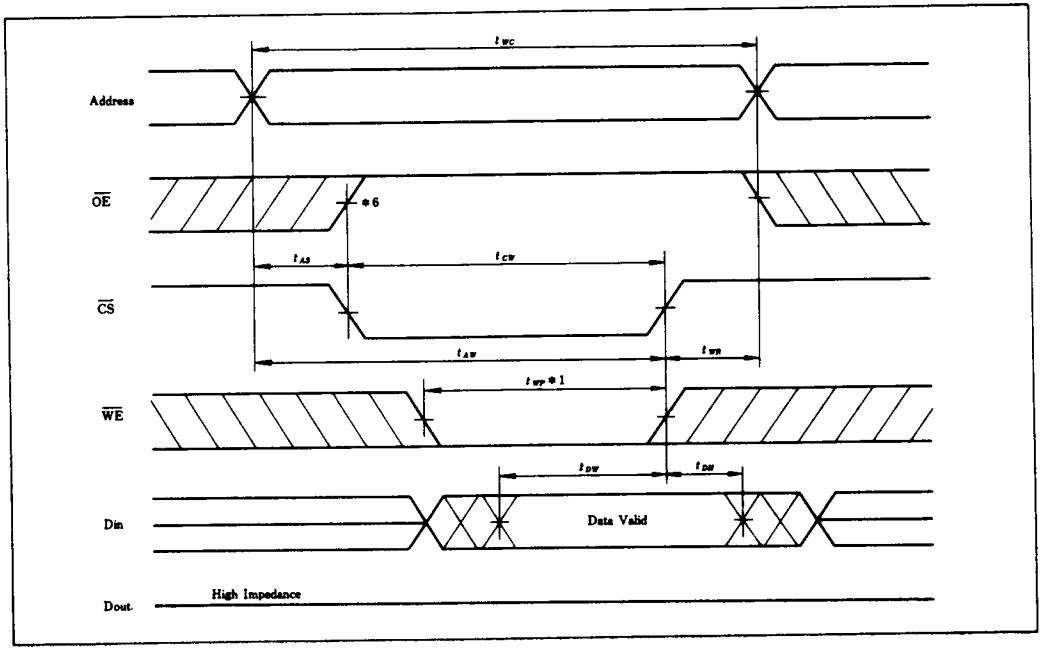
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



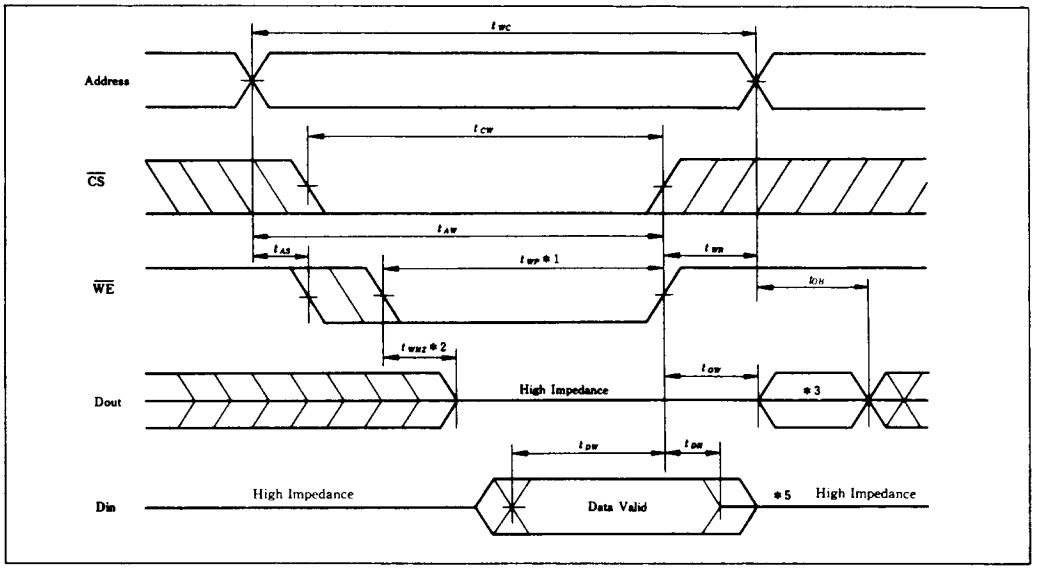
Write Cycle (3) ($\overline{OE}$ - Clocked, $\overline{WE}$ Controlled)



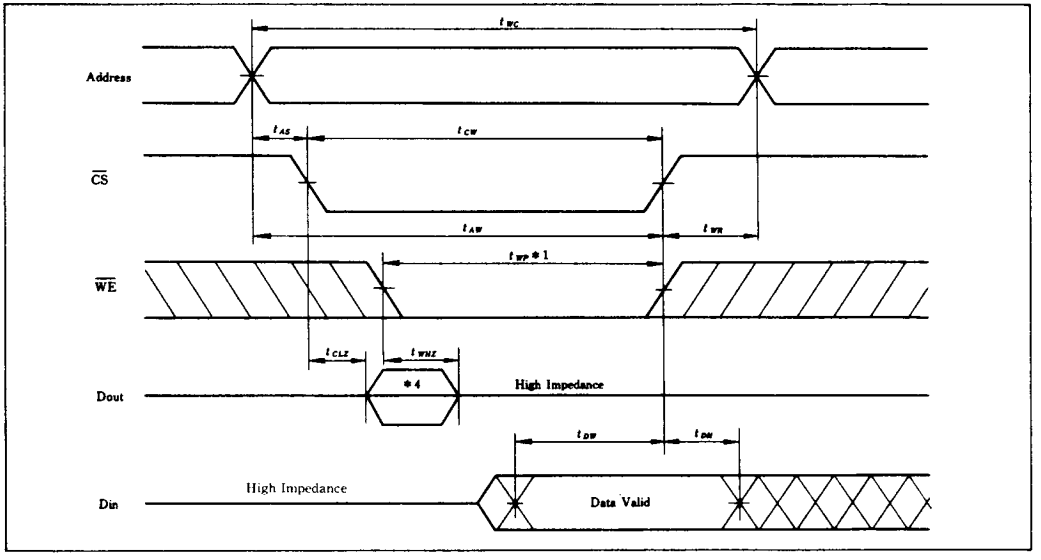
Write Cycle (4) ($\overline{OE}$ - Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Dout is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.