74C Family Characteristics

Fairchild Semiconductor
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FAIRCHILD SEMICONDUCTOR TM

INTRODUCTION

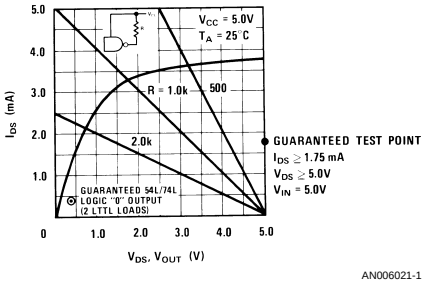
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

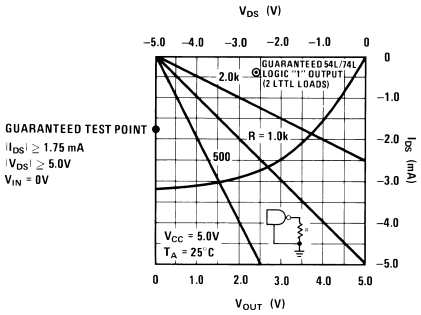
With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

Figure 1 and *Figure 2* show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to Application Note AN-77, "CMOS, The Ideal Logic Family". Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.

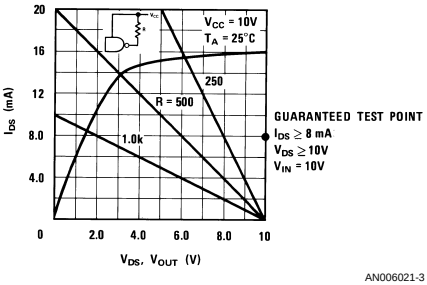


(A) Typical Output Sink Characteristic (N-Channel)



(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1.



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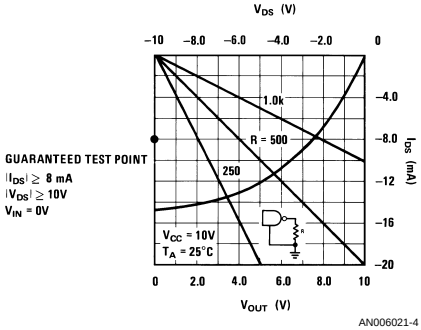


(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2.

The 54C/74C family is designed so that the output characteristics of all devices are matched as closely as possible. To ensure uniformity all devices are tested at four output conditions (see *Figure 1* and *Figure 2*). These points are:

V_{CC} = 5.0V	V_{IN} = 5.0V $I_{DS} \geq$ 1.75 mA $V_{DS} \geq$ 5.0V	V_{IN} = 0V $\|I_{DS}\| \geq$ 1.75 mA $\|V_{DS}\| \geq$ 5.0V
V_{CC} = 10V	V_{IN} = 10V $I_{DS} \geq$ 8.0 mA $V_{DS} \geq$ 10V	V_{IN} = 0V $\|I_{DS}\| \geq$ 8.0 mA $\|V_{DS}\| \geq$ 10V

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. *Figure 1* and *Figure 2* show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at V_{CC} = 5.0V, V_{OUT} = 1.5V (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at V_{CC} = 5.0V.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the I_{DS} = 0 axis and the output will then typically switch to either V_{CC} or ground.

NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

The transfer characteristic of *Figure 3* shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.

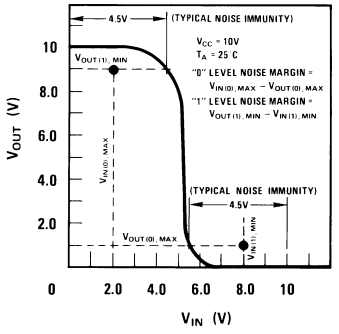


FIGURE 3. Typical Transfer Characteristics

All 54C/74C devices are guaranteed to have a noise margin of 1.0V or greater over all operating conditions (see *Figure 4*).

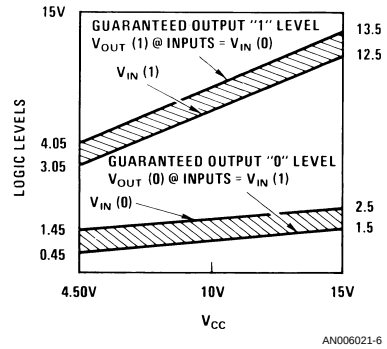
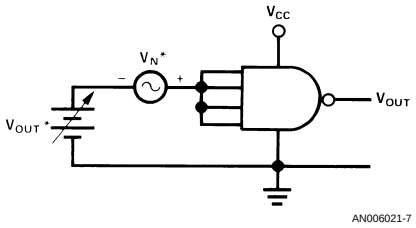


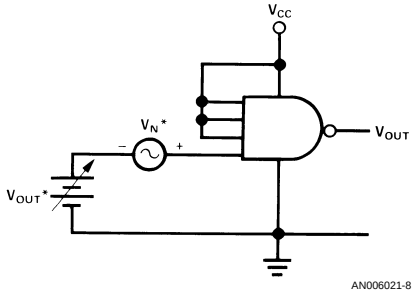
FIGURE 4. Guaranteed Noise Margin over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. *Figure 5* indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.



(A)



*V_{OUT} = $V_{OUT\ (1)\ MIN}$, $V_{OUT\ (0)\ MAX}$
V_N = Allowable Noise Voltage = 1.0V

(B)

FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in *Figure 5*.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current; (2) transient power due to load capacitance; (3) transient power due to internal capacitance and; (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is 1/2 CV^2. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then $2[(1/2)\ CV_{CC}^2] = CV_{CC}2$. Energy per unit time, or power, is then $CV_{CC}^2\ f$, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in Application Note AN-77. The expression is:

$$P_{VI} = \frac{1}{2}(V_{CC} - 2\ V_T)\ I_{CC(MAX)}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

Power (no load) = $C_{PD}\ V_{CC}2\ f$

The total power consumption is then simplified to:

Total Power = $(C_{PD} + C_L)\ V_{CC}2\ f + I_{LEAK}\ V_{CC}$(1)

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further *Figure 6* gives a graph of normalized power vs frequency for different power supply

voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.

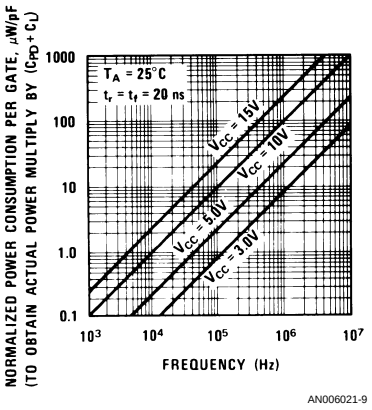


FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10 μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\ \mu\text{W}}{\text{pF}} \times (12\ \text{pF} + 50\ \text{pF}) = \frac{0.62\ \text{mW}}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ \text{mW} + 0.01\ \mu\text{A} \times 10\text{V} \cong 2.48\ \text{mW}$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}2\ f$. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even though the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD}\ V_{CC}^2\ f}_{\text{no load power}} + \underbrace{C_L\ V_{CC}^2\ \frac{f}{2}}_{\substack{\text{output power of} \\ \text{1st stage}}} + \underbrace{C_L\ V_{CC}^2\ \frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L\ V_{CC}^2\ \frac{f}{8}}_{\text{3rd stage}} + \underbrace{2\ C_L\ V_{CC}^2\ \frac{f}{16}}_{\substack{\text{4th stage} \\ \text{\& carry} \\ \text{output}}} + \underbrace{I_L\ V_{CC}}_{\substack{\text{leakage} \\ \text{term}}}$$

This reduces to:

$P_{TOTAL} = (C_{PD} + C_L)\ V_{CC}2\ f + I_L\ V_{CC}$

From the data sheet C_{PD} = 90 pF and I_L = 0.05 μA. Using *Figure 6* total power is then:

$$P_{TOTAL} = (90\ \text{pF} + 50\ \text{pF}) \times \frac{100\ \mu\text{W}}{\text{pF}} +$$
$$0.05 \times 10^{-6} \times 10\text{V} \cong 14\ \text{mW}$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of *Figure 6* and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF *and input rise and fall times of 20 ns.* A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF

fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

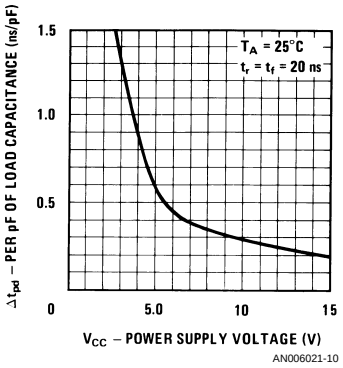


FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem *Figure 7* has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

$$t_{pd}\Big|_{C_L = C} = (C - 50)\ \text{pF} \times \frac{\Delta t_{pd}}{\text{pF}} + t_{pd}\Big|_{C_L = 50\ \text{pF}}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50\ \text{pF}}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\frac{\Delta t_{pd}}{\text{pF}}$ = Value obtained from *Figure 7*.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15\ \text{pF}} = (15 - 50)\ \text{pF} \times 0.57\frac{\text{ns}}{\text{pF}} + 50\ \text{ns}$$

$$= -20\ \text{ns} + 50\ \text{ns} = 30\ \text{ns}$$

The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100\ \text{pF}} = (100 - 50)\ 0.29\ \text{ns} + 70\ \text{ns}$$

$$= 14.5 + 70 \cong 85\ \text{ns}$$

It is significant to note that this equation and *Figure 7* apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller Δt_{pd}/pF.

Another point to consider in the design of a CMOS system is the effect of power supply voltage on propagation delay. *Figure 8* shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.

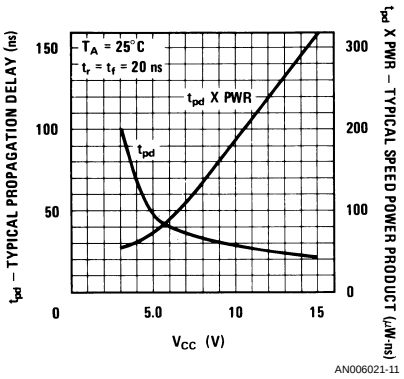


FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

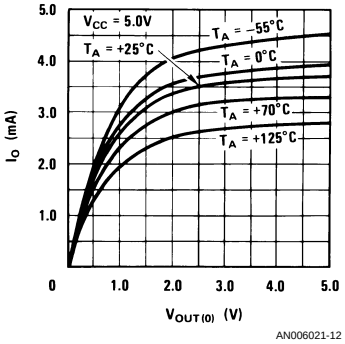
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out". Going from *V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%.* Clearly for V_{CC} > 10V a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However, in general it can be seen from *Figure 8* that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

TEMPERATURE CHARACTERISTICS

Figure 9 and *Figure 10* give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The effect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependence of t_{PD} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.



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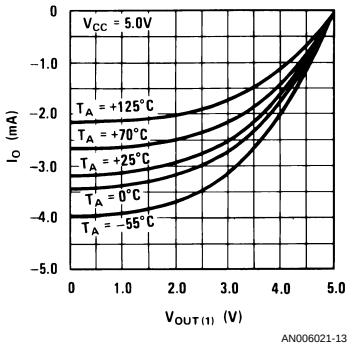
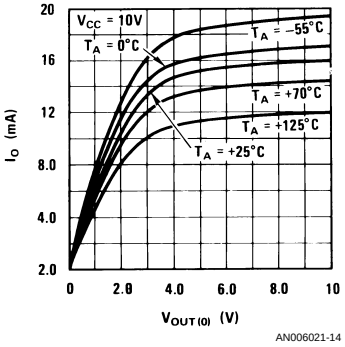


(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9.



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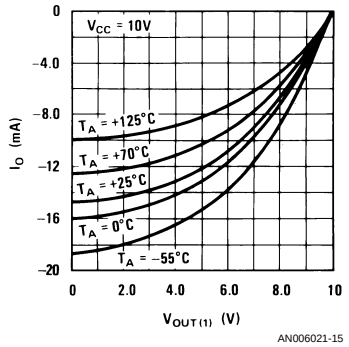

(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10.

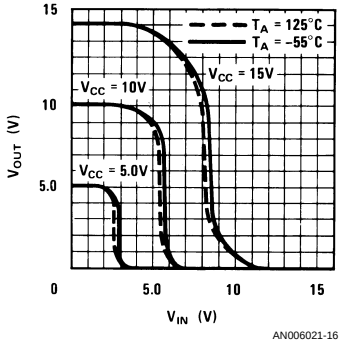

FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of *Figure 9* and *Figure 10* show considerable variation with temperature. Examination of the transfer characteristics of *Figure 11* indicates that they are almost independent of temperature. The transfer characteristic is not dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independence of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

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