National Semiconductor Corporation

ADVANCED INFORMATION

microCMOS

NMC6164AN/6164AN-L 8192 x 8-Bit Static RAM

March 1987

General Description

The NMC6164A/6164AN-L is an 8192 by 8-bit, new generation, static RAM. It is fabricated with National's proprietary microCMOS double-polysilicon technology which combines high performance and high density with low power consumption and excellent reliability.

The NMC6164A/6164AN-L operates with a single 5V power supply with ±10% tolerance. Additional battery back-up operation is available (L version) for data retention down to 2V, with low standby current.

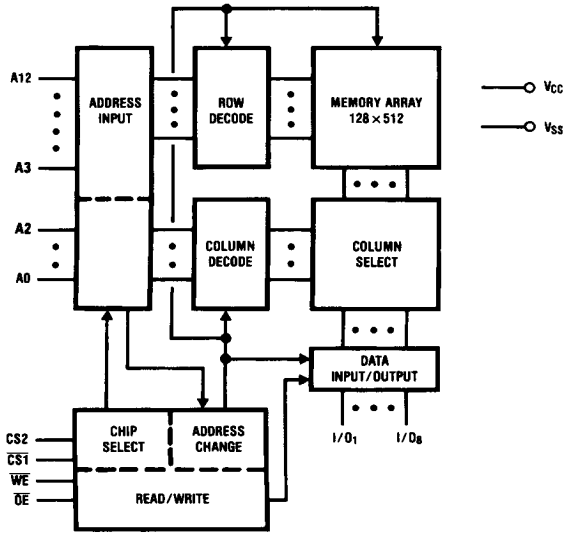
Packaging is available in standard 28-pin plastic DIP.

In addition to the inputs and outputs being TTL compatible, the outputs are also CMOS compatible, in that capacitive loads are driven to V_{CC} or V_{SS}.

Features

- Single power supply: 5V ±10%
- Fast access time 45 ns/55 ns/70 ns max
- Equal access and cycle times
- Completely static RAM: no clock or timing strobe required
- Low standby power and low power operation
  - Standby: 10 μW, typical
  - Operation: 10 mW/MHz, typical
- Battery back-up operation available (L version) with data retention supply voltage: 2V–5.5V
- Common data input and output, TRI-STATE® output
- TTL compatible: all inputs and outputs
- CMOS compatible: outputs drive capacitive loads to V_{CC} or V_{SS}
- Standard 28-pin package configuration

Block and Connection Diagrams



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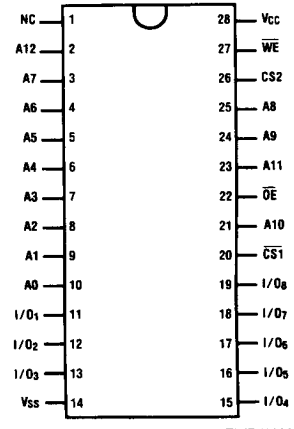
Dual-In-Line Package



Top View

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Order Number NMC6164AN or NMC6164AN-L
See NS Package Number N28B

Order Number / Parameter	NMC6164AN-45L	NMC6164AN-45	NMC6164AN-55L	NMC6164AN-55	NMC6164AN-70L	NMC6164AN-70
Access Time (ns)	45	45	55	55	70	70
I_{CC} Standby, CMOS	100 μA	2 mA	100 μA	2 mA	100 μA	2 mA

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Relative to V_{SS}	−0.6V to +7V
Storage Temperature, T_{STG}	−55°C to +125°C
Temperature Under Bias, T_{BIAS}	−10°C to +85°C
Power Dissipation, P_D	1.0W
Current Through Any Pin	100 mA

ESD rating to be determined.

Recommended DC Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
V_{SS} Supply Voltage	0	0	V
V_{IH}, Input High Voltage (Logic 1)			
TTL	2.2	6.0	V
CMOS	V_{CC} − 0.2	V_{CC} + 0.2	V
V_{IL}, Input Low Voltage (Logic 0)			
TTL	−0.3	0.8	V
CMOS	−0.3	0.2	V
T_{OPR}, Operating Temp	0	70	°C

DC Electrical Characteristics at recommended operating conditions

Symbol		Parameter	Conditions	Min	Max	Units
I_{LI}		Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	−2	2	μA
I_{LO}		Output Leakage Current	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	−2	2	μA
I_{CC}		Active Quiescent Current, TTL	All Inputs at TTL Levels		25	mA
I_{CC}	Std	Active Quiescent Current, CMOS	All Inputs at CMOS Levels		2	mA
	L				100	μA
I_{CC1}		Average Operating Current, TTL	$t_{RC} = t_{RC}$ Min $\overline{CS1} = V_{IL}$ TTL and CS2 = V_{IH} TTL $I_{I/O}$ = 0 mA All Inputs at TTL Levels		50	mA
		Average Operating Current, CMOS	$t_{RC} = t_{RC}$ Min $\overline{CS1} = V_{IL}$ CMOS and CS2 = V_{IH} CMOS $I_{I/O}$ = 0 mA All Inputs at CMOS Levels		30	mA
I_{SB}	Std	Standby Power Supply Current	$\overline{CS1} = V_{IH}$ TTL or CS2 = V_{IL} TTL		4	mA
	L				2	mA
I_{SB1}	Std	Standby Power Supply Current	$\overline{CS1} = V_{IH}$ CMOS or CS2 = V_{IL} CMOS		2	mA
	L				100	μA
V_{OL}		Output Low Voltage, TTL	I_{OL} = 8 mA		0.4	V
		Output Low Voltage, CMOS	I_{OL} = ±10 μA	−0.2	0.2	V
V_{OH}		Output High Voltage, TTL	I_{OH} = −4.0 mA	2.4		V
		Output High Voltage, CMOS	I_{OH} = ±10 μA	V_{CC} − 0.2	V_{CC} + 0.2	V

Capacitance

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V (Note 5)	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V (Note 5)	10	pF

Truth Table

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	Current
Not Selected (Power Down)	*	H	*	*	Hi-Z	I_{SB}, I_{SB1}
	*	*	L	*	Hi-Z	I_{SB}, I_{SB1}
Output Disabled	H	L	H	H	Hi-Z	I_{CC}, I_{CC1}
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}
Write	L	L	H	*	D_{IN}	I_{CC}, I_{CC1}

*Don't Care (H or L) H = Logic HIGH Level L = Logic LOW Level

AC Electrical Characteristics* (Note 1)

Symbol	Parameter	NMC6164AN/6164AN-L						Units
		-45		-55		-70		
		Min	Max	Min	Max	Min	Max	
READ CYCLE (Note 4)								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address Access Time		45		55		70	ns
t_{CO1}	Chip Selection ($\overline{CS1}$) to Output Valid		45		55		70	ns
t_{CO2}	Chip Selection (CS2) to Output Valid		45		55		70	ns
t_{OE}	Output Enable ($\overline{OE}$) to Output Valid		20		25		30	ns
t_{LZ1}	Chip Selection ($\overline{CS1}$) to Output Active (Note 12)	15		15		15		ns
t_{LZ2}	Chip Selection (CS2) to Output Active (Note 12)	15		15		15		ns
t_{OLZ}	Output Enable ($\overline{OE}$) to Output Active (Note 12)	5		5		5		ns
t_{HZ1}	Chip Deselection ($\overline{CS1}$) to Output in Hi-Z (Notes 2 and 3)	0	20	0	25	0	30	ns
t_{HZ2}	Chip Deselection (CS2) to Output in Hi-Z (Notes 2 and 3)	0	20	0	25	0	30	ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z (Notes 2 and 3)	0	15	0	20	0	25	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{CW1}	Chip Selection ($\overline{CS1}$) to End of Write (Note 10)	40		50		60		ns
t_{CW2}	Chip Selection ($\overline{CS2}$) to End of Write	40		50		60		ns
t_{AS}	Address Setup Time (Note 7)	0		0		0		ns
t_{AW}	Address Valid to End of Write	40		50		60		ns
t_{WP}	Write Pulse Width (Note 6)	35		40		50		ns
t_{WR1}	Write Recovery Time from $\overline{CS1}$ (Note 8)	0		0		0		ns
t_{WR2}	Write Recovery Time from CS2 (Note 8)	0		0		0		ns
t_{WHZ}	Beginning of Write to Output in Hi-Z (Note 9)	0	15	0	20	0	25	ns
t_{DW}	Data Valid to Write Time Overlap	20		25		35		ns
t_{DH}	Data Hold from End of Write	0		0		0		ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z	0	15	0	20	0	25	ns
t_{OW}	Output Active from End of Write	0		0		0		ns

*Applies to Standard and L Versions.

Note 1: AC test conditions T_A = 0°C to +70°C, V_{CC} = 5V ±10%.

Note 2: t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are determined as:
High to TRI-STATE, measured V_{OH} (DC) −0.10V
Low to TRI-STATE, measured V_{OL} (DC) +0.10V

Note 3: At any given temperature and voltage condition, $t_{HZ\ MAX}$ is less than $t_{LZ\ MIN}$, both for a given device and from device to device (guaranteed, not tested).

Note 4: $\overline{WE}$ is high for read cycle.

Note 5: T_A = 25°C, f = 1.0 MHz. This parameter is sampled and not 100% tested.

Note 6: A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$ and a high CS2 and a low $\overline{WE}$.

Note 7: t_{AS} is measured from the address changes to the beginning of the write.

Note 8: t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of the write cycle.

Note 9: If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. At this time, the data input signals of opposite phase to the outputs must not be applied.

Note 10: If the $\overline{CS1}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the outputs will remain in a Hi-Z state.

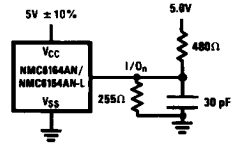
Note 11: CS2 controls the address buffers, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, D_{IN} buffer and $\overline{OE}$ buffer. When CS2 controls the data retention mode, all inputs (address, I/O, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$) can be in the high impedance state. When $\overline{CS1}$ controls the data retention mode, CS2 must be at V_{IH}, CMOS. All other input levels (address, $\overline{OE}$, $\overline{WE}$, I/O) can be in the high impedance state.

Note 12: Output active level is defined as steady state TRI-STATE level ±0.1V.

AC Test Conditions

Input pulse levels	V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall times	5 ns
All Input timing reference levels	1.5V
Output timing reference levels	V_{OH} = 2.0V, V_{OL} = 0.8V

AC Test Load



(Including Jig & Probe Capacitance)

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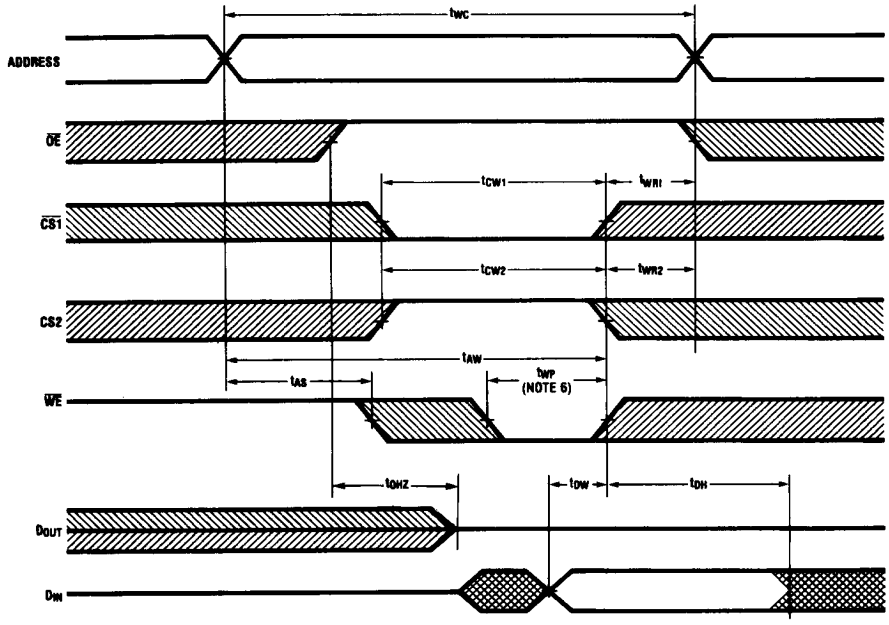
Timing Waveforms

Write Cycle 1 ($\overline{OE}$ Clocked)



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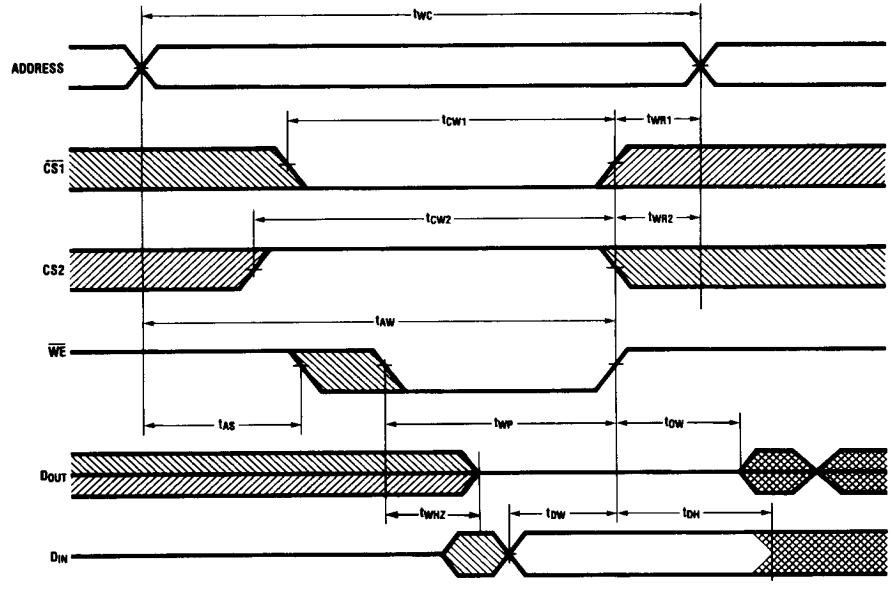
Write Cycle 2 ($\overline{OE}$ Low Fixed)



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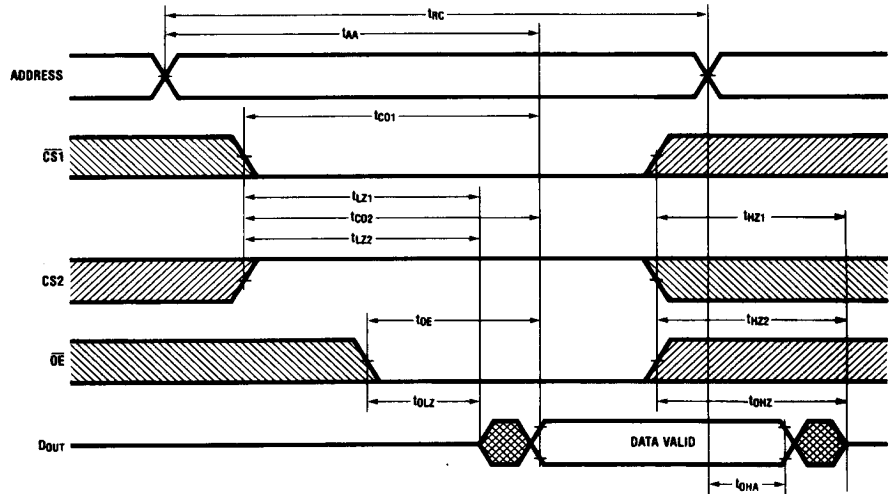
Timing Waveforms (Continued)

Read Cycle ($\overline{WE}$ = V_{IH})



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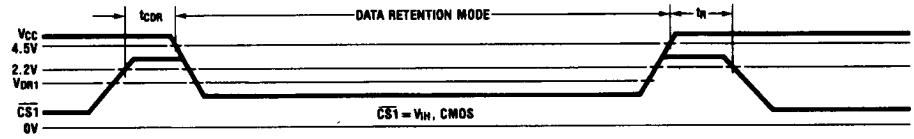
Low V_{CC} Data Retention (L Version)

Symbol	Parameter	Conditions	Min	Max	Units
V_{DR1}	V_{CC} for Data Retention	$\overline{CS1}$ > V_{IH}, CMOS (Note 11) CS2 > V_{IH}, CMOS	2.0	5.5	V
V_{DR2}	V_{CC} for Data Retention	CS2 < V_{IL}, CMOS (Note 11)	2.0	5.5	V
I_{CCDR1}	Data Retention Current	V_{CC} = 2V $\overline{CS1}$ > V_{IH}, CMOS CS2 > V_{IH}, CMOS		40	μA
I_{CCDR2}	Data Retention Current	V_{CC} = 2V CS2 < V_{IL}, CMOS		40	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}		ns

Low V_{CC} Data Retention Waveforms

No. 1 ($\overline{CS1}$ Controlled)



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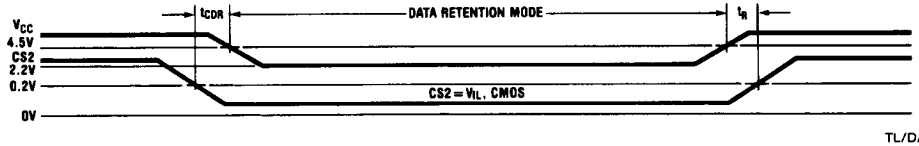
No. 2 (CS2 Controlled)



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