

MITSUBISHI MICROCOMPUTERS

M37207MF-XXXSP/FP, M37207M8-XXXSP

M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37207MF-XXXSP/FP and M37207M8-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 80-pin plastic molded QFP.

In addition to their simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

The M37207MF-XXXSP/FP has a PWM function and an OSD function, so it is useful for a channel selection system for TV. The features of the M37207EFSP/FP are similar to those of the M37207MF-XXXSP/FP except that these chips have a built-in PROM which can be written electrically. The difference between M37207MF-XXXSP/FP and M37207M8-XXXSP are the ROM size, RAM size, ROM size for display and kinds of character. Accordingly, the following descriptions will be for the M37207MF-XXXSP/FP unless otherwise noted.

FEATURES

- Number of basic instructions 71
- Memory size
 - ROM 32K bytes (M37207M8-XXXSP)
 - 62K bytes (M37207MF-XXXSP/FP,
 - M37207EFSP/FP)
 - RAM 512 bytes (M37207M8-XXXSP)
 - 960 bytes (M37207MF-XXXSP/FP,
 - M37207EFSP/FP)
 - ROM correction memory 64 bytes
 - ROM for display 8K bytes (M37207M8-XXXSP)
 - 12K bytes (M37207MF-XXXSP/FP,
 - M37207EFSP/FP)
 - RAM for display 144 bytes
- Minimum instruction execution time 0.5 μ s (at 8 MHz oscillation frequency)
- Power source voltage 5 V $\pm$ 10 %
- Subroutine nesting 128 levels (Max.)
- Interrupts 15 types, 14 vectors
- 8-bit timers 6
- Programmable I/O ports (Ports P0, P1, P2, P30–P36, P4, P6) 47
- Input ports (Ports P70, P71) 2
- Output ports (Ports P52–P56) 5
- 12 V withstand ports 10
- LED drive ports 4
- Serial I/O 8-bit X1 channel (2 systems)

- Multi-master I²C-BUS interface 1 (3 systems)
- Power dissipation
 - In high-speed mode 165 mW
 - (at V_{CC} = 5.5 V, 8 MHz oscillation frequency, CRT on)
 - In low-speed mode 0.33 mW
 - (at V_{CC} = 5.5 V, 32 kHz oscillation frequency)
- A-D comparator (6-bit resolution) 8 channels
- PWM output circuit 14-bit X1, 8-bit X10
- Interrupt interval determination circuit 1
- ROM correction function 32 bytes X 2
- CRT display function
 - Number of display characters 24 characters X 3 lines
 - (16 lines maximum)
 - Kinds of characters 256 kinds (M37207M8-XXXSP)
 - 384 kinds (M37207MF-XXXSP/FP,
 - M37207EFSP/FP)
 - Character display area 12 X 16 dots
 - Kinds of character sizes 4 kinds
 - Kinds of character colors (It can be specified by the character)
 - maximum 15 kinds (R, G, B, I)
 - Kinds of character background colors (It can be specified by the character)
 - maximum 7 kinds (R, G, B)
 - 1/2-character unit color specification is possible.
 - Kinds of raster colors (maximum 15 kinds)
 - Display position
 - Horizontal 64 levels
 - Vertical 128 levels
 - Bordering (horizontal and vertical)
 - Wipe function
 - Scanning line double count mode display is possible.

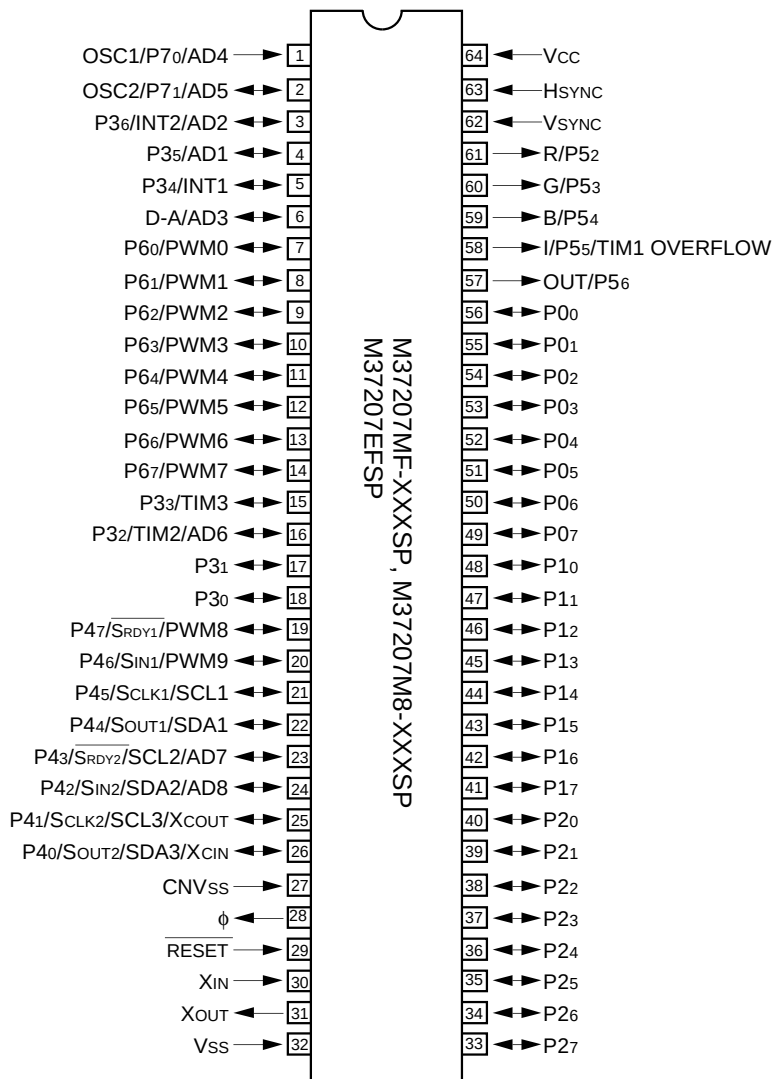
APPLICATION

TV

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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PIN CONFIGURATION (TOP VIEW)

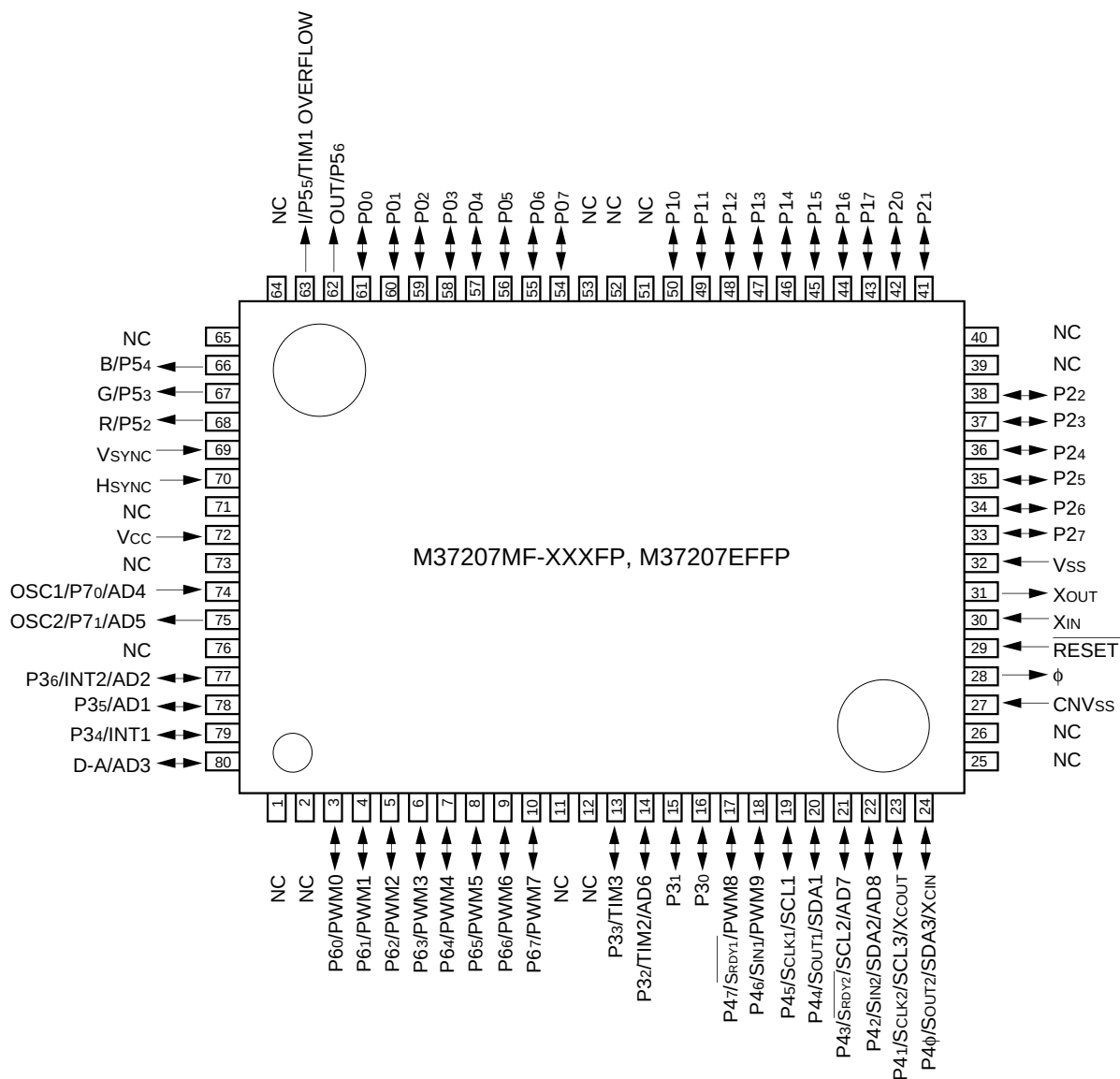


Outline 64P4B

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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PIN CONFIGURATION (TOP VIEW)



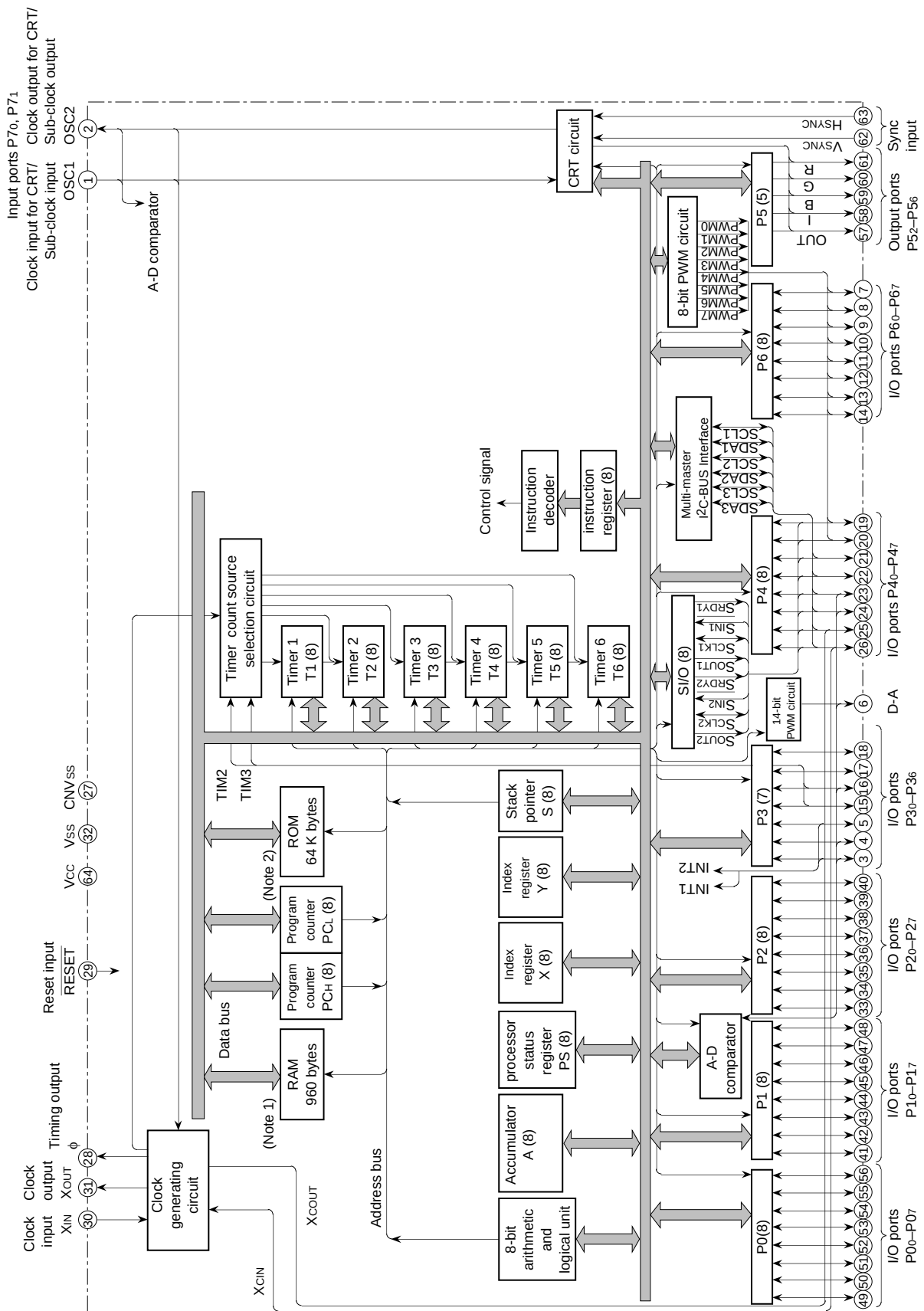
Outline 80P6N-A

NC: Unconnected

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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FUNCTIONAL BLOCK DIAGRAM of M37207M8-XXXSP



Note 1: M37207M8-XXXSP has a 512 bytes RAM.
Note 2: M37207M8-XXXSP has a 32 K bytes ROM.

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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FUNCTIONS

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 ms (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM	M37207M8-XXXSP	32 K bytes
		M37207MF-XXXSP/FP, M37207EFSP/FP	64 K bytes
	RAM	M37207M8-XXXSP	512 bytes
		M37207MF-XXXSP/FP, M37207EFSP/FP	960 bytes
	ROM correction memory		64 bytes
	CRT ROM	M37207M8-XXXSP	8K bytes
		M37207MF-XXXSP/FP, M37207EFSP/FP	12K bytes
	CRT RAM		144 bytes
Input/Output ports	P00–P07	I/O	8-bit X 1 (CMOS input/output structure)
	P10–P17	I/O	8-bit X 1 (CMOS input/output structure)
	P20–P27	I/O	8-bit X 1 (CMOS input/output structure)
	P30, P31	I/O	2-bit X 1 (CMOS input/output structure)
	P32–P36	I/O	5-bit X 1 (N-channel open-drain output structure, can be used as external clock input pins, A-D input pins, INT input pins)
	P40–P47	I/O	8-bit X 1 (N-channel open-drain output structure, can be used as serial I/O pins, A-D input pins, PWM output pins, multi-master I ² C-BUS interface, sub-clock I/O pins)
	P52–P56	Output	5-bit X 1 (CMOS output structure, can be used as CRT output pins, an external clock output pin)
	P60–P67	I/O	8-bit X 1 (N-channel open-drain output structure, can be used as PWM output)
	P70, P70	Input	2-bit X 1 (can be used as CRT display clock I/O pins, analog input pins)
Serial I/O			8-bit X 1 (2 systems)
Multi-master I ² C-BUS interface			1 (3 systems)
A-D comparator			8 channels (6-bit resolution)
PWM output circuit			14-bit X 1, 8-bit X 10
Timers			8-bit timer X 6
ROM correction function			32 bytes X 2
Subroutine nesting			128 levels (maximum)
Interrupt interval determination circuit			1
Interrupt			External interrupt X 2, Internal timer interrupt X 6, Serial I/O interrupt X 1, CRT interrupt X 1, Multi-master I ² C-BUS interface interrupt X 1, f(Xin)/4096 interrupt X 1, Vsync interrupt X 1, BRK interrupt X 1
Clock generating circuit			2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)

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FUNCTIONS (continued)

Parameter			Functions
Power source voltage			5 V ± 10 %
Power dissipation	In high-speed mode	CRT ON	165 mW typ. (at oscillation frequency f(XIN) = 8 MHz, fosc = 8 MHz)
		CRT OFF	82.5 mW typ. (at oscillation frequency f(XIN) = 8 MHz)
	In low-speed mode	CRT OFF	0.33 mW typ. (at oscillation frequency fCLK = 32 kHz, f(XIN) = stopped)
	In stop mode		1.1 mW (maximum)
Operating temperature range			−10 °C to 70 °C
Device structure			CMOS silicon gate process
Package	M37207MF-XXXSP, M37207M8-XXXSP M37207EFSP		64-pin shrink plastic molded DIP
	M37207MF-XXXFP, M37207EFP		80-pin plastic molded QFP
CRT display function	Number of display characters		24 characters X3 lines (maximum 16 lines by software)
	Character display area		12 X16 dots
	Kinds of characters	M37207M8-XXXSP	256 Kinds
		M37207MF-XXXSP/FP, M37207EFSP/FP	384 Kinds
	Kinds of character sizes		4 kinds
	Kinds of character colors		Maximum 15 kinds (R, G, B, I); can be specified by the character
Display position (horizontal, vertical)		64 levels (horizontal) X 128 levels (vertical)	

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power source		Apply voltage of 5 V $\pm$ 10 % (typical) to Vcc and AVcc, and 0 V to Vss.
CNVss	CNVss		Connected to Vss.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2 ms or more (under normal Vcc conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
P00–P07	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output. See notes at end of table for full details of port P0 functions.
P10–P17	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
P20–P27	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
P30, P31	I/O port P3	I/O	Ports P30, P31 are 2-bit I/O ports and have basically the same functions as port P0. The output structure is CMOS output.
P32/TIM2/ AD6,	I/O port P3 Analog input External clock input External interrupt input	I/O	Ports P32–P36 are 5-bit I/O ports and have basically the same functions as port P0. The output structure is N-channel open-drain output.
P33/TIM3,		Input	Pins P32, P35, P36 are also used as analog input pins AD6, AD1 and AD2 respectively.
P34/INT1,		Input	Pins P32, P33 are also used as external clock input pins TIM2, TIM3 respectively.
P35/AD1,		Input	Pins P34, P36 are also used as external interrupt input pins INT1, INT2.
P36/INT2/ AD2			
P40/SOUT2/ SDA3/XCIN,	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open-drain output.
P41/SCLK2/ SCL3/ XCOUT, P42/ SIN2/SDA2/ AD8,	Serial I/O data input/output	I/O	Pins P40, P42, P44, P46 are also used as serial I/O data input/output pins SOUT2, SIN2, SOUT1, SIN1 respectively. The output structure is N-channel open-drain output.
	Serial I/O synchronous clock input/output	I/O	Pins P41, P45 are also used as serial I/O synchronous clock input/output pins SCLK2, SCLK1 respectively.
P43/SRDY2/ SCL2/AD7,	Serial I/O receive enable signal output	Output	Pins P43, P47 are also used as serial I/O receive enable signal output pins SRDY2, SRDY1 respectively. The output structure is N-channel open-drain output.
P44/SOUT1/ SDA1,	Multi-master I ² C-BUS interface	I/O	Pins P40–P45 are also used as SDA3, SCL3, SDA2, SCL2, SDA1, SCL1 respectively when multi-master I ² C-BUS interface is used. The output structure is N-channel open-drain output.
P45/SCLK1/ SCL1,	Sub-clock input	Input	Pin P40 is also used as sub-clock input pin XCIN.
P46/SIN1/ PWM9,	Sub-clock output	Output	Pin P41 is also used as sub-clock output pin XCOUT. The output structure is N-channel open-drain output.
P47/SRDY1/ PWM8	Analog input	Input	Pins P42, P43 are also used as analog input pins AD8, AD7 respectively.
	PWM output	Output	Pins P46, P47 are also used as PWM output pins PWM9, PWM8 respectively. The output structure is N-channel open-drain output.

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PIN DESCRIPTION (continued)

Pin	Name	Input/ Output	Functions
R/P52, G/P53, B/P54, I/P55/TIM1 OVERFLOW, OUT/P56	Output port P5	Output	Ports P52–P56 are 5-bit output ports. The output structure is CMOS output.
	CRT output	Output	Pins P52–P56 are also used as CRT output pins R, G, B, I, OUT respectively. The output structure is CMOS output.
	Timer 1 overflow signal output	Output	Pin P55 is also used as timer 1 overflow signal output pin TIM1 OVERFLOW. The output structure is CMOS output.
P60/PWM– P67/PWM7	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open-drain output.
	PWM output	Output	Pins P60–P67 are also used as PWM output pins PWM0–PWM7. The output structure is CMOS output.
OSC1/P70/ AD4, OSC2/P71/ AD5	Input port P7	Input	Ports P70, P71 are 2-bit input port.
	Clock input for CRT display	Input	Pin P70 is also used as CRT display clock input pin OSC1.
	Clock output for CRT display	Output	Pin P71 is also used as CRT display clock output pin OSC2. The output structure is CMOS output.
	Analog input	Input	Pins P70, P71 are also used as analog input pins AD4, AD5 respectively.
HSYNC	HSYNC input	Input	This is a horizontal synchronous signal input for CRT display.
VSNC	VSNC input	Input	This is a vertical synchronous signal input for CRT display.
f	Timing output	Output	This is a timing output pin. This pin has reset-out output function. The output structure is CMOS output.
D-A/AD3	DA output	Output	This is an output pin for 14-bit PWM.
	Analog input	Input	The D-A pin is also used as analog input pin AD3.

Note : As shown in the memory map (Figure 5), port P0 is accessed as a memory at address 00C0₁₆ of zero page. Port P0 has the port P0 direction register (address 00C1₁₆ of zero page) which can be used to program each bit as an input (“0”) or an output (“1”). The pins programmed as “1” in the direction register are output pins. When pins are programmed as “0,” they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output “L” voltage has risen, for example, because a light emitting diode was directly driven. The input pins float, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

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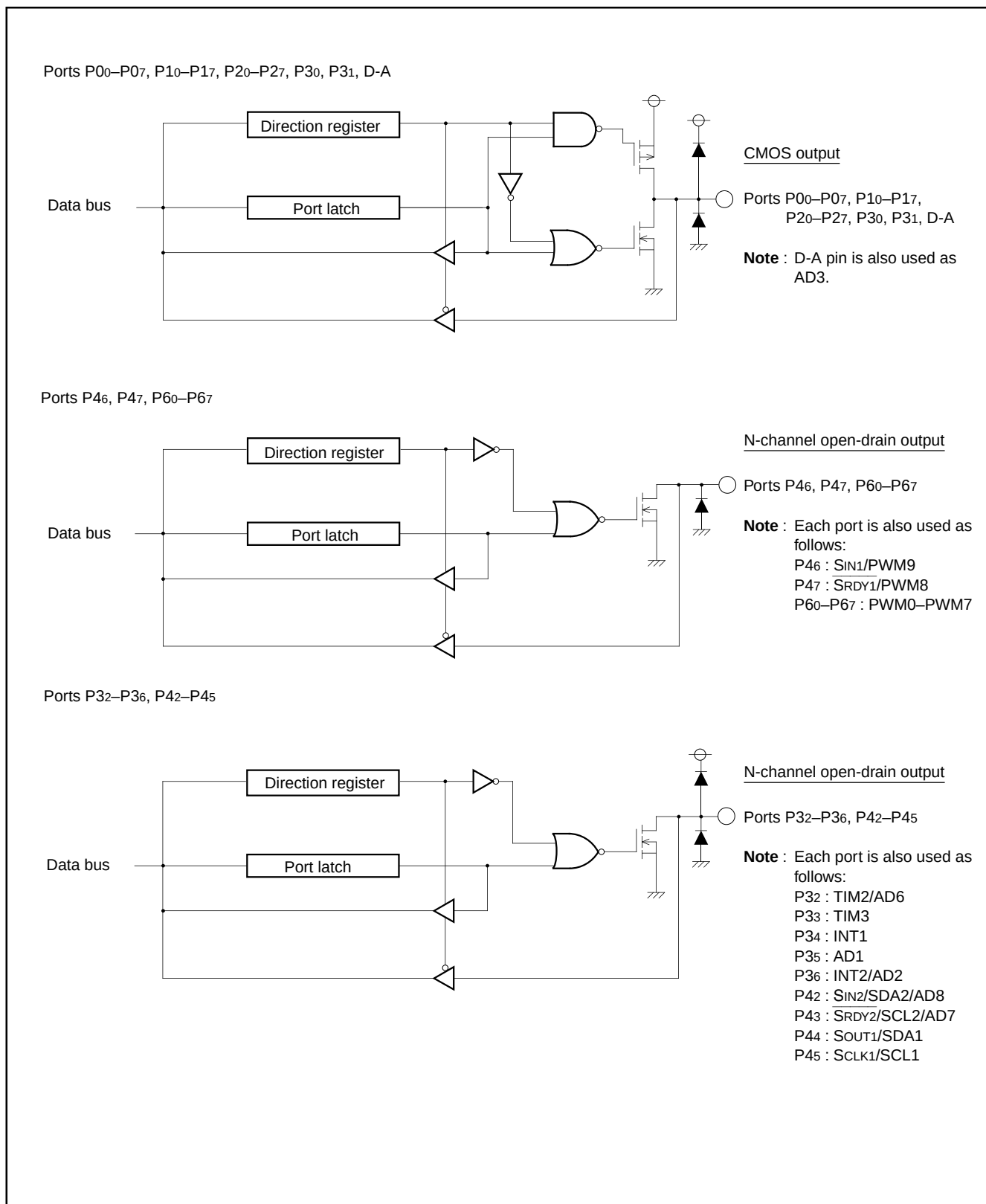


Fig. 1. I/O Pin Block Diagram (1)

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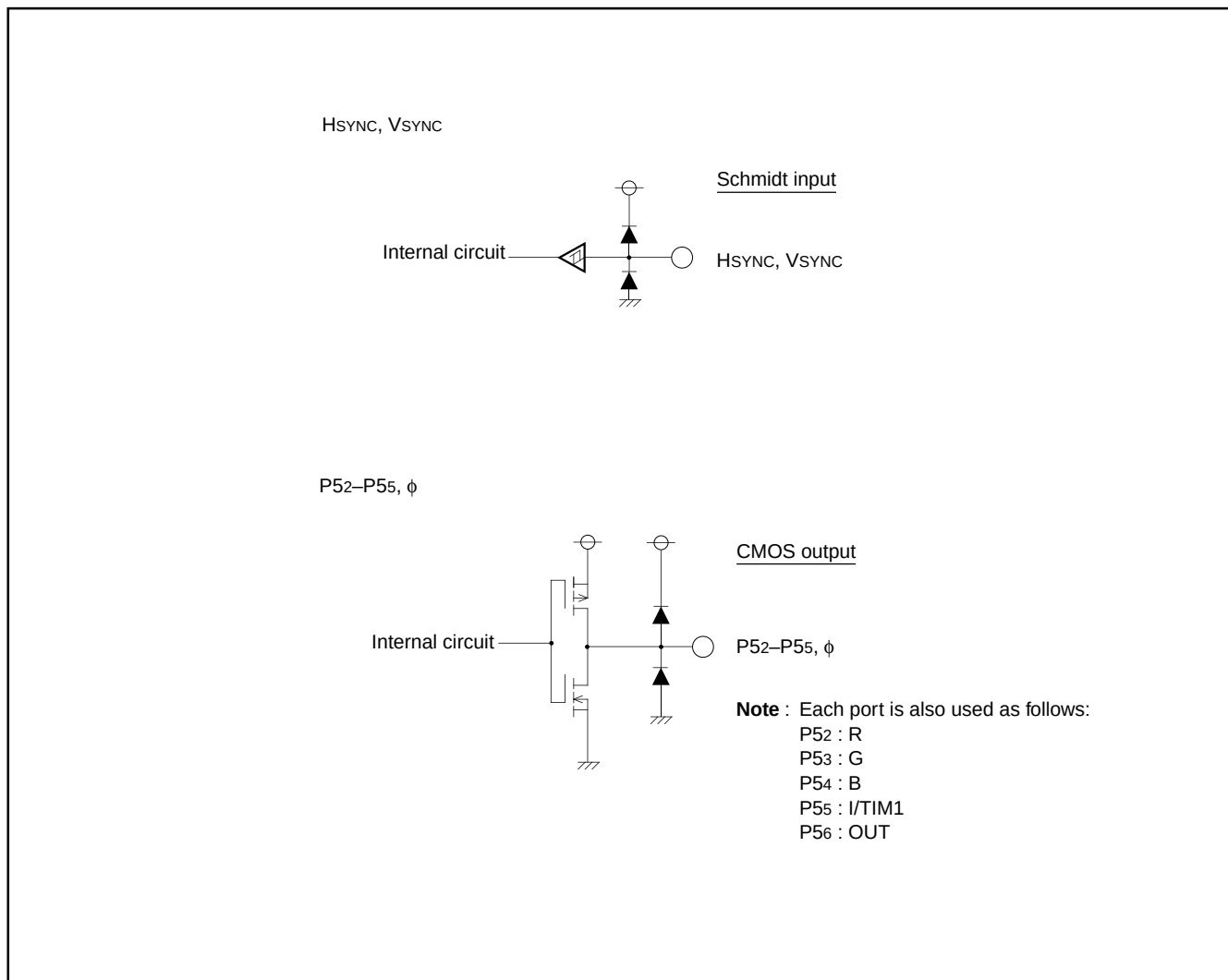


Fig. 2. I/O Pin Block Diagram (2)

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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FUNCTIONAL DESCRIPTION Central Processing Unit (CPU)

This microcomputer uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

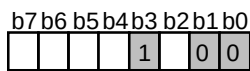
The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instructions can be used.

CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address 00FB16.

CPU Mode Register



CPU mode register (CPUM) (CM) [Address 00FB 16]

B	Name	Functions	After reset	R:W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } Not available 1 0: } 1 1: }	0	R:W
2	Stack page selection bit (CM2) (See note 1)	0: 0 page 1: 1 page	1	R:W
3	Fix these bits to "1."		1	R:W
4	Internal system clock output selection bit (CM4) (See note 2)	0: Output is stopped 1: Internal system clock ϕ output	1	R:W
5	XCOU drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R:W
6	Main Clock (XIN-XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R:W
7	Internal system clock selection bit (CM7)	0: XIN-XOUT selected (high-speed mode) 1: XCIN-XCOU selected (high-speed mode)	0	R:W

Notes 1: This bit is set to "1" after the reset release.

2: The internal system clock ϕ stops at HIGH.

Fig. 3. CPU Mode Register

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MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

ROM is used for storing user programs as well as the interrupt vector area.

RAM for Display

RAM for display is used for specifying the character codes and colors to display.

ROM for Display

ROM for display is used for storing character data.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Correction Memory (RAM)

This is used as the program area for ROM correction.

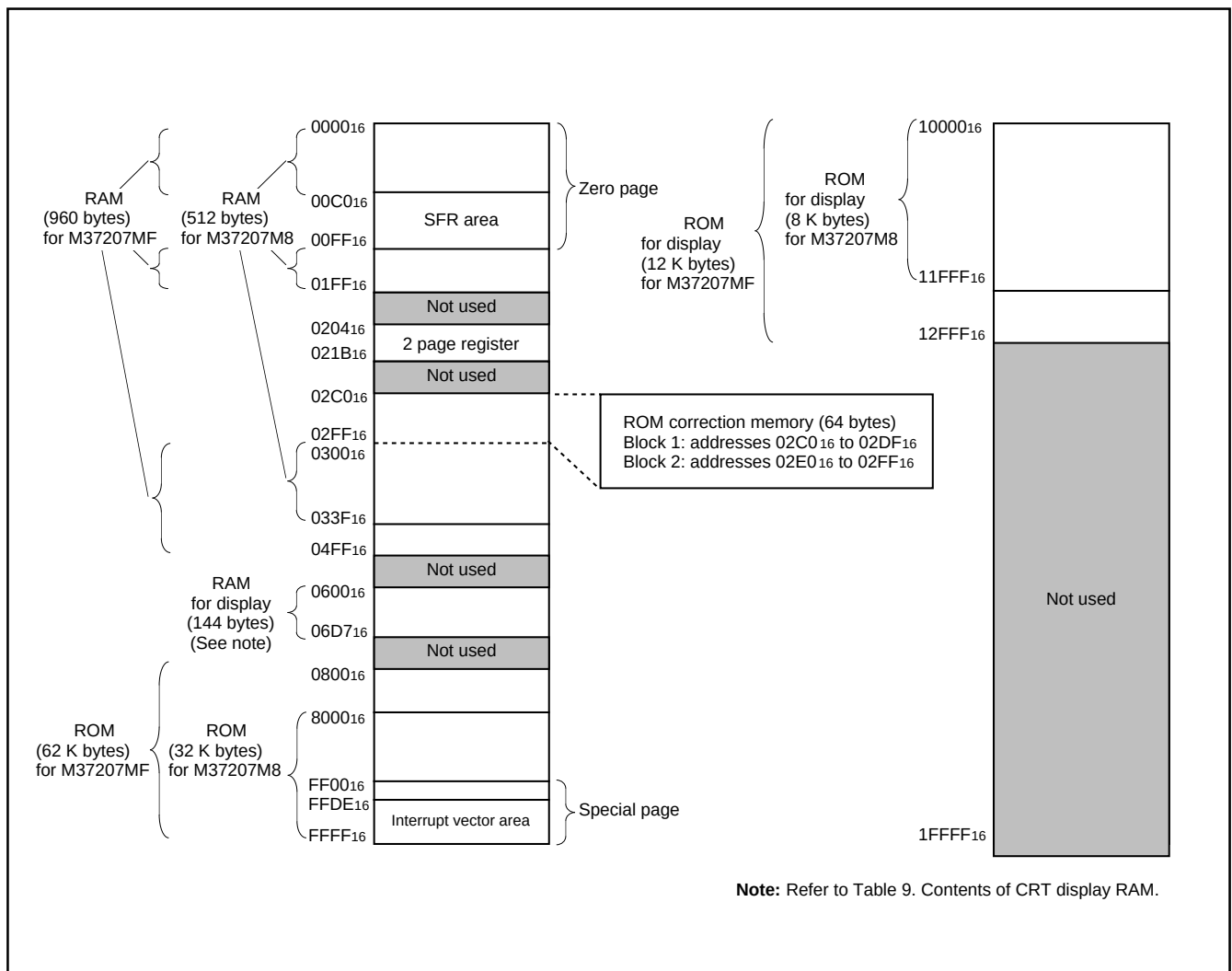


Fig. 4. Memory Map

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

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■SFR Area (addresses C0₁₆ to DF₁₆)

< Bit allocation >

☐ : } Function bit
 Name : }
☐ : No function bit
☐ 0 : Fix this bit to "0"
 (do not write "1")
☐ 1 : Fix this bit to "1"
 (do not write "0")

< State immediately after reset >

☐ 0 : "0" immediately after reset
☐ 1 : "1" immediately after reset
☐ ? : Undefined immediately
 after reset

Address	Register	Bit allocation	State immediately after reset
C0 ₁₆	Port P0 (P0)	b7 b0	b7 b0
C1 ₁₆	Port P0 direction register (D0)		?
C2 ₁₆	Port P1 (P1)		00 ₁₆
C3 ₁₆	Port P1 direction register (D1)		?
C4 ₁₆	Port P2 (P2)		00 ₁₆
C5 ₁₆	Port P2 direction register (D2)		?
C6 ₁₆	Port P3 (P3)		00 ₁₆
C7 ₁₆	Port P3 direction register (D3)		?
C8 ₁₆	Port P4 (P4)		00 ₁₆
C9 ₁₆	Port P4 direction register (D4)		?
CA ₁₆	Port P5 (P5)		?
CB ₁₆	Port P5 control register (D5)		0 ? ? ? ? ? ? ?
CC ₁₆	Port P6 (P6)		00 ₁₆
CD ₁₆	Port P6 direction register (D6)		?
CE ₁₆	DA-H register (DA-H)		00 ₁₆
CF ₁₆	DA-L register (DA-L)		?
D0 ₁₆	PWM0 register (PWM0)		0 ? ? ? ? ? ? ?
D1 ₁₆	PWM1 register (PWM1)		00 ₁₆
D2 ₁₆	PWM2 register (PWM2)		?
D3 ₁₆	PWM3 register (PWM3)		?
D4 ₁₆	PWM4 register (PWM4)		?
D5 ₁₆	PWM output control register 1 (PW)	PW7 PW6 PW5 PW4 PW3 PW2 PW1 PW0	00 ₁₆
D6 ₁₆	PWM output control register 2 (PN)	PN4 PN3 PN2 PN1 PN0	00 ₁₆
D7 ₁₆	Interrupt interval determination register (??)		?
D8 ₁₆	Interrupt interval determination control register (RE)	RE5 RE4 RE3 RE2 RE1 RE0	00 ₁₆
D9 ₁₆	I ² C data shift register (S0)	D7 D6 D5 D4 D3 D2 D1 D0	?
DA ₁₆	I ² C address register (S0D)	SAD6 SAD5 SAD4 SAD3 SAD2 SAD1 SAD0 RBW	00 ₁₆
DB ₁₆	I ² C status register (S1)	MST TRX BB PIN AL AAS AD0 LRB	0 0 0 1 0 0 0 ?
DC ₁₆	I ² C control register (S1D)	BSEL1 BSEL0 10BIT SAD	00 ₁₆
DD ₁₆	I ² C clock control register (S2)	ACK ACK BIT FAST MODE CCR4 CCR3 CCR2 CCR1 CCR0	00 ₁₆
DE ₁₆	Serial I/O mode register (SM)	SM6 SM5 0 SM3 SM2 SM1 SM0	00 ₁₆
DF ₁₆	Serial I/O register (SIO)		?

Fig. 5. Memory Map of Special Function Register (SFR)

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■ SFR Area (addresses E0₁₆ to FF₁₆)

< Bit allocation >

☐ : } Function bit
Name : }

☐ : No function bit

☒ 0 : Fix this bit to "0"
(do not write "1")

☒ 1 : Fix this bit to "1"
(do not write "0")

< State immediately after reset >

☐ 0 : "0" immediately after reset

☐ 1 : "1" immediately after reset

☐ ? : Undefined immediately
after reset

Address	Register	Bit allocation								State immediately after reset							
		b7				b0				b7				b0			
E0 ₁₆	Horizontal register (HR)	0		HR5	HR4	HR3	HR2	HR1	HR0	00 ₁₆							
E1 ₁₆	Vertical register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0	?	?	?	?	?	?	?
E2 ₁₆	Vertical register 2 (CV2)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0	?	?	?	?	?	?	?
E3 ₁₆	Vertical register 3 (CV3)		CV36	CV35	CV34	CV33	CV32	CV31	CV30	0	?	?	?	?	?	?	?
E4 ₁₆	Character size register (CS)	CS7		CS31	CS30	CS21	CS20	CS11	CS10	0	0	?	?	?	?	?	?
E5 ₁₆	Border selection register (MD)			MD31	MD30	MD21	MD20	MD11	MD10	0	0	?	?	?	?	?	?
E6 ₁₆	Color register 0 (CO0)	CO07	CO06	CO05	CO04	CO03	CO02	CO01	CO00	00 ₁₆							
E7 ₁₆	Color register 1 (CO1)	CO17	CO16	CO15	CO14	CO13	CO12	CO11	CO10	00 ₁₆							
E8 ₁₆	Color register 2 (CO2)	CO27	CO26	CO25	CO24	CO23	CO22	CO21	CO20	00 ₁₆							
E9 ₁₆	Color register 3 (CO3)	CO37	CO36	CO35	CO34	CO33	CO32	CO31	CO30	00 ₁₆							
EA ₁₆	CRT control register 1 (CC)	0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	00 ₁₆							
EB ₁₆	Display block counter (CBC)									00 ₁₆							
EC ₁₆	CRT port control register (CRTP)	B	G	R	I		R/G/B	VSYS	HSYC	00 ₁₆							
ED ₁₆	Wipe mode register (SL)		SL6	SL5	SL4	SL3	SL2	SL1	SL0	00 ₁₆							
EE ₁₆	Wipe start register (??)									00 ₁₆							
EF ₁₆	A-D control register 1 (ADM)				ADM4		ADM2	ADM1	ADM0	0	0	0	?	0	0	0	0
F0 ₁₆	Timer 1 (TM1)									FF ₁₆							
F1 ₁₆	Timer 2 (TM2)									07 ₁₆							
F2 ₁₆	Timer 3 (TM3)									FF ₁₆							
F3 ₁₆	Timer 4 (TM4)									07 ₁₆							
F4 ₁₆	Timer mode register 1 (TMR1)	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10	00 ₁₆							
F5 ₁₆	Timer mode register 2 (TMR2)	TMR27	TMR26	TMR25	TMR24	TMR23	TMR22	TMR21	TMR20	00 ₁₆							
F6 ₁₆	PWM5 register (PWM5)									?							
F7 ₁₆	PWM6 register (PWM6)									?							
F8 ₁₆	PWM7 register (PWM7)									?							
F9 ₁₆	PWM8 register (PWM8)									?							
FA ₁₆	PWM9 register (PWM9)									?							
FB ₁₆	CPU mode register (CPUM)	CM7	CM6	CM5	1	1	CM2	0	0	0	0	1	1	1	0	0	
FC ₁₆	Interrupt request register 1 (IREQ1)		IICR	VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	00 ₁₆							
FD ₁₆	Interrupt request register 2 (IREQ2)	0		TM56R	MSR		S1R	IT2R	IT1R	00 ₁₆							
FE ₁₆	Interrupt control register 1 (ICON1)		IICE	VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	00 ₁₆							
FF ₁₆	Interrupt control register 2 (ICON2)	TM56C	0	TM56E	MSE	0	SIE	IT2E	IT1E	00 ₁₆							

Fig. 6. Memory Map of Special Function Register (SFR)

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■ SFR Area (addresses 204₁₆ to 21B₁₆)

< Bit allocation >

☐ : } Function bit
Name : }

☐ : No function bit

☐ 0 : Fix this bit to "0"
(do not write "1")

☐ 1 : Fix this bit to "1"
(do not write "0")

< State immediately after reset >

☐ 0 : "0" immediately after reset

☐ 1 : "1" immediately after reset

☐ ? : Undefined immediately
after reset

Address	Register	Bit allocation								State immediately after reset							
		b7							b0	b7							b0
204 ₁₆	Timer 5 (T5)									00 ₁₆							
205 ₁₆	Timer 6 (T6)									00 ₁₆							
206 ₁₆	Port control register (P7D)				P7D4		P7D2	P7D1	P7D0	0	0	0	0	0	0	?	?
207 ₁₆	Serial I/O control register (SIC)	SIC7	SIC8	SIC5	SIC4	SIC3	SIC2	SIC1	SIC0	00 ₁₆							
208 ₁₆	CRT control register 2 (CBR)							CBR1	CBR0	00 ₁₆							
209 ₁₆	CRT clock selection register (OP)	0						OP1	OP0	00 ₁₆							
20A ₁₆	A-D control register (ADC)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	0	0	?	?	?	?	?	?
20B ₁₆	Timer mode register (TMR3)								TMR30	00 ₁₆							
20C ₁₆										?							
20D ₁₆										?							
20E ₁₆										?							
20F ₁₆										?							
210 ₁₆										?							
211 ₁₆										?							
212 ₁₆										?							
213 ₁₆										?							
214 ₁₆										?							
215 ₁₆										?							
216 ₁₆										?							
217 ₁₆	ROM correction address 1 (high-order)									00 ₁₆							
218 ₁₆	ROM correction address 1 (low-order)									00 ₁₆							
219 ₁₆	ROM correction address 2 (high-order)									00 ₁₆							
21A ₁₆	ROM correction address 2 (low-order)									00 ₁₆							
21B ₁₆	ROM correction enable register (RCR)					0	0	RC1	RC0	?	?	?	?	0	0	0	0

Fig. 7. Memory Map of 2 Page Register

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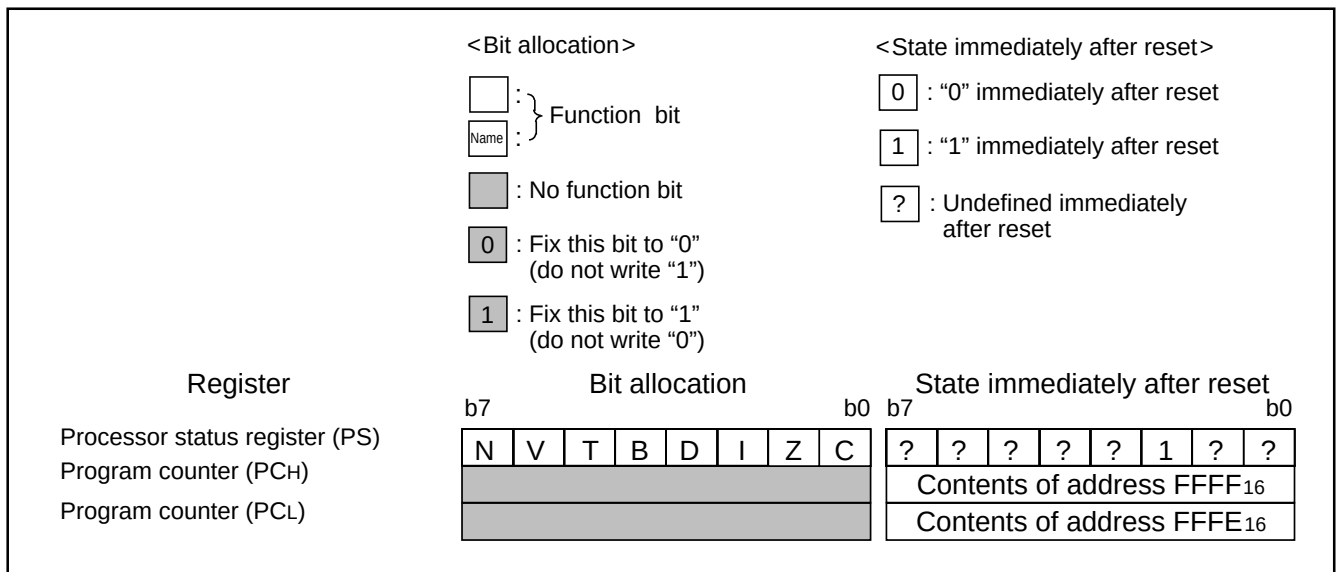


Fig. 8. Internal State of Processor Status Register and Program Counter at Reset

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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INTERRUPTS

Interrupts can be caused by 15 different sources consisting of 3 external, 10 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities as shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

- (1) The contents of the program counter and processor status register are automatically stored into the stack.
- (2) The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
- (3) The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figures 10 to 13 show the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority.

Figure 9 shows interrupt control.

Interrupt Causes

- (1) VSYNC and CRT interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.

The CRT interrupt occurs after character block display to the CRT is completed.

- (2) INT1, INT2 interrupts

With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L," and generates an interrupt request. The input active edge can be selected by bits 3 and 4 of the interrupt interval determination control register (address 00D8₁₆) : when this bit is "0," a change from "L" to "H" is detected; when it is "1," a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

- (3) Timer 1, 2, 3 and 4 interrupts

An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

- (4) Serial I/O interrupt

This is an interrupt request from the clock synchronous serial I/O function.

Table 1. Interrupt Vector Addresses and Priority

Interrupt Source	Priority	Vector Addresses	Remarks
Reset	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT1 interrupt	3	FFFB ₁₆ , FFFA ₁₆	Active edge selectable
INT2 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	Active edge selectable
Timer 4 interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
f(X _{IN})/4096 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
VSYNC interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	Active edge selectable
Timer 3 interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 2 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 1 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Serial I/O interrupt	11	FFEB ₁₆ , FFEA ₁₆	
Multi-master I ² C-BUS interface interrupt	12	FFE7 ₁₆ , FFE6 ₁₆	
Timer 5 · 6 interrupt	13	FFE3 ₁₆ , FFE2 ₁₆	Source switch by software (See note)
BRK instruction interrupt	14	FFDF ₁₆ , FFDE ₁₆	Non-maskable (software interrupt)

Note : Switching a source during a program causes an unnecessary interrupt. Therefore, set a source at initializing of program.

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- (5) $f(X_{IN})/4096$ interrupt
This interrupt occurs regularly with a $f(X_{IN})/4096$ period. Set bit 0 of the PWM output control register 1 to "0."
- (6) Multi-master I²C-BUS interface interrupt
This is an interrupt request related to the multi-master I²C-BUS interface.
- (7) Timer 5 · 6 interrupt
An interrupt is generated by an overflow of timer 5 or 6. Their priorities are same, and can be switched by software.
- (8) BRK instruction interrupt
This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

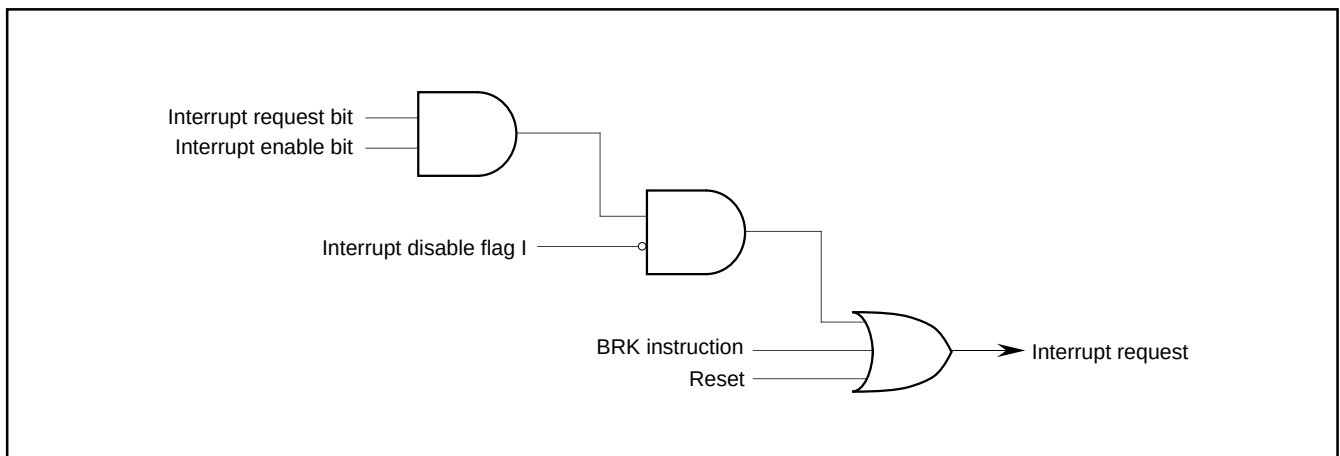


Fig. 9. Interrupt Control

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0



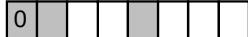
Interrupt request register 1 (IREQ1) [Address 00FC 16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	CRT interrupt request bit (CRTR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Multi-master I ² C-BUS interface interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 10. Interrupt Request Register 1

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt request register 2 (IREQ2) [Address 00FD 16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (IT1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	INT2 interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (SIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3,6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

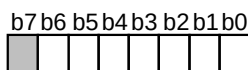
*: "0" can be set by software, but "1" cannot be set.

Fig. 11. Interrupt Request Register 2

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Interrupt Control Register 1

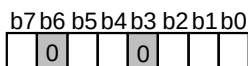


Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	CRT interrupt enable bit (CRTE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Multi-master I ² C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 12. Interrupt Control Register 1

Interrupt Control Register 2



Interrupt control register 2 (ICON2) [Address 00FF16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3, 6	Fix these bits to "0."		0	R	W
4	f(X _{IN})/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56C)	0 : Timer 5 1 : Timer 6	0	R	W

Fig. 13. Interrupt Control Register 2

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TIMERS

The M37267M6-XXXSP has 6 timers: timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 17.

0.

All of the timers count down and their divide ratio is $1/(n+1)$, where n is the value of timer latch. By writing a count value to the corresponding timer latch (addresses 00F0₁₆ to 00F3₁₆: timers 1 to 4, addresses 020C₁₆ and 020D₁₆: timers 5 and 6), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse after the count value reaches "00₁₆."

(1) Timer 1

Timer 1 can select one of the following count sources:

- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- $f(X_{IN})/4096$ or $f(X_{CIN})/4096$
- $f(X_{CIN})$
- External clock from the TIM2 pin

The count source of timer 1 is selected by setting bits 5 and 0 of timer mode register 1 (address 00F4₁₆). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

Timer 1 interrupt request occurs at timer 1 overflow.

(2) Timer 2

Timer 2 can select one of the following count sources:

- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer mode register 1 (address 00F4₁₆). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register. When timer 1 overflow signal is a count source for timer 2, timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bit 0 of timer mode register 2 (address 00F5₁₆). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- $f(X_{IN})/2$ or $f(X_{CIN})/2$
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 1 and 4 of timer mode register 2 (address 00F5₁₆). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register. When timer 3 overflow signal is a count source for timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

(5) Timer 5

Timer 5 can select one of the following count sources:

- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- $f(X_{CIN})$
- Timer 4 overflow signal

The count source of timer 3 is selected by setting bit 6 of timer mode register 1 (address 00F4₁₆) and bit 7 of timer mode register 2 (address 00F5₁₆). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

Timer 5 interrupt request occurs at timer 5 overflow.

(6) Timer 6

Timer 6 can select one of the following count sources:

- $f(X_{IN})/16$ or $f(X_{CIN})/16$
- Timer 5 overflow signal

The count source of timer 6 is selected by setting bit 7 of timer mode register 1 (address 00F4₁₆). Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register. When timer 5 overflow signal is a count source for timer 6, timer 5 functions as an 8-bit prescaler.

Timer 6 interrupt request occurs at timer 6 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF₁₆" is automatically set in timer 3; "07₁₆" in timer 4. The $f(X_{IN})^*/16$ is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF₁₆" is automatically set in timer 3; "07₁₆" in timer 4. However, the $f(X_{IN})^*/16$ is not selected as the timer 3 count source. So set bit 0 of timer mode register 2 (address 00F5₁₆) to "0" before execution of the STP instruction ($f(X_{IN})^*/16$ is selected as timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

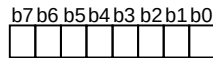
*: When bit 7 of the CPU mode register (CM7) is "1," $f(X_{IN})$ becomes $f(X_{CIN})$.

The timer-related registers is shown in Figures 14 to 16.

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Timer Mode Register 1



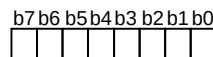
Timer mode register 1 (TMR1) [Address 00F416]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TMR10, TMR15)	b5 b0 0 0: f(XIN)/16 or f(XCIN)/16 (See note) 0 1: f(XIN)/4096 or f(XCIN)/4096 (See note) 1 0: f(XCIN) 1 1: External clock from TIM2 pin	0	R	W
1	Timer 2 count source selection bit 1 (TMR11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TMR12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TMR13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TMR14)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 1 overflow	0	R	W
6	Timer 5 count source selection bit 2 (TMR16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 internal count source selection bit (TMR17)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: Timer 5 overflow	0	R	W

Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Fig. 14. Timer Mode Register 1

Timer Mode Register 2



Timer mode register 2 (TMR2) [Address 00F516]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TMR20)	0: f(XIN)/16 or f(XCIN)/16 (See note) 1: External clock from TIM3 pin	0	R	W
1	Timer 4 count source selection bit 2 (TMR21)	0: Timer 3 overflow signal 1: f(XIN)/16 or f(XCIN)/16 (See note)	0	R	W
2	Timer 3 count stop bit (TMR22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TMR23)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit 1 (TMR24)	0: Count source selected by bit 1 of TMR2 1: f(XIN)/2 or f(XCIN)/2 (See note)	0	R	W
5	Timer 5 count stop bit (TMR25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TMR26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TMR27)	0: Count source selected by bit 0 of TMR3 1: Count source selected by bit 6 of TMR1	0	R	W

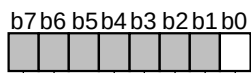
Note: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Fig. 15. Timer Mode Register 2

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Timer Mode Register 3



Timer mode register 3 (TMR3) [Address 020B16]

B	Name	Functions	After reset	R	W
0	Timer 5 count source selection bit 3 (TMR30)	0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$ (See note) 1 : $f(X_{CIN})$	0	R	W
1 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Note: Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

Fig. 16. Timer Mode Register 3

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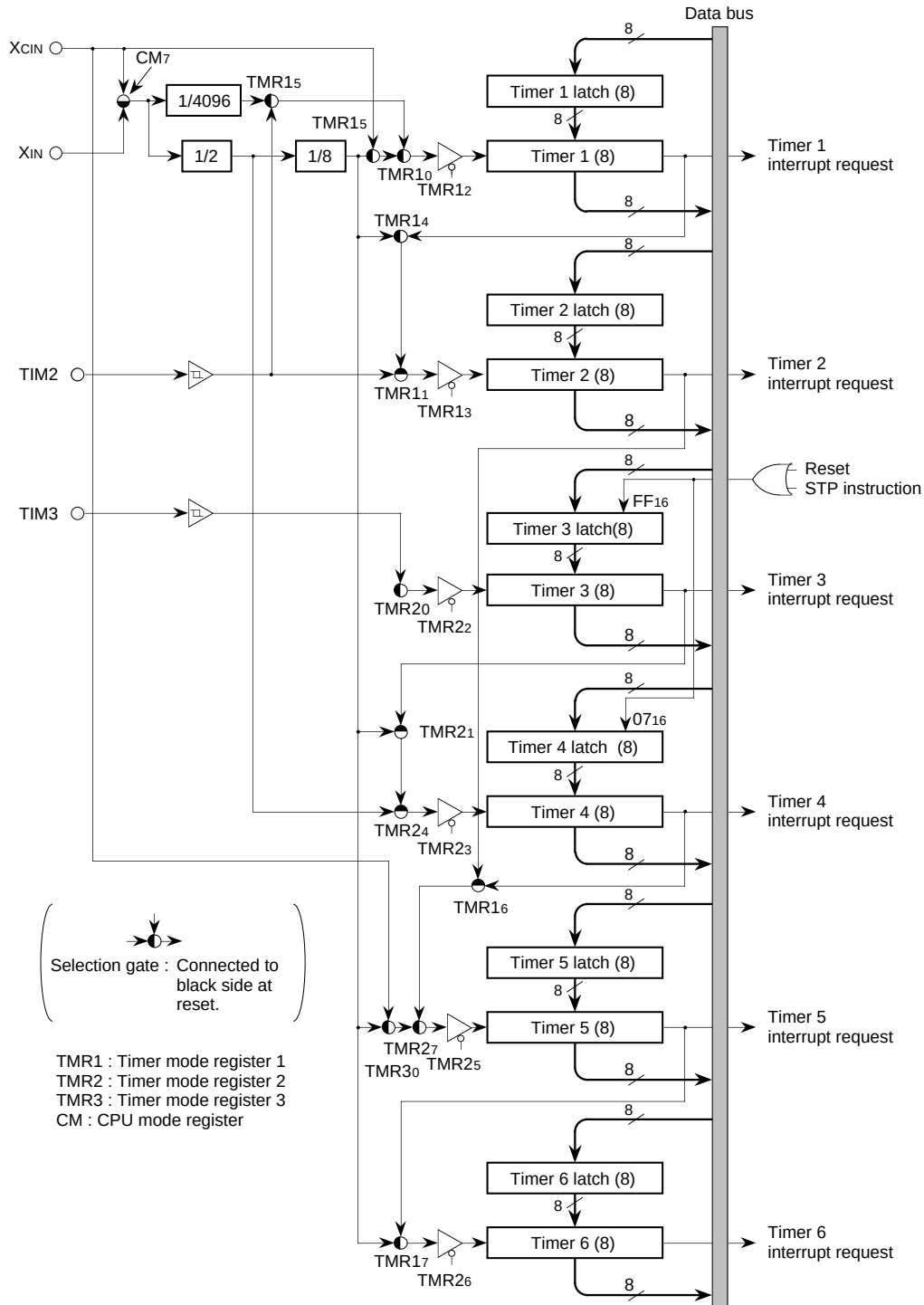


Fig. 17. Timer Block Diagram

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Internal clock : The $\overline{\text{SRDY}}$ signal goes to HIGH during the write cycle by writing data into the serial I/O register (address 00DD16). After the write cycle, the $\overline{\text{SRDY}}$ signal goes to "L" (receive enable state). The $\overline{\text{SRDY}}$ signal goes to "H" at the next falling edge of the transfer clock for the serial I/O register.

The serial I/O counter is set to "7" during write cycle into the serial I/O register (address 00DD16), and transfer clock goes HIGH forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.

After the transfer clock has counted 8 times, the serial I/O counter becomes "0" and the transfer clock stops at HIGH. At this time the interrupt request bit is set to "1."

External clock : When an external clock is selected as the clock source, the interrupt request is set to "1" after the transfer clock has counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 1 MHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 19. When using an external clock for transfer, the external clock must be held at "H" for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions such as SEB and CLB.

2: When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.

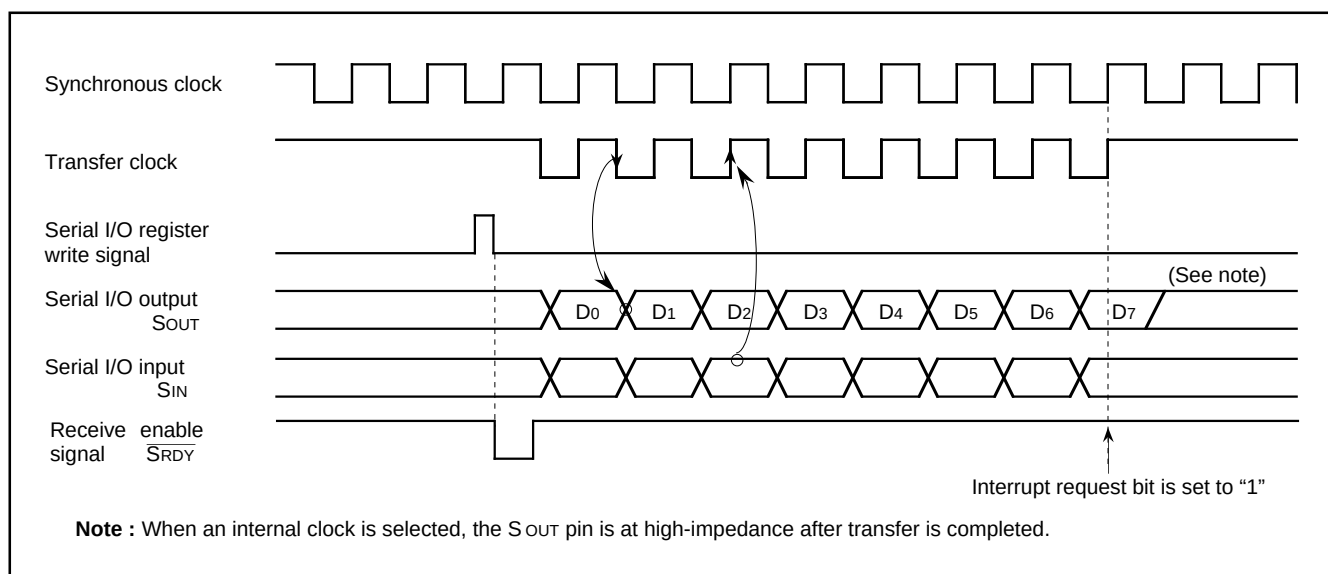
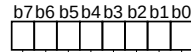


Fig. 19. Serial I/O Timing (for LSB first)

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Serial I/O Mode Register



Serial I/O mode register (SM) [Address 00DE16]

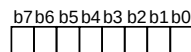
B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1) (See note 1)	b1 b0 0 0: f(XIN)/4 or f(XCIN)/4 0 1: f(XIN)/16 or f(XCIN)/16 1 0: f(XIN)/32 or f(XCIN)/32 1 1: f(XIN)/64 or f(XCIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3, 7	Ports P40, P41 function selection bits (SM3, SM7) (See note 2)	b7 b3 P40/SOUT2/ SDA3/XCIN P41/SCLK2/ SCL3/XCOUT X 0 P40 P41 0 1 SOUT2 SCLK2 1 SDA3 SCL3	0	R	W
4, 6	Ports P42, P43 function selection bits (SM4, SM6) (See note 2)	b6 b4 P42/SIN2/ SDA2/AD8 P43/SRDY2/ SCL2/AD7 0 0 P42 P43 1 SDA2 0 1 P42 SRDY2 1 SDA2 SDA2	0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W

Notes 1: Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

2: When using ports P40–P43 as serial I/O pins, set bit 1 of the serial control register to “1.”

Fig. 20. Serial I/O Mode Register

Serial I/O Control Register



Serial I/O control register (SIC) [Address 020716]

B	Name	Functions	After reset	R	W
0	Input signal to sift register selection bit (SIC0)	CSIO b0 0 0: Input signal from SIN1 0 1: Input signal from SOUT1 (See note 1) 1 0: Input signal from SIN2 1 1: Input signal from SOUT2 (See note 1)	0	R	W
1	Serial I/O pin switch bit (CSIO)	0: SOUT1, SCLK1, SIN1, SRDY1 1: SOUT2, SCLK2, SIN2, SRDY2	0	R	W
2	I ² C-BUS connection ports switch bit (SIC2)	0: SDA2, SCL2, SDA1, SCL1 1: SDA3, SCL3	0	R	W
3, 7	Ports P47 function selection bits (SM3, SM7) (See note 2)	b7 b3 P47/SRDY1/PWM8 0 X P47 1 0 SRDY1 1 PWM8	0	R	W
4, 5	Ports P44, P45 function selection bits (SM4, SM6) (See note 2)	b5 b4 P44/SOUT1/ SDA1 P45/SCLK1/ SCL1 0 X P44 P45 1 0 SOUT1 SCLK1 1 SDA1 SCL1	0	R	W
6	Ports P46 function selection bits (SIC6) (See note 2)	b6 P46/SIN1/PWM9 0 P46 1 PWM9	0	R	W

Notes 1: When inputting data from the S out pin, set “FF16” to the serial I/O register.

2: When using ports P44–P47 as serial I/O pins, set bit 1 of the serial I/O control register to “0.”

Fig. 21. Serial I/O Control Register

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Serial I/O Common Transmission/Reception Mode

By writing "1" to bit 0 of the serial I/O control register, signals S_{IN} and S_{OUT} are switched internally to be able to transmit or receive the serial data.

Figure 22 shows signals on serial I/O common transmission/reception mode.

Note : When receiving the serial data after writing "FF₁₆" to the serial I/O register.

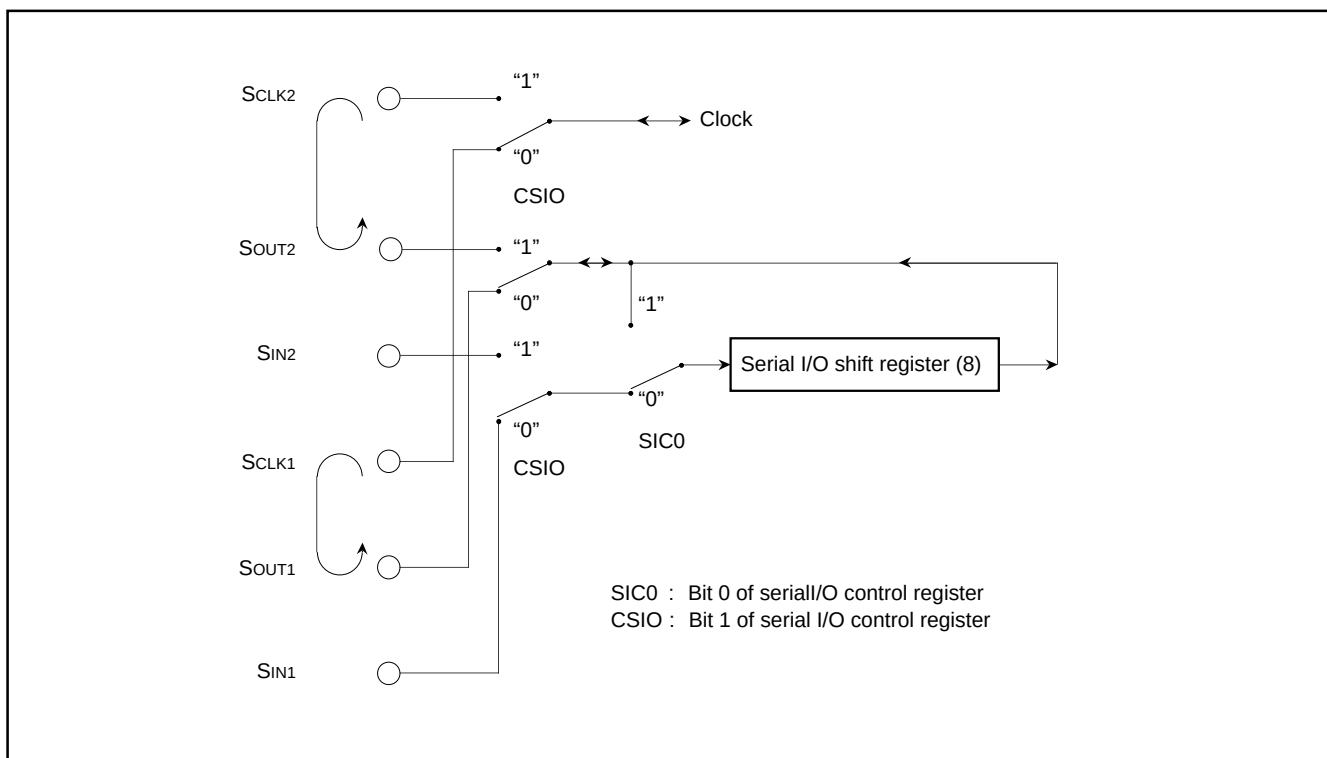


Fig. 22. Signals on Serial I/O Common Transmission/Reception Mode

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MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications. Figure 23 shows a block diagram of the multi-master I²C-BUS interface and Table 2 shows multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register and other control circuits.

Table 2. Multi-master I²C-BUS Interface Functions

Item	Function
Format	In conformity with Philips I ² C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I ² C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at $\phi = 4$ MHz)

ϕ : System clock = $f(X_{IN})/2$

Note: We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I²C control register at address 00F916) for connections between the I²C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

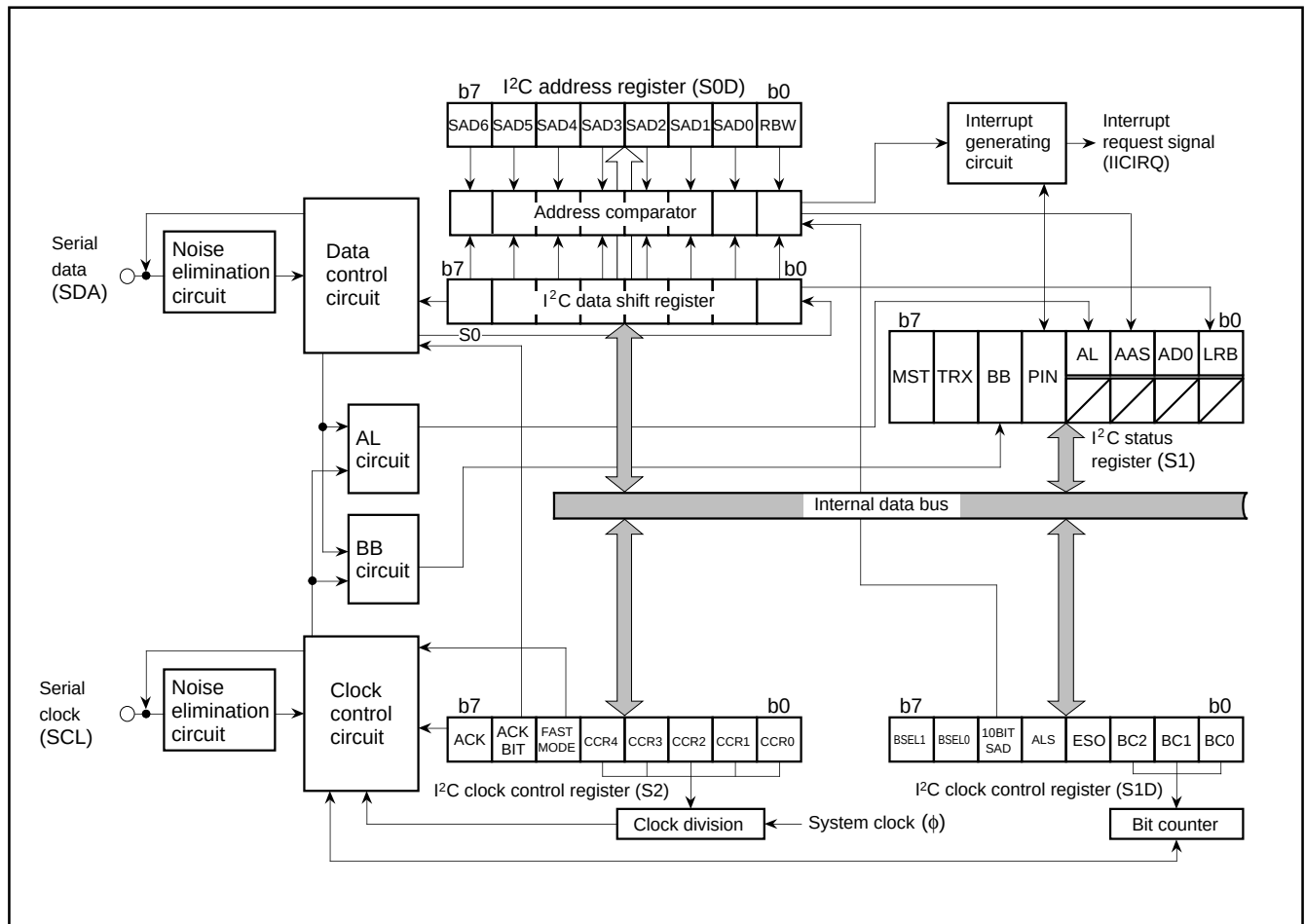


Fig. 23. Block Diagram of Multi-master I²C-BUS Interface

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(1) I²C Data Shift Register

The I²C data shift register (S0 : address 00D9₁₆) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.

The I²C data shift register is in a write enable status only when the ESO bit of the I²C control register (address 00DC₁₆) is "1." The bit counter is reset by a write instruction to the I²C data shift register. When both the ESO bit and the MST bit of the I²C status register (address 00F8₁₆) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ESO bit value.

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

(2) I²C Address Register

The I²C address register (address 00DA₁₆) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

■Bit 0: Read/Write Bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I²C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

■Bits 1 to 7: Slave Address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

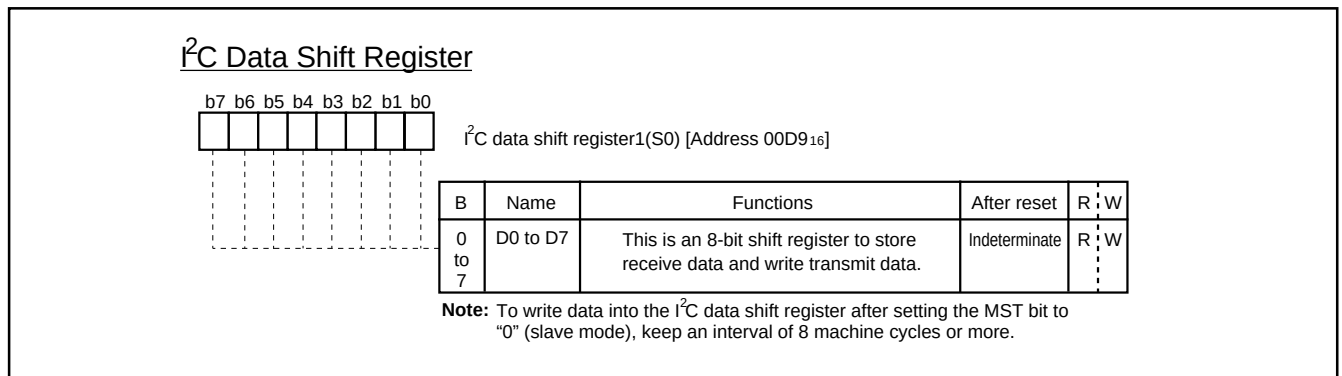


Fig. 24. I²C Data Shift Register

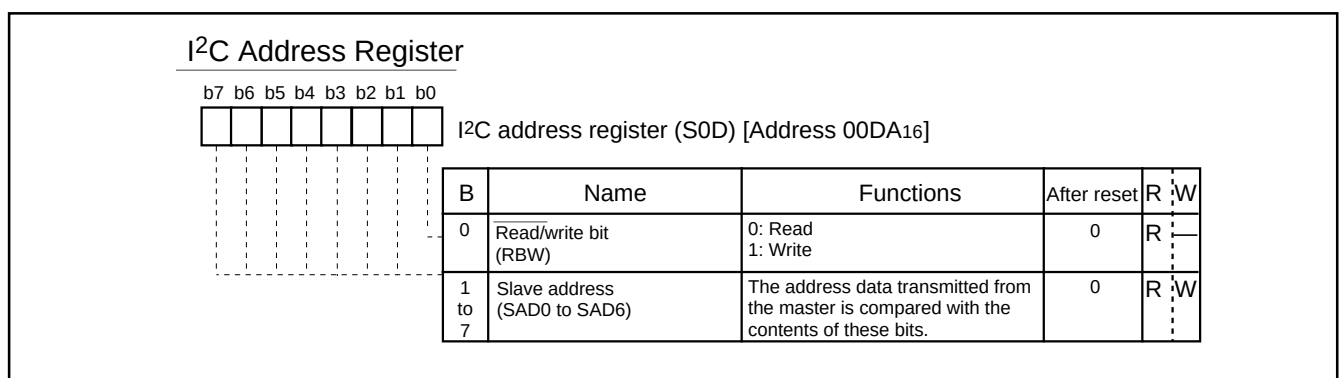


Fig. 25. I²C Address Register

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(3) I²C Clock Control Register

The I²C clock control register (address 00DD16) is used to set ACK control, SCL mode and SCL frequency.

■Bits 0 to 4: SCL Frequency Control Bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Figure 26.

■Bit 5: SCL Mode Specification Bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is set. When the bit is set to "1," the high-speed clock mode is set.

■Bit 6: ACK Bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.

However, when the slave address matches the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

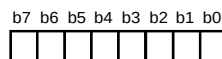
■Bit 7: ACK Clock Bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to "0," the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmission. If data is written during transmission, the I²C clock generator is reset, so that data cannot be transmitted normally.

*ACK clock: Clock for acknowledgement

I²C Clock Control Register



I²C clock control register (S2 : address 00DD16)

B	Name	Functions	After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4–CCR0 Standard clock mode High speed clock mode	0	R	W
		00 to 02 Setup disabled Setup disabled			
		03 Setup disabled 333			
		04 Setup disabled 250			
		05 100 400 (See note)			
		06 83.3 166			
		⋮ 500/CCR value 1000/CCR value			
		1D 17.2 34.5			
		1E 16.6 33.3			
		1F 16.1 32.3			
		(at $\phi = 4$ MHz, unit : kHz)			
5	SCL mode specification bit (FAST MODE)	0 : Standard clock mode 1 : High-speed clock mode	0	R	W
6	ACK bit (ACK BIT)	0 : ACK is returned. 1 : ACK is not returned.	0	R	W
7	ACK clock bit (ACK)	0 : No ACK clock 1 : ACK clock	0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
"0" period : "1" period = 3 : 2
In the other cases, the duty is as below .
"0" period : "1" period = 1 : 1

Fig. 26. I²C Clock Control Register

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(4) I²C Control Register

The I²C control register (address 00DC16) controls the data communication format.

■Bits 0 to 2: Bit Counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.

When a START condition is received, these bits become "0002" and the address data is always transmitted and received in 8 bits.

■Bit 3: I²C Interface Use Enable Bit (ESO)

This bit enables usage of the multimaster I²C BUS interface. When this bit is set to "0," the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.

When ESO = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (they are bits of the I²C status register at address 00F816).
- Writing data to the I²C data shift register (address 00F616) is disabled.

■Bit 4: Data Format Selection Bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "(5) I²C Status Register," bit 1) is received, transmission processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

■Bit 5: Addressing Format Selection Bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 00F716) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, all the bits of the I²C address register are compared with address data.

■Bits 6 and 7: Connection Control Bits between I²C-BUS Interface and Ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 28).

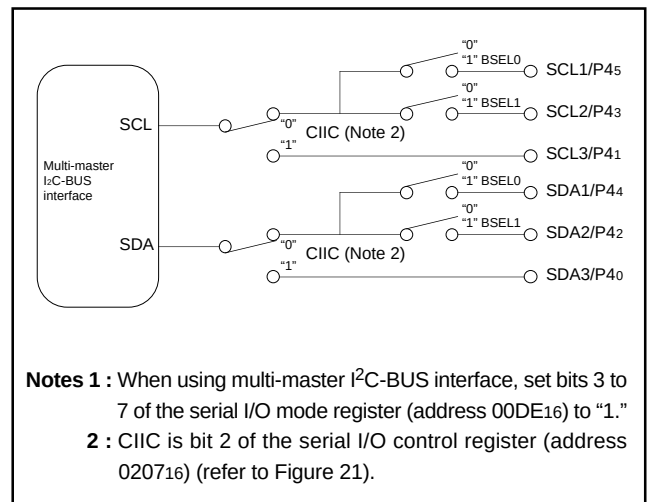
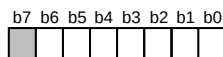


Fig. 27. Connection Port Control by BSEL0 and BSEL1

I²C Control Register



I²C control register (S1D : address 00DC16)

B	Name	Functions	After reset	R : W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0 : 8 0 0 1 : 7 0 1 0 : 6 0 1 1 : 5 1 0 0 : 4 1 0 1 : 3 1 1 0 : 2 1 1 1 : 1	0	R : W
3	I ² C-BUS interface use enable bit (ESO)	0 : Disabled 1 : Enabled	0	R : W
4	Data format selection bit (ALS)	0 : Addressing mode 1 : Free data format	0	R : W
5	Addressing format selection bit (10BIT SAD)	0 : 7-bit addressing format 1 : 10-bit addressing format	0	R : W
6, 7	Connection control bits between I ² C-BUS interface and ports	b7 b6 Connection port (See note) 0 0 : None 0 1 : SCL1, SDA1 1 0 : SCL2, SDA2 1 1 : SCL1, SDA1 SCL2, SDA2	0	R : W

Note: When using ports P11-P14 as I²C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

Fig. 28. I²C Control Register

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(5) I²C Status Register

The I²C status register (address 00DB16) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

■Bit 0: Last Receive Bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D916).

■Bit 1: General Call Detecting Flag (AD0)

This bit is set to "1" when a general call*whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

* General call: The master transmits the general call address "0016" to all slaves.

■Bit 2: Slave Address Comparison Flag (AAS)

This flag indicates a comparison result of address data.

- ① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.
 - The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I²C address register (address 00DA16).
 - A general call is received.
- ② In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.
 - When the address data is compared with the I²C address register (8 bits consists of slave address and RBW), the first bytes match.
- ③ The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D916).

■Bit 3: Arbitration Lost* Detecting Flag (AL)

In the master transmission mode, when a device other than the microcomputer sets the SDA to "L," arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

* Arbitration lost: The status in which communication as a master is disabled.

■Bit 4: I²C-BUS Interface Interrupt Request Bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 30 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in any one of the following conditions.

- Executing a write instruction to the I²C data shift register (address 00F616).
- When the ESO bit is "0"
- At reset

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

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■Bit 5: Bus Busy Flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (Note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ESO bit of the I²C control register (address 00DC16) is "0" and at reset, the BB flag is kept in the "0" state.

■Bit 6: Communication Mode Specification Bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I²C control register (address 00DC16) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/W bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/W bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication prevention function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

■Bit 7: Communication Mode Specification Bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

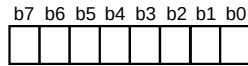
Note: The START condition duplication prevention function disables the START condition generation, reset of bit counter reset, and SCL output, when the following condition is satisfied:

- a START condition is set by another master device.

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I²C Status Register



I²C status register (S1) [Address 00DB16]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0 " 1 : Last bit = "1 "	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected	0	R	—
4	I ² C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	0	R	—
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave receive mode 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannot be written.

Fig. 29. I²C Status Register

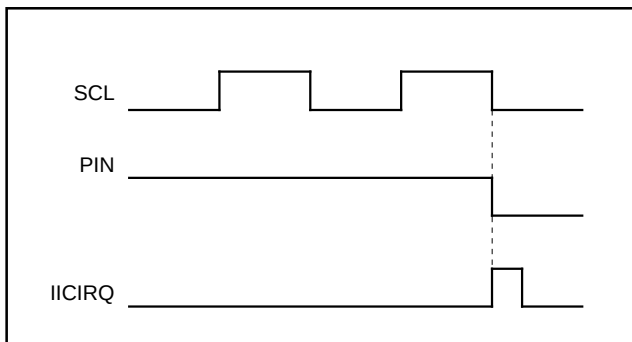


Fig. 30. Interrupt Request Signal Generation Timing

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(6) START Condition Generation Method

When the ESO bit of the I²C control register (address 00DC16) is "1," execute a write instruction to the I²C status register (address 00DB16) to set the MST, TRX and BB bits to "1." A START condition will then be generated. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 31 for the START condition generation timing diagram, and Table 3 for the START condition/STOP condition generation timing table.

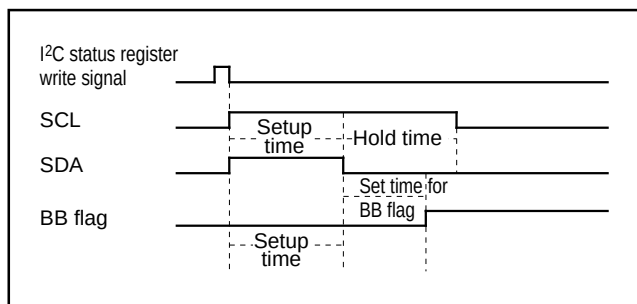


Fig. 31. START Condition Generation Timing Diagram

(7) RESTART Condition Generation Method

To generate the RESTART condition, take the following sequence:

- ① Set "2016" to the I²C status register (S1).
- ② Write a transmit data to the I²C data shift register.
- ③ Set "F016" to the I²C status register (S1) again.

<Example of Setting of RESTART Condition>

I²C status register ; S1 = 2016
I²C data shift register ; S0 = transmit data after restart
I²C status register ; S1 = F016

(8) STOP Condition Generation Method

When the ESO bit of the I²C control register (address 00DC16) is "1," execute a write instruction to the I²C status register (address 00DB16) for setting the MST bit and the TRX bit to "1" and the BB bit to "0". A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 32 for the STOP condition generation timing diagram, and Table 3 for the START condition/STOP condition generation timing table.

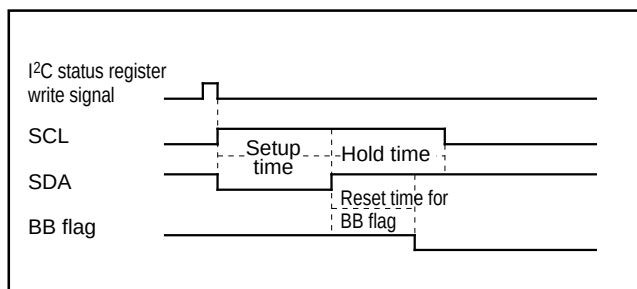


Fig. 32. STOP Condition Generation Timing Diagram

Table 3. START Condition/STOP Condition Generation Timing
Table

Item	Standard Clock Mode	High-speed Clock Mode
Setup time	5.0 μ s (20 cycles)	2.5 μ s (10 cycles)
Hold time	5.0 μ s (20 cycles)	2.5 μ s (10 cycles)
Set/reset time for BB flag	3.0 μ s (12 cycles)	1.5 μ s (6 cycles)

Note: Absolute time at $\phi = 4$ MHz. The value in parentheses denotes the number of ϕ cycles.

(9) START/STOP Condition Detect Conditions

The START/STOP condition detect conditions are shown in Figure 33 and Table 4. Only when the 3 conditions of Table 4 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" is generated to the CPU.

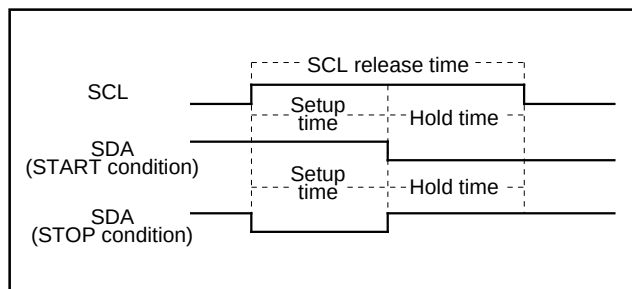


Fig. 33. START Condition/STOP Condition Detect Timing Diagram

Table 4. START Condition/STOP Condition Detect Conditions

Standard Clock Mode	High-speed Clock Mode
6.5 μ s (26 cycles) < SCL release time	1.0 μ s (4 cycles) < SCL release time
3.25 μ s (13 cycles) < Setup time	0.5 μ s (2 cycles) < Setup time
3.25 μ s (13 cycles) < Hold time	0.5 μ s (2 cycles) < Hold time

Note: Absolute time at $\phi = 4$ MHz. The value in parentheses denotes the number of ϕ cycles.

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(10) Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

① 7-bit addressing format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00DC16) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 00DA16). At the time of this comparison, address comparison of the RBW bit of the I²C address register (address 00DA16) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 34, (1) and (2).

② 10-bit addressing format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00DC16) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I²C address register (address 00DA16). At the time of this comparison, an address comparison between the RBW bit of the I²C address register (address 00DA16) and the R/W bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/W bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

When the first-byte address data matches the slave address, the AAS bit of the I²C status register (address 00DB16) is set to "1." After the second-byte address data is stored into the I²C data shift register (address 00D916), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd bytes matches the slave address, set the RBW bit of the I²C address register (address 00DA16) to "1" by software. This processing can match the 7-bit slave address and R/W data, which are received after a RESTART condition is detected, with the value of the I²C address register (address 00DA16). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 34, (3) and (4).

(11) Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C address register (address 00DA16) and "0" in the RBW bit.
- ② Set the ACK return mode and SCL = 100 kHz by setting "8516" in the I²C clock control register (address 00DD16).
- ③ Set "1016" in the I²C status register (address 00DB16) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting "4816" in the I²C control register (address 00DC16).
- ⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I²C data shift register (address 00D916) and set "0" in the least significant bit.
- ⑥ Set "F016" in the I²C status register (address 00DB16) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.

- ⑦ Set transmit data in the I²C data shift register (address 00D916). At this time, an SCL and an ACK clock automatically occurs.
- ⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
- ⑨ Set "D016" in the I²C status register (address 00DB16). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

(12) Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode, using the addressing format, is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C address register (address 00DA16) and "0" in the RBW bit.
- ② Set the no ACK clock mode and SCL = 400 kHz by setting "2516" in the I²C clock control register (address 00DD16).
- ③ Set "1016" in the I²C status register (address 00DB16) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting "4816" in the I²C control register (address 00DC16).
- ⑤ When a START condition is received, an address comparison is made.
- ⑥ •When all transmitted addresses are "0" (general call) :
AD0 of the I²C status register (address 00DB16) is set to "1" and an interrupt request signal occurs.
•When the transmitted addresses match the address set in ① :
AAS of the I²C status register (address 00DB16) is set to "1" and an interrupt request signal occurs.
•In the cases other than the above :
AD0 and AAS of the I²C status register (address 00DB16) are set to "0" and no interrupt request signal occurs.
- ⑦ Set dummy data in the I²C data shift register (address 00D916).
- ⑧ When receiving control data of more than 1 byte, repeat step ⑦.
- ⑨ When a STOP condition is detected, the communication ends.

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S	Slave address	R/W	A	Data	A	Data	A/A	P
---	---------------	-----	---	------	---	------	-----	---

7 bits "0" 1 to 8 bits 1 to 8 bits

(1) A master-transmitter transmits data to a slave-receiver

S	Slave address	R/W	A	Data	A	Data	A	P
---	---------------	-----	---	------	---	------	---	---

7 bits "1" 1 to 8 bits 1 to 8 bits

(2) A master-receiver receives data from a slave-transmitter

S	Slave address 1st 7 bits	R/W	A	Slave address 2nd byte	A	Data	A	Data	A/A	P
---	-----------------------------	-----	---	---------------------------	---	------	---	------	-----	---

7 bits "0" 8 bits 1 to 8 bits 1 to 8 bits

(3) A master-transmitter transmits data to a slave-receiver with a 10-bit address

S	Slave address 1st 7 bits	R/W	A	Slave address 2nd byte	A	Sr	Slave address 1st 7 bits	R/W	Data	A	Data	A	P
---	-----------------------------	-----	---	---------------------------	---	----	-----------------------------	-----	------	---	------	---	---

7 bits "0" 8 bits 7 bits "1" 1 to 8 bits 1 to 8 bits

(4) A master-receiver receives data from a slave-transmitter with a 10-bit address

S : START condition P : STOP condition  From master to slave
A : ACK bit R/W : Read/Write bit  From slave to master
Sr : Restart condition

Fig. 34. Address Data Communication Format

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PWM OUTPUT FUNCTION

This microcomputer is equipped with a 14-bit PWM (DA) and ten 8-bit PWMs (PWM0–PWM9). DA has a 14-bit resolution with the minimum resolution bit width of 250 ns and a repeat period of 4096 μ s (for $f(X_{IN}) = 8$ MHz). PWM0–PWM9 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 μ s and repeat period of 1024 μ s (for $f(X_{IN}) = 8$ MHz).

Figure 35 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM9 using $f(X_{IN})$ divided by 2 as a reference signal.

(1) Data Setting

When outputting DA, first set the high-order 8 bits to the DA-H register (address 00CE16), then the low-order 6 bits to the DA-L register (address 00CF16). When outputting PWM0–PWM9, set 8-bit output data to the PWMi register (i means 0 to 9; addresses 00D016 to 00D416, 00F616 to 00FA16).

(2) Transferring Data from Registers to Latches

The data written to the 8-bit PWM register is transferred to the PWM latch in each 8-bit PWM cycle period. For 14-bit PWM, the data is transferred in the next high-order 8-bit period after the write. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. When bit 7 is "0," the transfer has been completed. When bit 7 is "1," the transfer has not yet begun.

(3) Operating of 8-bit PWM

The following explains PWM operation.

First, set the bit 0 of PWM output control register 1 (address 00D516) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied.

PWM0–PWM7 are also used as pins P60–P67, PWM8, PWM9 are also used as ports pins P47, P46, respectively. For PWM0–PWM9, set the corresponding bits of the ports P4 or P6 direction register to "1" (output mode). And select each output polarity by bit 3 of PWM output control register 2 (address 00D616). Then, for PWM0–PWM5, set bits 2 to 7 of PWM output control register 1 to "1" (PWM output). For PWM6 and PWM7, set bits 0 and 1 of the PWM output control register 2 to "1." For PWM8 and PWM9, set bits 3, 6 and 7 of the serial I/O control register to "1."

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 36 shows the 8-bit PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses, relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 36 (a). The 8-bit PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in

Figure 36 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH output cannot be output, i.e. 256/256.

(4) Operating of 14-bit PWM

As with 8-bit PWM, set the bit 0 of PWM output control register 1 (address 00D516) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied. Next, select the output polarity by bit 2 of PWM output control register 2 (address 00D616). Then, the 14-bit PWM outputs from the D-A output pin by setting bit 1 of PWM output control register 1 to "0" (at reset, this bit already set to "0" automatically) to select the DA output.

The output example of the 14-bit PWM is shown in Figure 37.

The 14-bit PWM divides the data of the DA latch into the low-order 6 bits and the high-order 8 bits.

The fundamental waveform is determined with the high-order 8-bit data "DH." A HIGH area with a length $\tau \times D_H$ (HIGH area of fundamental waveform) is output every short area of " t " = 256τ = 64 μ s (τ is the minimum resolution bit width of 250 ns). The "H" level area increase interval (t_m) is determined with the low-order 6-bit data "DL." The HIGH are of smaller intervals " t_m " shown in Table 5 is longer by τ than that of other smaller intervals in PWM repeat period " T " = 64t. Thus, a rectangular waveform with the different HIGH width is output from the D-A pin. Accordingly, the PWM output changes by τ unit pulse width by changing the contents of the DA-H and DA-L registers. A length of entirely HIGH cannot be output, i. e. 256/256.

(5) Output after Reset

At reset, the output of ports P60–P67, P46 and P47 are in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

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Table 5. Relation Between the Low-order 6-bit Data and High-level Area Increase Interval

Low-order 6 bits of Data	Area Longer by τ than That of Other t_m ($m = 0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m = 32$
0 0 0 0 1 0	$m = 16, 48$
0 0 0 1 0 0	$m = 8, 24, 40, 56$
0 0 1 0 0 0	$m = 4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m = 1, 3, 5, 7, \dots, 57, 59, 61, 63$

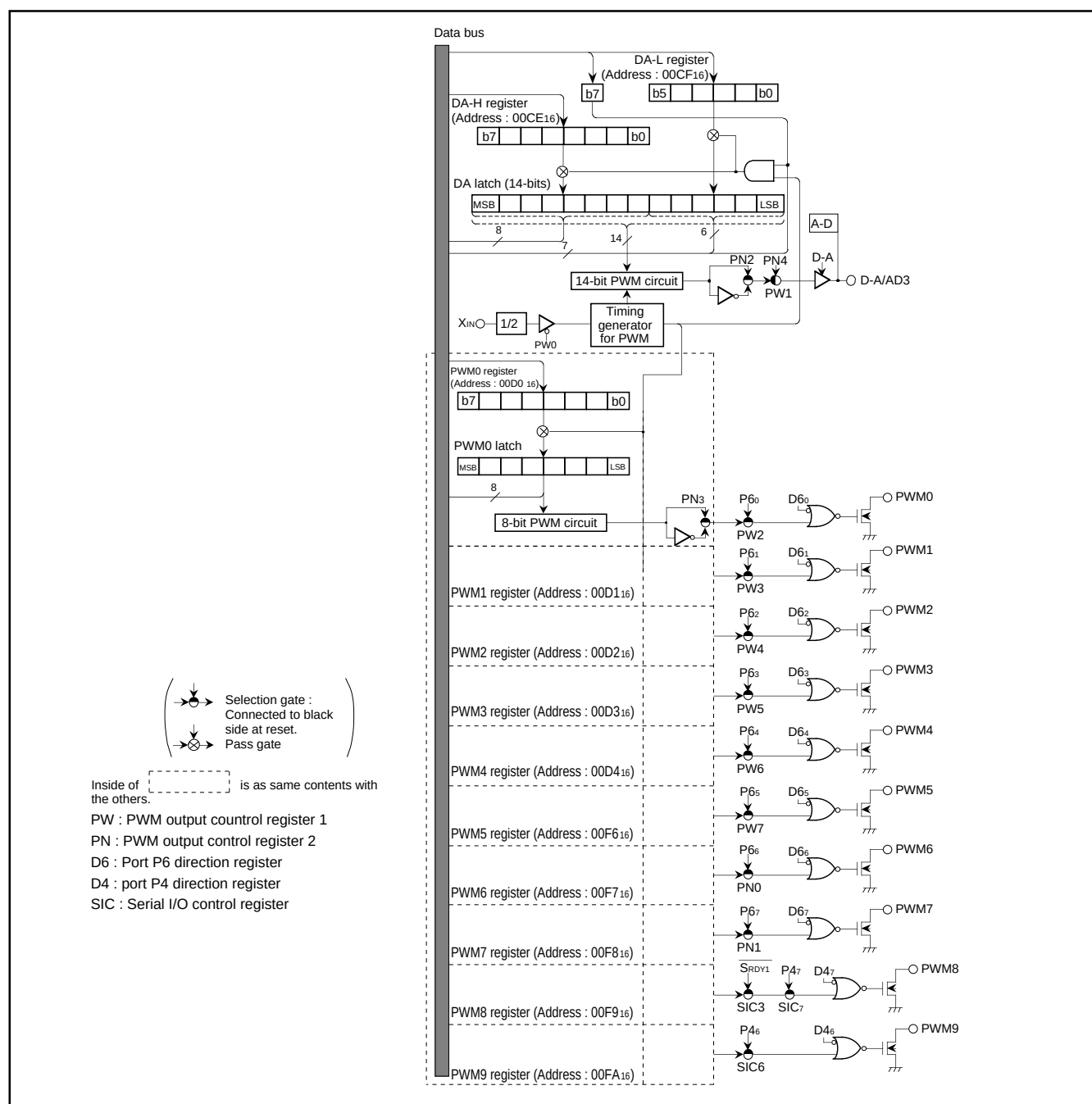


Fig. 35. PWM Block Diagram

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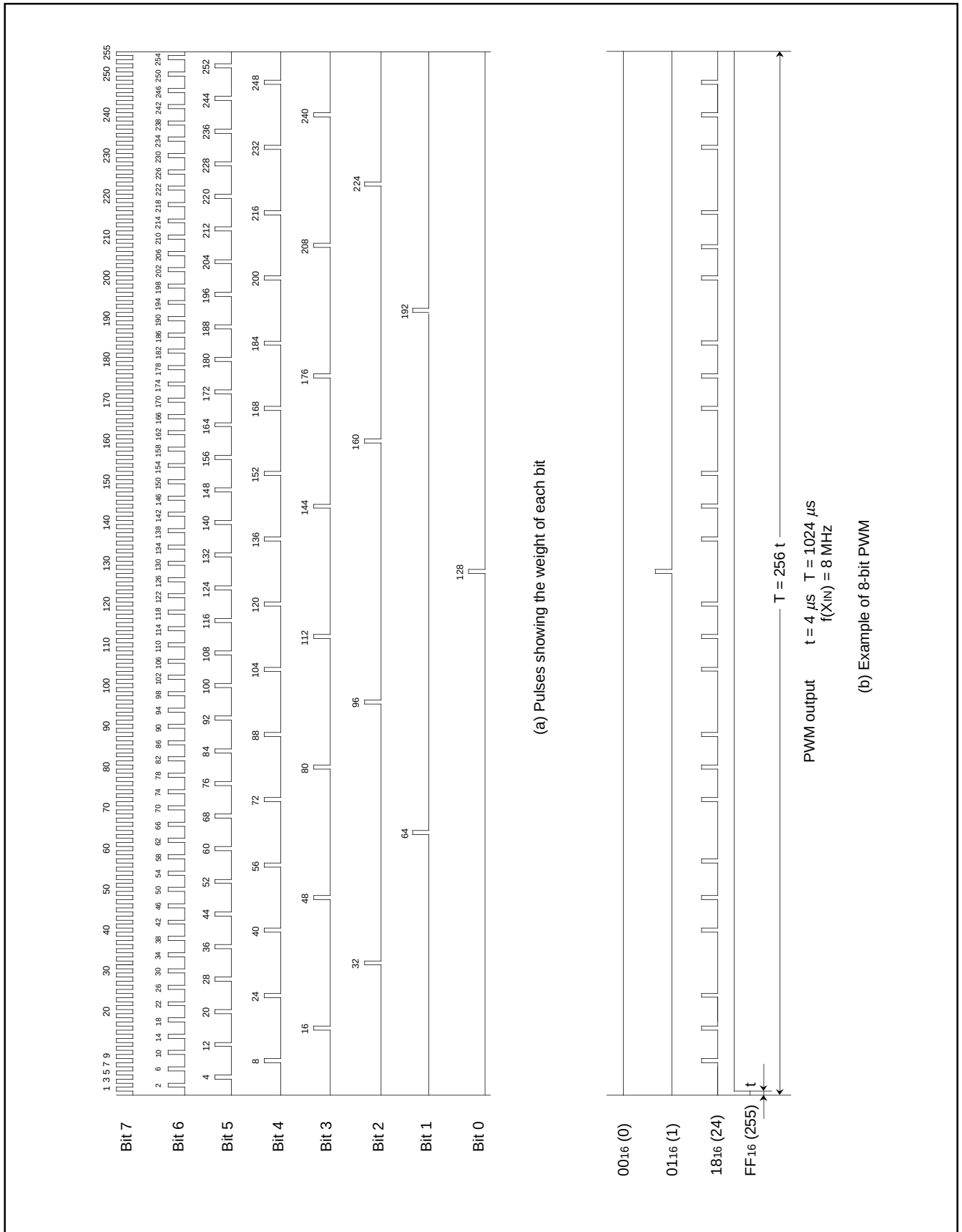


Fig. 36. 8-bit PWM Timing

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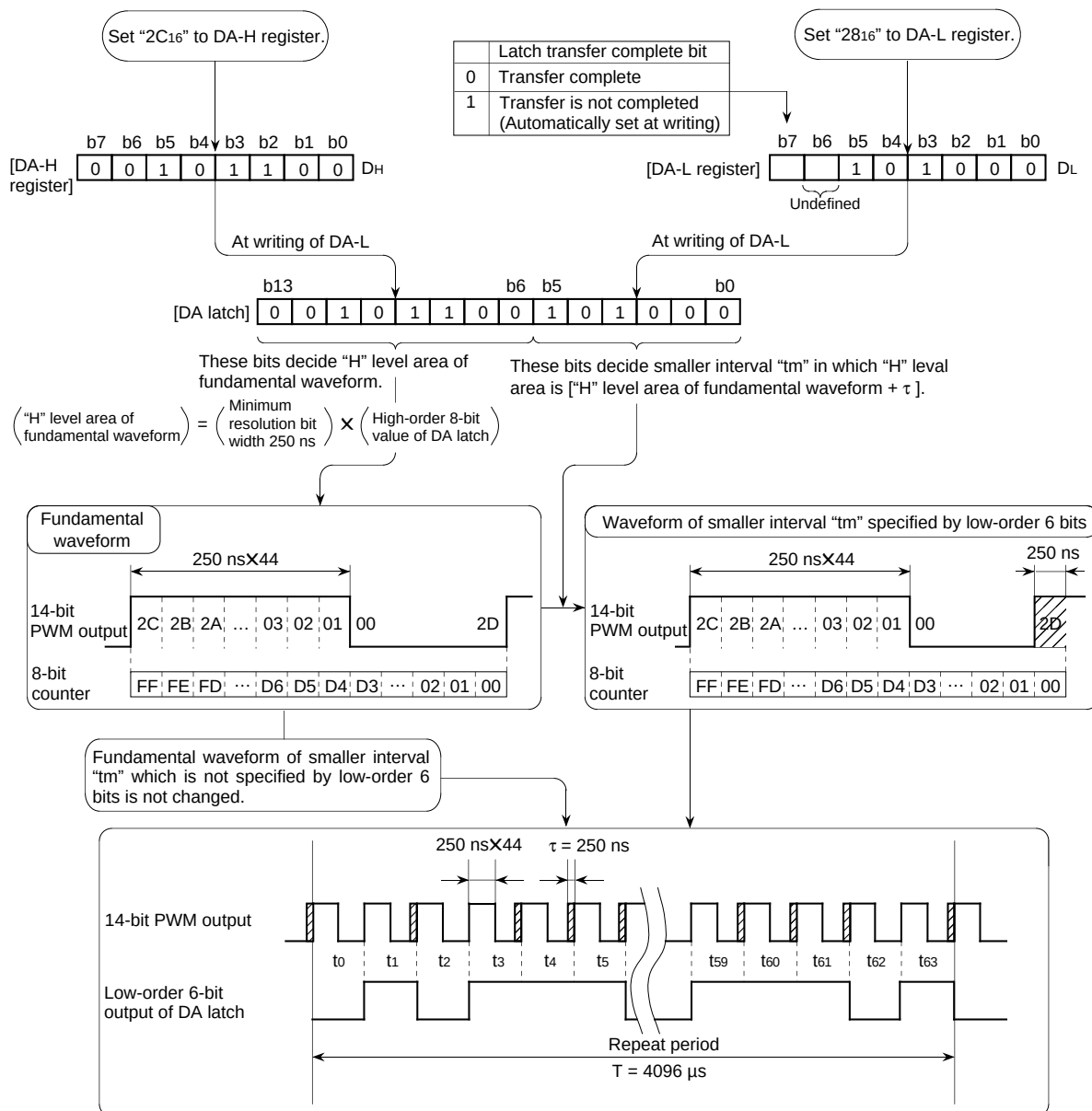


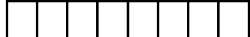
Fig. 37. 14-bit PWM (DA) Output Example (at $f(X_{IN}) = 8 \text{ MHz}$)

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PWM Output Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



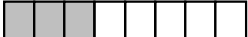
PWM output control register 1 (PW) [Address 00D516]

B	Name	Functions	After reset	R	W
0	DA, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA/PN4 output selection bit (PW1)	0 : DA output 1 : PN4 output	0	R	W
2	P60/PWM0 output selection bit (PW2)	0: P60 output 1: PWM0 output	0	R	W
3	P61/PWM1 output selection bit (PW3)	0: P61 output 1: PWM1 output	0	R	W
4	P62/PWM2 output selection bit (PW4)	0: P62 output 1: PWM2 output	0	R	W
5	P63/PWM3 output selection bit (PW5)	0: P63 output 1: PWM3 output	0	R	W
6	P64/PWM4 output selection bit (PW6)	0: P64 output 1: PWM4 output	0	R	W
7	P65/PWM5 output selection bit (PW7)	0: P65 output 1: PWM5 output	0	R	W

Fig. 38. PWM Output Control Register 1

PWM Output Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0



PWM output control register 2 (PN) [Address 00D616]

B	Name	Functions	After reset	R	W
0	P66/PWM6 output selection bit (PN0)	0 : P66 output 1 : PWM6 output	0	R	W
1	P67/PWM7 output selection bit (PN1)	0 : P67 output 1 : PWM7 output	0	R	W
2	DA output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN4)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA general-purpose output bit (PN5)	0 : Output LOW 1 : Output HIGH	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 39. PWM Output Control Register 2

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A-D COMPARATOR

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 40.

The reference voltage "V_{ref}" for D-A conversion is set by bits 0 to 5 of the A-D control register 2 (address 020A₁₆).

The comparison result of the analog input voltage and the reference voltage "V_{ref}" is stored in bit 4 of the A-D control register 1 (address 00EF₁₆).

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data for select of analog input pins to bits 0 to 2 of the A-D control register 1 and write the digital value corresponding to V_{ref} to be compared to the bits 0 to 5 A-D control register 2. The voltage comparison starts by writing to the A-D control register 2, and it is completed after 16 machine cycles (NOP instruction X 8).

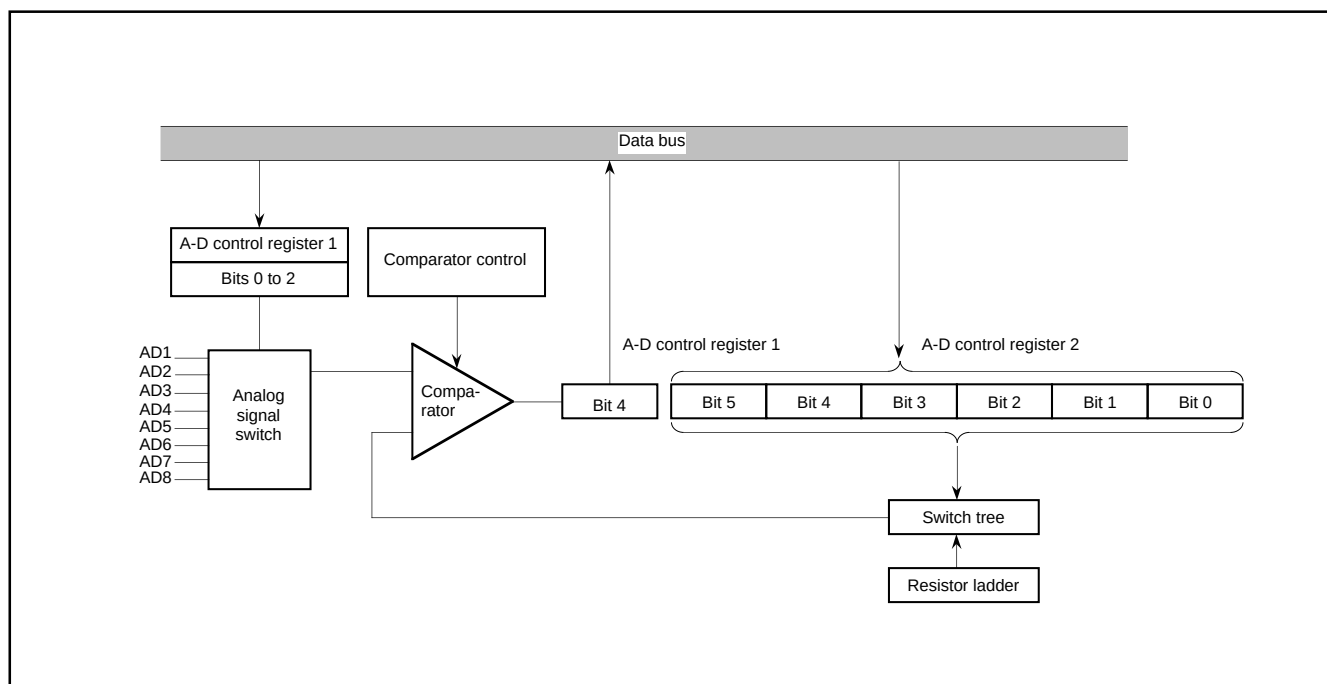
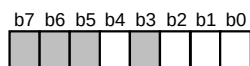


Fig. 40. A-D Comparator Block Diagram

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A-D Control Register 1

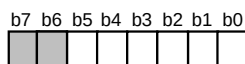


A-D control register 1 (ADM) [Address 00EF16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADM0 to ADM2)	b2 b1 b0 0 0 0 : AD1 0 0 1 : AD2 0 1 0 : AD3 0 1 1 : AD4 1 0 0 : AD5 1 0 1 : AD6 1 1 0 : AD7 1 1 1 : AD8	0	R	W
3, 5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	—

Fig. 41. A-D Control Register 1

A-D Control Register 2



A-D control register 2(ADC) [Address 020A16]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC0 to ADC5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc : 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	Indeterminate	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 42. A-D Control Register 2

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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 6 outlines the CRT display functions of this microcomputer. This microcomputer incorporates a CRT display circuit of 24 characters X 3 lines. CRT display is controlled by the CRT control register. Up to 256 kinds of characters can be displayed. The colors can be specified for each character and up to 4 kinds of colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B and I).

Characters are displayed in a 12 X 16 dots configuration to obtain smooth character patterns (refer to Figure 43).

The following shows the procedure how to display characters on the CRT screen.

- ① Write the display character code in the display RAM.
- ② Specify the display color by using the color register.
- ③ Write the color register in which the display color is set in the display RAM.
- ④ Specify the vertical position by using the vertical position register.
- ⑤ Specify the character size by using the character size register.
- ⑥ Specify the horizontal position by using the horizontal position register.
- ⑦ Write the display enable bit to the designated block display flag of the CRT control register 1. When this is done, the CRT display starts according to the input of the VSYNC signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (4 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 44 shows the CRT display control register 1. Figure 45 shows the block diagram of the CRT display circuit.

Table 6. Outline of CRT Display Functions

Parameter		Functions
Number of display characters		24 characters X 3 lines
Character display area		12 X 16 dots (refer to Figure 43)
Kinds of characters		256 kinds
Kinds of character sizes		4 kinds
Color	Kinds of colors	1 screen : 4 kinds, maximum 15 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 15 kinds)
Character background coloring		Possible (a character unit, 1 screen : 4 kinds, maximum 7 kinds)

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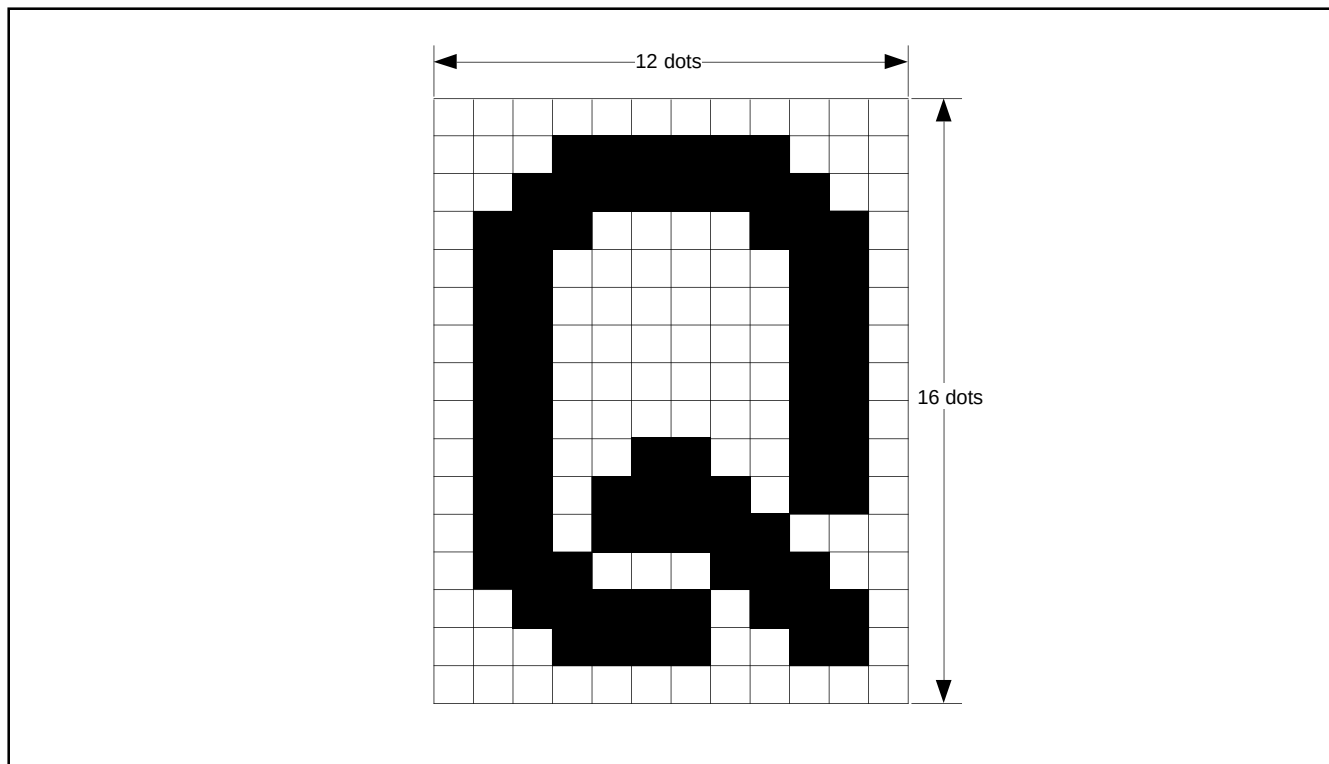
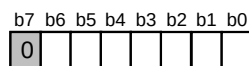


Fig. 43. CRT Display Character Configuration

CRT Control Register 1



CRT control register 1 (CC) [Address 00EA16]

B	Name	Functions	After reset	R	W
0	All-blocks display control bit (CC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Block 1 display control bit (CC1)	0 : Block 1 display off 1 : Block 1 display on	0	R	W
2	Block 2 display control bit (CC2)	0 : Block 2 display off 1 : Block 2 display on	0	R	W
3	Block 3 display control bit (CC3)	0 : Block 3 display off 1 : Block 3 display on	0	R	W
4	Block 1 color specification mode switch bit (CC4)	0 : Ordinary mode 1 : 1/2-character unit color specification mode	0	R	W
5	Display oscillation stop bit (CC5)	0 : Oscillation stopped 1 : Oscillation enabled	0	R	W
6	Scanning line double count mode flag(CC6)	0 : Ordinary 256 count mode 1 : Double count mode	0	R	W
7	Fix this bit to "0."		0	R	W

Note: Display is controlled by logical product (AND) between the all-blocks display control bit and each block control bit.

Fig. 44. CRT Control Register 1

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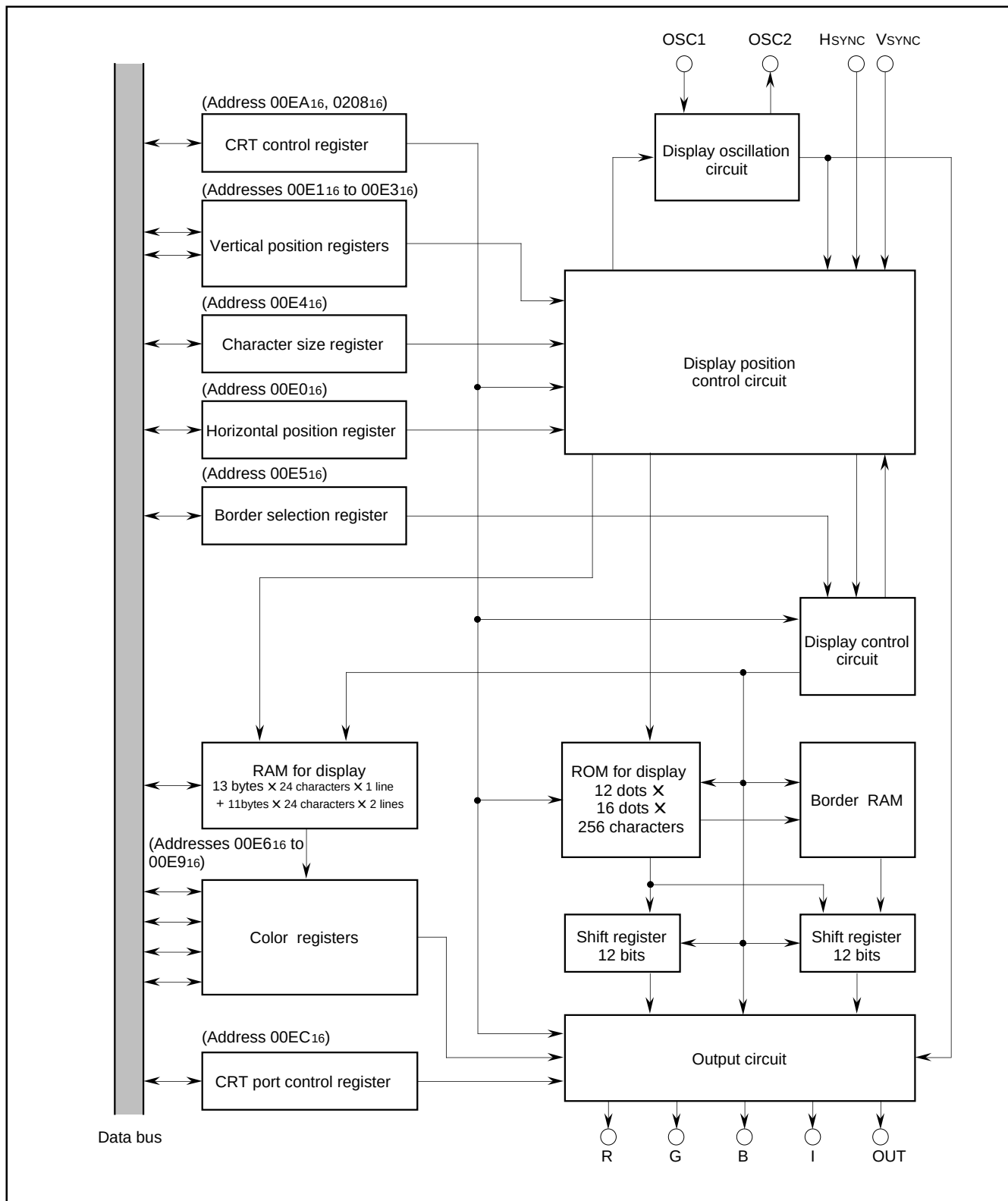


Fig. 45. Block Diagram of CRT Display Circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are 3 blocks, blocks 1 to 3. Up to 24 characters can be displayed in each block (refer to (4) Memory for Display).

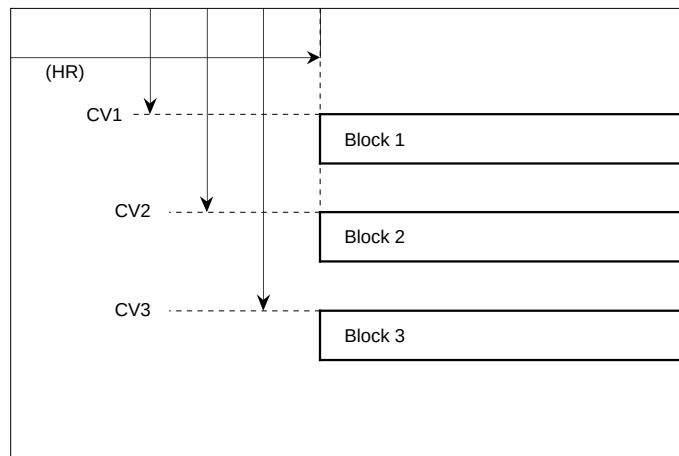
The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 64-step display positions in units of 4Tc (Tc = oscillating cycle for display).

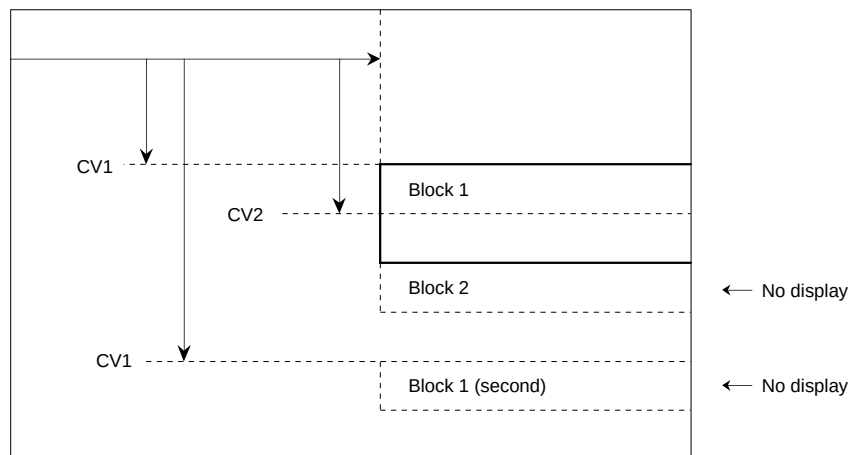
The display position in the vertical direction for each block can be selected from 128-step display positions in units of 4 scanning lines.

Block 2 is displayed after the display of block 1 is completed (refer to Figure 46 (a)). Accordingly, if the display of block 2 starts during the display of block 1, only block 1 is displayed. Similarly, when multiline display, block 1 is displayed after the display of block 2 is completed (refer to Figure 46 (b)).

The vertical position can be specified from 128-step positions (4 scanning lines per a step) for each block by setting values "00₁₆" to "7F₁₆" to bits 0 to 6 in the vertical position register (addresses 00E1₁₆ to 00E3₁₆). Figure 48 shows the vertical position register.



(a) Example when each block is separated



(b) Example when block 2 overlaps with block 1

Fig. 46. Display Position

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The display position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time, when VSYNC and HSYNC are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of HSYNC signal from after fixed cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the CRT port control register (address 00EC16).

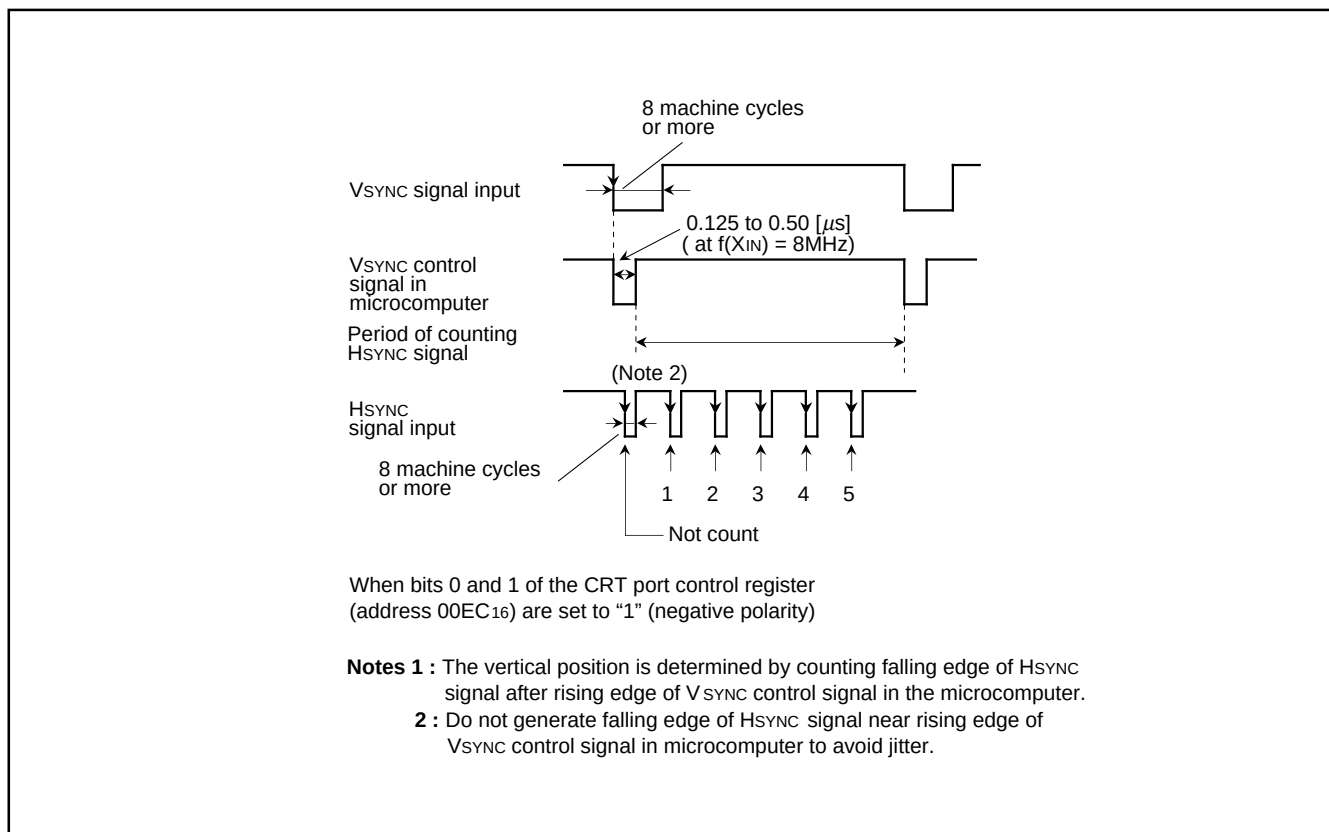


Fig. 47. Supplement Explanation for Display Position

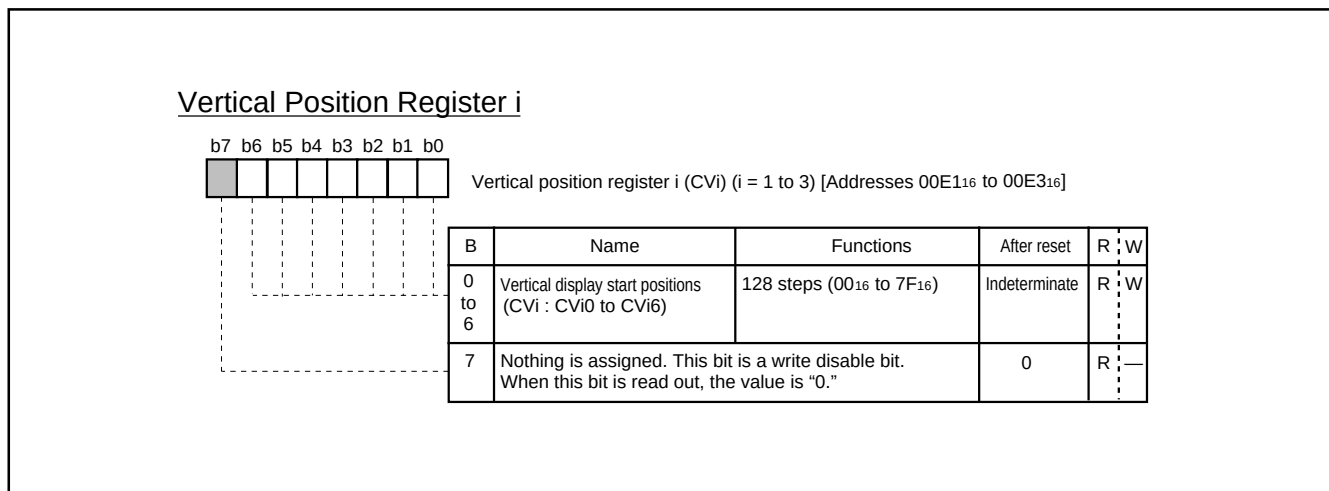


Fig. 48. Vertical Position Register i

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The horizontal position is common to all blocks, and can be set in 64 steps (where 1 step is 4Tosc, Tosc being the display oscillation period) as values "0016" to "3F16" in bits 0 to 5 of the horizontal position register (address 00E016). The structure of the horizontal position register is shown in Figure 49.

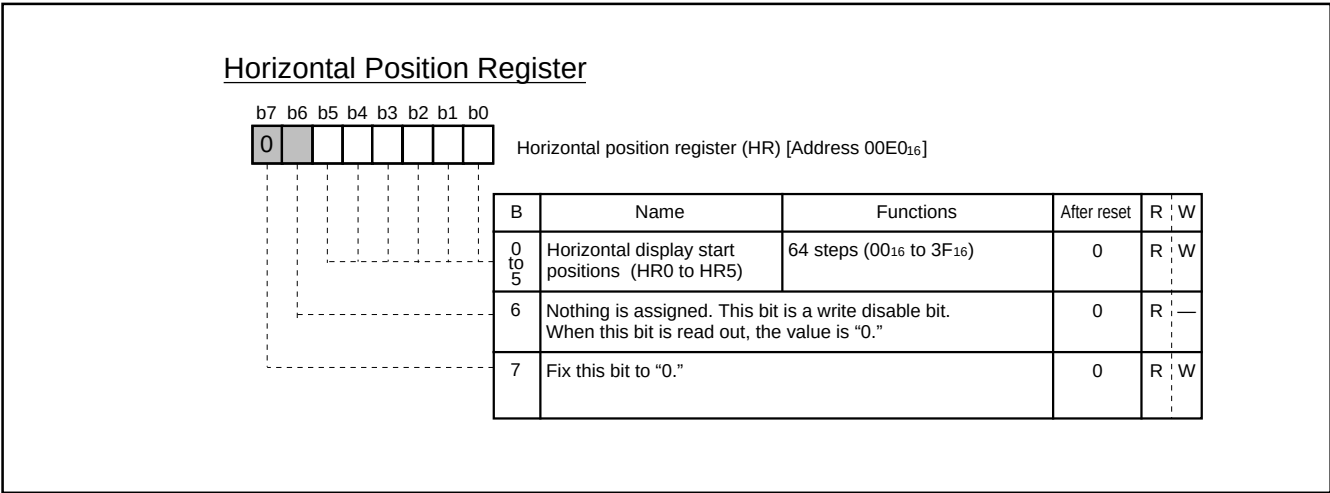


Fig. 49. Horizontal Position Register

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(3) Character Size

The size of characters to be displayed can be from 4 sizes for each block. Use the character size register (address 00E416) to set a character size. The character size of block 1 can be specified by using bits 0 and 1 of the character size register; the character size of block 2 can be specified by using bits 2 and 3; the character size of block 3 can be specified by using bits 4 and 5. Figure 51 shows the character size register.

The character size can be selected from 4 sizes: minimum size, medium size, large size and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the oscillating cycle for display (T_c) in the width (horizontal) direction. The minimum size consists of [1 scanning line] $\times$ [$1T_c$]; the medium size consists of [2 scanning lines] $\times$ [$2T_c$]; the large size consists of [3 scanning lines] $\times$ [$3T_c$]; and the extra large size consists of [4 scanning lines] $\times$ [$4T_c$]. Table 7 shows the relation between the set values in the character size register and the character sizes.

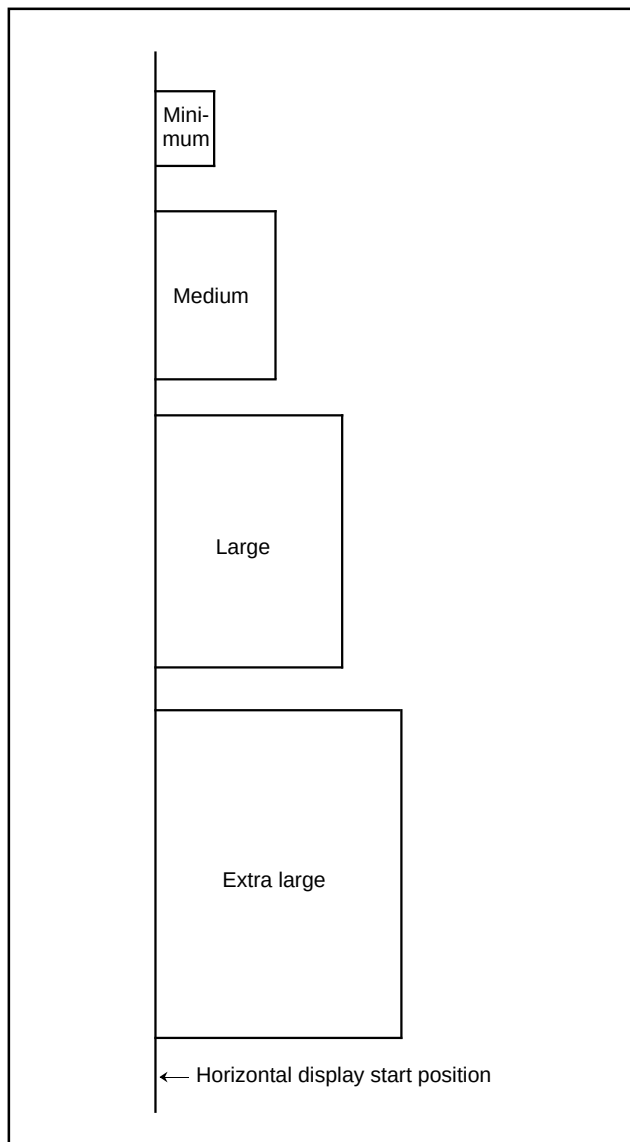
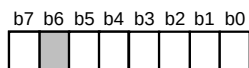


Fig. 50. Display Start Position of Each Character Size (horizontal direction)

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Character Size Register



Character size register (CS) [Address 00E4₁₆]

B	Name	Functions	After reset	R	W
0, 1	Character size of block 1 selection bits (CS10, CS11)	b1 b0 0 0 : Minimum size 0 1 : Medium size 1 0 : Large size 1 1 : Extra large size	Indeterminate	R	W
2, 3	Character size of block 2 selection bits (CS20, CS21)	b3 b2 0 0 : Minimum size 0 1 : Medium size 1 0 : Large size 1 1 : Extra large size	Indeterminate	R	W
4, 5	Character size of block 2 selection bits (CS30, CS31)	b5 b4 0 0 : Minimum size 0 1 : Medium size 1 0 : Large size 1 1 : Extra large size	Indeterminate	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
7	OUT signal output switch bit (CS7)	0 : OUT signal output 1 : MUTE signal output (See note)	Indeterminate	R	W

Note: This erases a video signal on an entire screen.

Fig. 51. Character Size Register

Table 7. Relation between Set Values in Character Size Register and Character Sizes

Set Values of Character Size Register		Character Size	Width (horizontal) Direction Tc: Oscillating Cycle for Display	Height (Vertical) Direction Scanning Lines
CSn0	CSn1			
0	0	Minimum	1Tc	1
0	1	Medium	2Tc	2
1	0	Large	3Tc	3
1	1	Extra large	4Tc	4

Note: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 50).

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(4) Memory for Display

There are 2 types of memory for display : CRT display ROM (addresses 10000_{16} to $12FFF_{16}$) used to store character dot data (masked) and CRT display RAM (addresses 0600_{16} to $06D7_{16}$) used to specify the colors and characters to be displayed. The following describes each type of display memory.

① ROM for display (addresses 10000_{16} to $12FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code based on the addresses in the CRT display ROM) into the CRT display RAM. The character code list is shown in Table 8.

The CRT display ROM has a capacity of 12 K bytes. Since 32 bytes are required for 1 character data, the ROM can store up to 384 kinds of characters.

The CRT display ROM space is broadly divided into 2 areas. The [vertical 16 dots] X [horizontal (left side) 8 dots] data of display characters are stored in addresses 10000_{16} to $107FF_{16}$, 11000_{16} to $117FF_{16}$ and 12000_{16} to $127FF_{16}$; the [vertical 16 dots] X [horizontal (right side) 4 dots] data of display characters are stored in addresses 10800_{16} to $10FFF_{16}$, 11800_{16} to $11FFF_{16}$ and 12800_{16} to $12FFF_{16}$ (refer to Figure 52). Note however that the high-order 4 bits in the data to be written to addresses 10800_{16} to $10FFF_{16}$, 11800_{16} to $11FFF_{16}$ and 12800_{16} to $12FFF_{16}$ must be set to "1" (by writing data "FX 16 ").

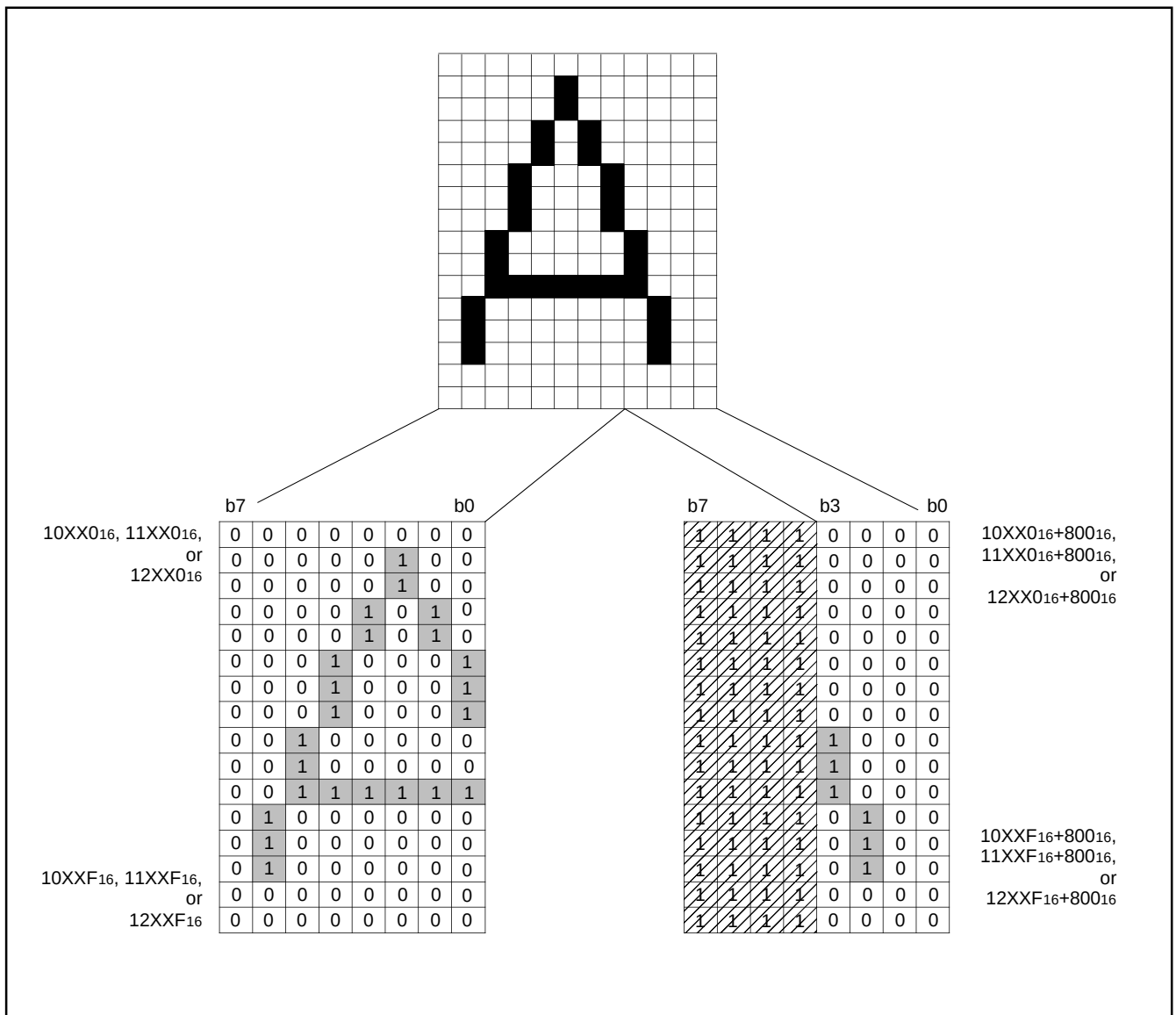


Fig. 52. Display Character Stored Data

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Table 8. Character Code List (partially abbreviated)

Character code	Character data storage address	
	Left 8 dots lines	Right 4 dots lines
000 ₁₆	10000 ₁₆ to 1000F ₁₆	10800 ₁₆ to 1080F ₁₆
001 ₁₆	10010 ₁₆ to 1001F ₁₆	10810 ₁₆ to 1081F ₁₆
002 ₁₆	10020 ₁₆ to 1002F ₁₆	10820 ₁₆ to 1082F ₁₆
003 ₁₆	10030 ₁₆ to 1003F ₁₆	10830 ₁₆ to 1083F ₁₆
:	:	:
07E ₁₆	107E0 ₁₆ to 107EF ₁₆	10FE0 ₁₆ to 10FEF ₁₆
07F ₁₆	107F0 ₁₆ to 107FF ₁₆	10FF0 ₁₆ to 10FFF ₁₆
080 ₁₆	11000 ₁₆ to 1100F ₁₆	11800 ₁₆ to 1180F ₁₆
081 ₁₆	11010 ₁₆ to 1101F ₁₆	11810 ₁₆ to 1181F ₁₆
:	:	:
17D ₁₆	127D0 ₁₆ to 127DF ₁₆	12FD0 ₁₆ to 12FDF ₁₆
17E ₁₆	127E0 ₁₆ to 127EF ₁₆	12FE0 ₁₆ to 12FEF ₁₆
17F ₁₆	127F0 ₁₆ to 127FF ₁₆	12FF0 ₁₆ to 12FFF ₁₆

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② RAM for display (addresses 0600₁₆ to 06D7₁₆)

The CRT display RAM is allocated at addresses 0600₁₆ to 06D7₁₆, and is divided into a display character code specification part and display color specification part for each block. Table 9 shows the contents of the CRT display RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0600₁₆ and write the color register No. to the low-order 2 bits (bits 0 and 1) in address 0680₁₆. The color register No. to be written here is one of the 4 color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers. The structure of the CRT display RAM is shown in Figure 53.

Table 9. Contents of CRT Display RAM

Block	Display Position (from left)	Character Code Specification		Color Specification
		Most Significant Bit	Low-order 8 bits	
Block 1	1st character	Bit 4 at 0680 ₁₆	0600 ₁₆	0680 ₁₆
	2nd character	Bit 4 at 0681 ₁₆	0601 ₁₆	0681 ₁₆
	3rd character	Bit 4 at 0682 ₁₆	0602 ₁₆	0682 ₁₆
	⋮	⋮	⋮	⋮
	22nd character	Bit 4 at 0695 ₁₆	0615 ₁₆	0695 ₁₆
	23rd character	Bit 4 at 0696 ₁₆	0616 ₁₆	0696 ₁₆
	24th character	Bit 4 at 0697 ₁₆	0617 ₁₆	0697 ₁₆
Not used		0698 ₁₆ to 069F ₁₆	0618 ₁₆ to 061F ₁₆	0698 ₁₆ to 069F ₁₆
Block 2	1st character	Bit 4 at 06A0 ₁₆	0620 ₁₆	06A0 ₁₆
	2nd character	Bit 4 at 06A1 ₁₆	0621 ₁₆	06A1 ₁₆
	3rd character	Bit 4 at 06A2 ₁₆	0622 ₁₆	06A2 ₁₆
	⋮	⋮	⋮	⋮
	22nd character	Bit 4 at 06B5 ₁₆	0635 ₁₆	06B5 ₁₆
	23rd character	Bit 4 at 06B6 ₁₆	0636 ₁₆	06B6 ₁₆
	24th character	Bit 4 at 06B7 ₁₆	0637 ₁₆	06B7 ₁₆
Not used		06B8 ₁₆ to 06BF ₁₆	0638 ₁₆ to 063F ₁₆	06B8 ₁₆ to 06BF ₁₆
Block 2	1st character	Bit 4 at 06C0 ₁₆	0640 ₁₆	06C0 ₁₆
	2nd character	Bit 4 at 06C1 ₁₆	0641 ₁₆	06C1 ₁₆
	3rd character	Bit 4 at 06C2 ₁₆	0642 ₁₆	06C2 ₁₆
	⋮	⋮	⋮	⋮
	22nd character	Bit 4 at 06D5 ₁₆	0655 ₁₆	06D5 ₁₆
	23rd character	Bit 4 at 06D6 ₁₆	0656 ₁₆	06D6 ₁₆
	24th character	Bit 4 at 06D7 ₁₆	0657 ₁₆	06D7 ₁₆
Not used		06D8 ₁₆ to 06FF ₁₆	0658 ₁₆ to 067F ₁₆	06D8 ₁₆ to 06FF ₁₆

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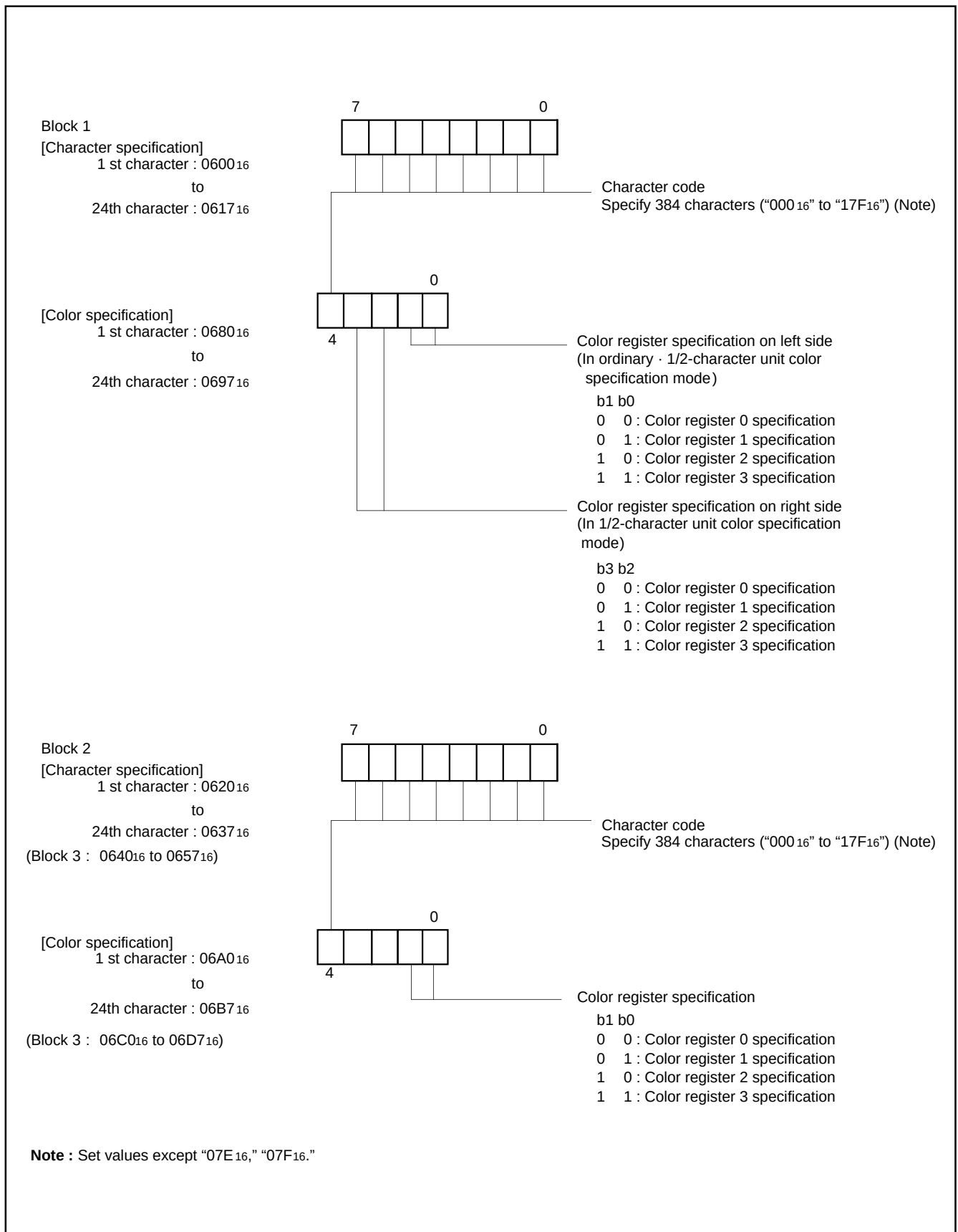


Fig. 53. Structure of RAM for Display

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(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the 4 registers (CO0 to CO3: addresses 00E6₁₆ to 00E9₁₆) and then specifying that color register with the CRT display RAM. There are 4 color outputs; R, G, B and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, since only 4 color registers are available, up to 4 colors can be disabled at one time.

R, G, B and I outputs are set by using bits 0 to 3 in the color register. Bit 5 is used to specify whether a character output or blank output. Bits 4, 6 and 7 are used to specify character background color. Figure 54 shows the structure of the color register.

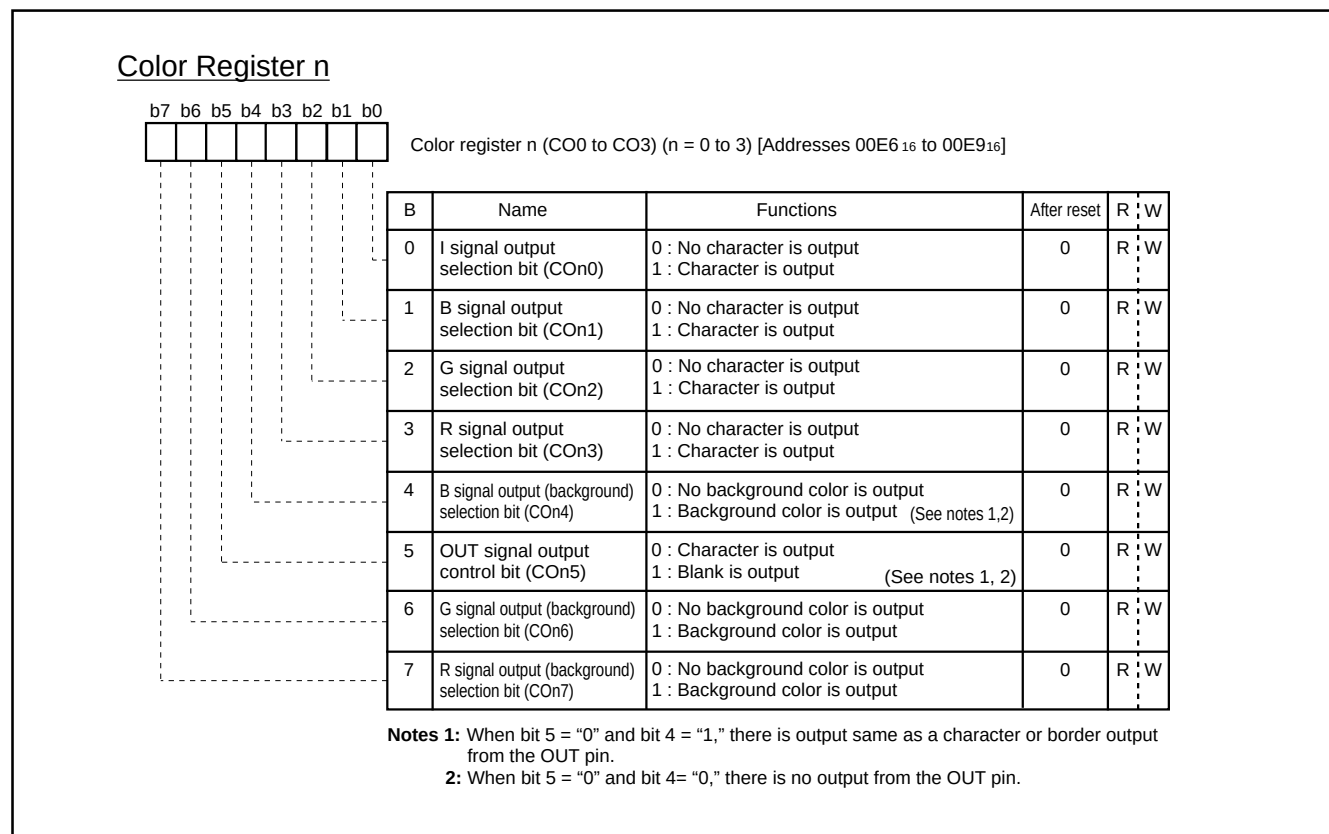


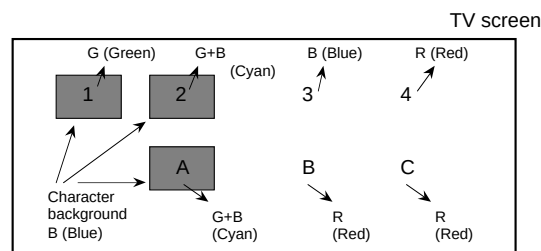
Fig. 54. Color Register n

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Table 10. Colorling to Character Background by R,G,B Output Signals

Color Register			RGB Output
Bit 7 (B)	Bit 6 (G)	Bit 3 (R)	Color
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White



Color registers (addresses 00E6₁₆ to 00E9₁₆)

Character	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	1	0	1	0	0
2	0	0	1	1	0	1	1	0
3	0	0	0	0	0	0	1	0
4	0	0	0	0	1	0	0	0
A	(R background)	(G background)	(OUT)	(B background)	(R)	(G)	(B)	(I)
B								
C								

Note : If border and background color are applied to a character in contact with a 12 X 16 -dot frame in the same block, the border (1 dot) is protruded from the frame.

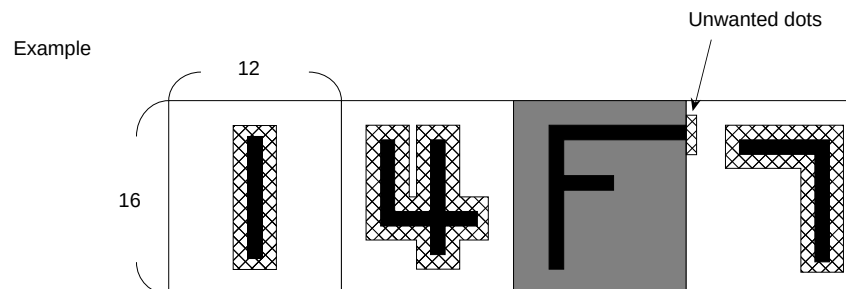
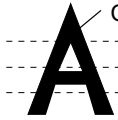
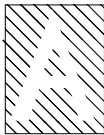
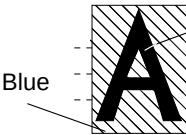
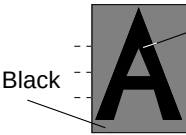


Fig. 55. Display Example

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Table 11. Display Example of Character Background Coloring (when green is set for a character and blue is set for background color)

Color registers								G output	B output	OUT output	Character output
CO _{n7}	CO _{n6}	CO _{n5}	CO _{n4}	CO _{n3}	CO _{n2}	CO _{n1}	CO _{n0}				
X	X	0	0	0	1	0	0	A	No output	No output	 Green TV image is displayed on the character background.
X	X	0	1	0	1	0	0	A	No output	A	 Green Same output as character A Video signal and character color (green) are not mixed.
0	0	1	1	0	1	0	0	A	 Background —character A	Blank output	 Green Blue TV image on the character background is not displayed.
0	0	1	0	0	1	0	0	A	No output	Blank output	 Green Black TV image on the character background is not displayed.

Notes 1: When CO_{n5} = "0" and CO_{n4} = "1," there is output same as a character or border output from the OUT pin.

When CO_{n5} = "0" and CO_{n4} = "0," there is no output from the OUT pin.

2: The portion "A" in which character dots are displayed is not mixed with any TV video signal.

3: The wavy-lined arrows in the table denote video signals.

4: n : 0 to 3, X : 0 or 1

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(6) 1/2-character Unit Color Specification Mode

By setting "1" to bit 4 of CRT control register 1 (address 00EA₁₆) it is possible to specify colors, in units of a 1/2-character size (16 dots high X 6 dots wide), to characters in only block 1.

In the 1/2-character unit color specification mode, colors of display characters in block 1 are specified as follows:

- The color on the left side :
this is set to the color of the color register which is specified by bits 0 and 1 at the color specification addresses (addresses 0680₁₆ to 0697₁₆) in the CRT display RAM.
- The color on the right side :
this is set to the color of the color register which is specified by bits 2 and 3 at the color specification addresses (addresses 0680₁₆ to 0697₁₆) in the CRT display RAM.

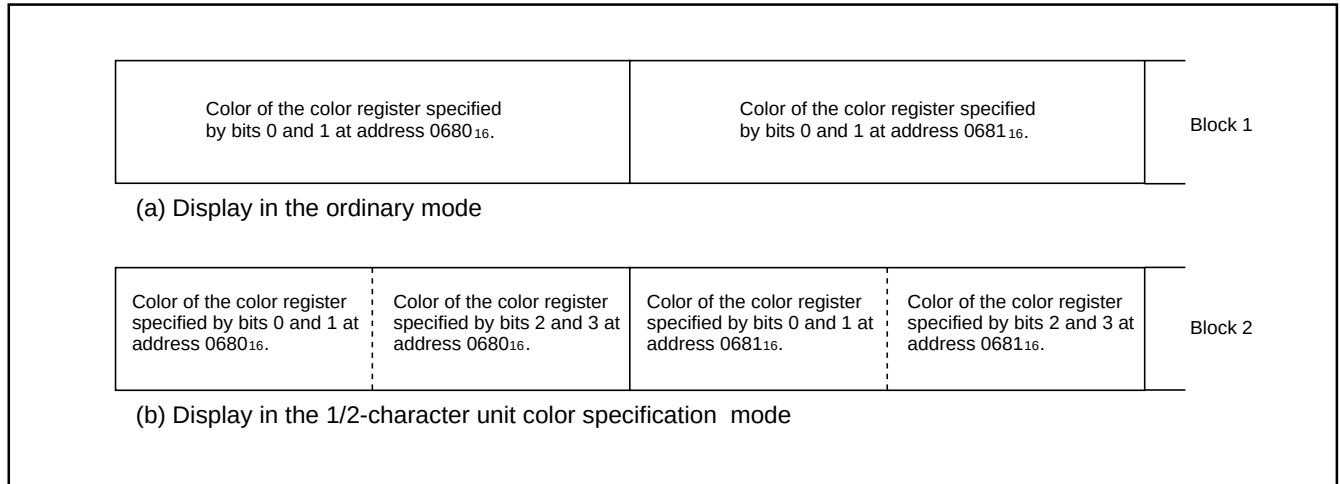


Fig. 56. Difference between Ordinary Color Specification Mode and 1/2-character Unit Color Specification Mode

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(7) Character Border Function

An border of 1 clock (1 dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT pin.

Border can be specified in units of block by using the border selection register (address 00E516). The setting of the border takes priority of the setting by bit 5 of the color register, however, the border of the character to which a background color has been set cannot be output. Figure 58 shows the border selection register. Table 12 shows the relationship between the values set in the border selection register and the character border function.

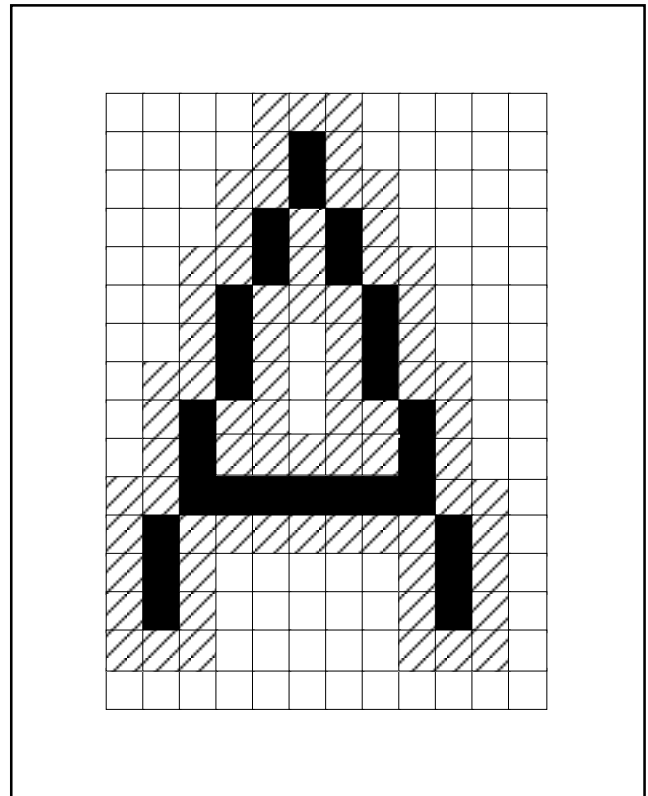
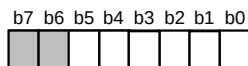


Fig. 57. Example of Border

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Border Selection Register



Border selection register (MD) [Address 00E5₁₆]

B	Name	Functions	After reset	R	W
0	Block 1 OUT output border selection bit (MD10)	0 : Same output as character output 1 : Border output	Indeterminate	R	W
1	Block 1 OUT output switch bit (MD11)	0 : Border including character 1 : Border only	Indeterminate	R	W
2	Block 2 OUT output border selection bit (MD20)	0 : Same output as character output 1 : Border output	Indeterminate	R	W
3	Block 2 OUT output switch bit (MD21)	0 : Border including character 1 : Border only	Indeterminate	R	W
4	Block 3 OUT output border selection bit (MD30)	0 : Same output as character output 1 : Border output	Indeterminate	R	W
5	Block 3 OUT output switch bit (MD31)	0 : Border including character 1 : Border only	Indeterminate	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 58. Border Selection Register

Table 12. Relationship between Set Value in Border Selection Register and Character Border Function

Border Selection Register		Functions	Example of Output
MDn1	MDn1		
X	0	Ordinary	R, G, B, I output OUT output
0	1	Border including character output	R, G, B, I output OUT output
1	1	Border only output	R, G, B, I output OUT output

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(8) Multiline Display

This microcomputer can ordinarily display 3 lines on the CRT screen by displaying 3 blocks at different vertical positions. In addition, it can display up to 16 lines by using CRT interrupts.

A CRT interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

Note: A CRT interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display with the display control bit of the CRT control register 1 (address 00EA16), a CRT interrupt request does not occur (refer to Figure 59).

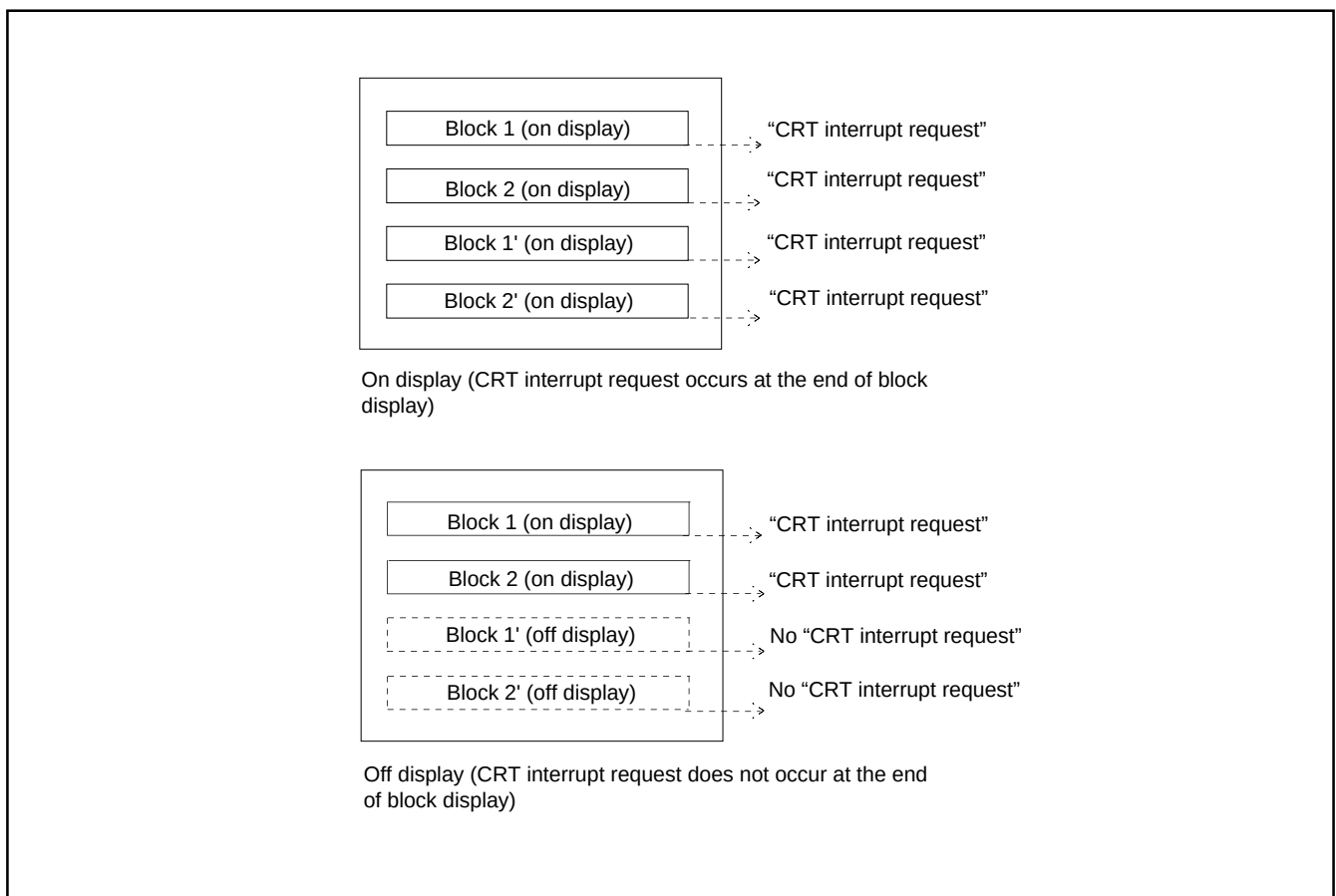


Fig. 59. Timing of CRT Interrupt Request

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The display block counter counts the number of times the display of a block has been completed, and its contents are incremented by 1 each time the display of one block is completed.

To provide multi-line display, enable CRT interrupts by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 of address 00FE16) to "1." After that, process the following sequence within the CRT interrupt processing routine:

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and vertical display position of that block with the character data (contents of CRT display RAM) and vertical display position (contents of vertical position register) to be displayed next.

Figure 60 shows the structure of the display block counter.

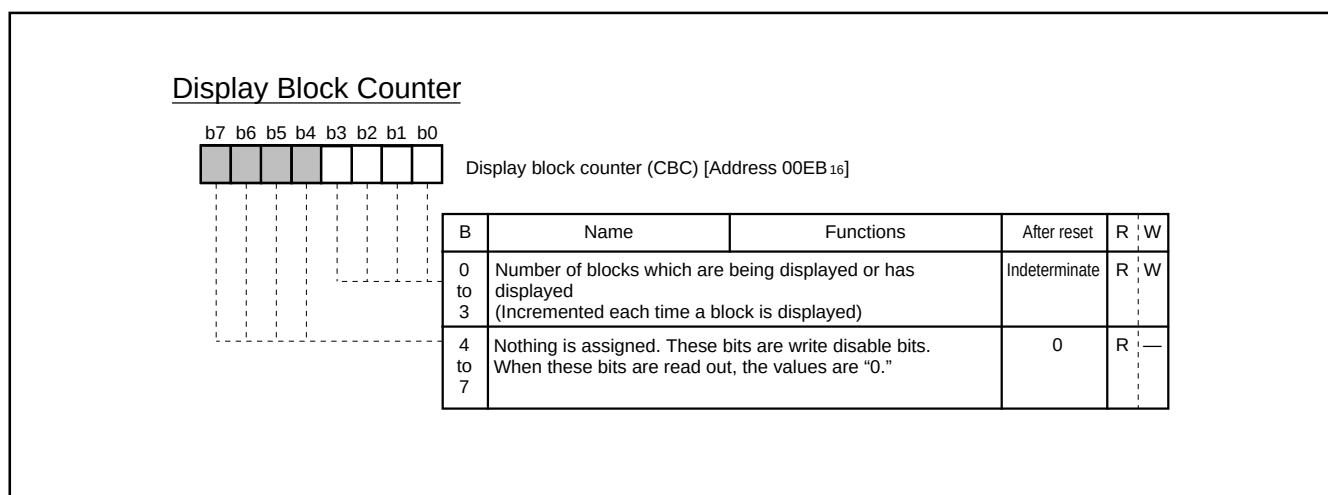


Fig. 60. Display Counter

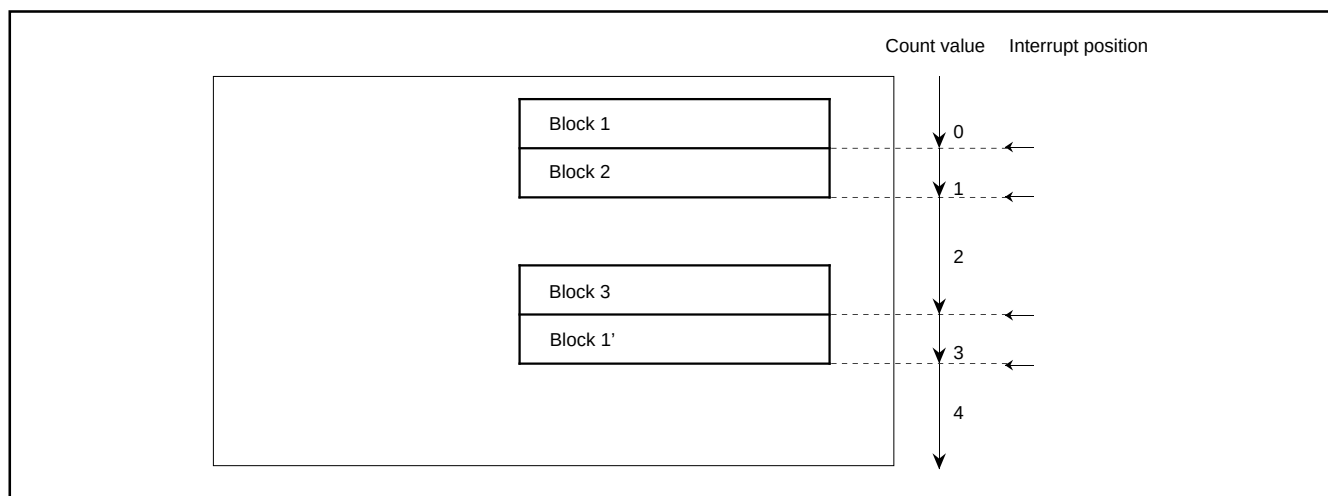


Fig. 61. Timing of CRT Interrupt Request and Display Counter Value

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(9) Scanning Line Double Count Mode

1 dot in a displayed character is normally shown with 1 scanning line. In the scanning double count mode, 1 dot can be shown with 2 scanning lines. As a result, the displayed dot is extended 2 times the normal size in the vertical direction only (that is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character becomes also twofold position in the vertical direction.

In other words, the contents of the vertical position register is as follows:

- In ordinary mode
256 steps as values "0016" to "FF16"
(4 scanning lines per step)
- In scanning line double count mode
128 steps as values "0016" to "7F16"
(8 scanning lines per step)

If the contents of the vertical position register for a block are set in the range of "8016" to "FF16" in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen). The scanning line double count mode is specified by setting bit 6 of the CRT control register 1 (address 00EA16) to "1."

Since this function works in units of a screen, even if the mode is changed during display of 1 screen, the mode before the change remains until the display of the next screen.

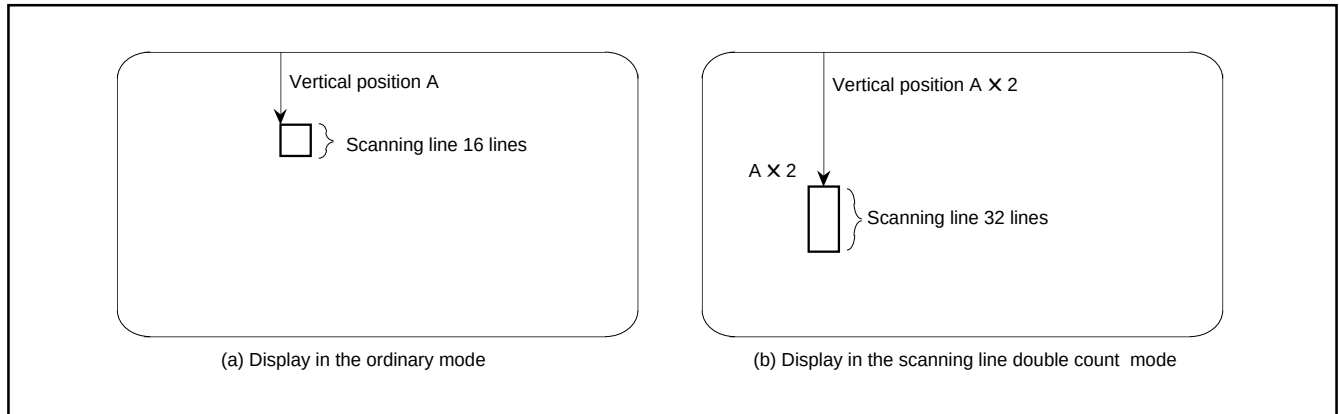


Fig. 62. Display in Ordinary Mode and in Scanning Line Double Count Mode

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(10) Wipe Function

① Wipe mode

This microcomputer allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: HSYNC signal).

There are 3 modes for this scroll method. Each mode has DOWN and UP modes, providing a total of 6 modes.

Table 13 shows the contents of each wipe mode.

Table 13. Wipe Operation in Each Mode and Values of Wipe Mode Register

Mode		Wipe Operation	Wipe Mode Register		
			Bit 2	Bit 1	Bit 0
1	DOWN	Appear from upper side	0	0	1
	UP	Erase from lower side	1	0	1
2	DOWN	Erase from upper side	0	1	0
	UP	Appear from lower side	1	1	0
3	DOWN	Erase from both upper and lower sides	0	1	1
	UP	Appear to both upper and lower sides	1	1	1

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②Wipe speed

The wipe speed is determined by the vertical synchronization (VSYNC) signal. For the NTSC interlace method, assuming that $V_{\text{SYNC}} = 16.7 \text{ ms}$, $262.5 \text{ H}_{\text{SYNC}}$ signals (per field) we obtain the wipe speed as shown in Table 14. Wipe resolution varies with each wipe mode. In mode 1 and mode 2, one of 3 resolutions (1H, 2H, 4H) can be selected. In mode 3, wipe is done in units of 4H only.

Table 14. Wipe Speed

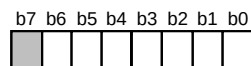
(NTSC interlace method, H = 262.5)

Wipe Resolution	Wipe Speed (entire screen)
1H Unit	$16.7 \text{ (ms)} \times 262.5 \div 1 \approx 4 \text{ (s)}$
2H Unit	$16.7 \text{ (ms)} \times 262.5 \div 2 \approx 2 \text{ (s)}$
4H Unit	$16.7 \text{ (ms)} \times 262.5 \div 4 \approx 1 \text{ (s)}$

Table 15. Wipe Mode and Wipe Resolution

Mode	Wipe Resolution	Wipe Speed
Mode 1	1H Unit	about 4 (s)
Mode 2	2H Unit	about 2 (s)
	4H Unit	about 1 (s)
Mode 3	4H Unit	about 1 (s)

Wipe Mode Register



Wipe mode register (SL) [Address 00ED₁₆]

B	Name	Functions	After reset	R	W
0, 1	Wipe mode selection bits (SL0, SL1)	b1 b0 0 0 : Wipe is not available 0 1 : Mode 1 1 0 : Mode 2 1 1 : Mode 3	0	R	W
2	Direction mode selection bits (SL2)	0: DOWN mode 1: UP mode	0	R	W
3, 4	Wipe unit selection bits (SL3, SL4)	b4 b3 0 0 : 1H unit 0 1 : 2H unit 1 0 : 3H unit 1 1 : Do not set	0	R	W
5, 6	Stop mode selection bits (SL5, SL6)	b6 b5 0 0 : Stop at the 312nd H 0 1 : Stop at the 156th H 1 0 : Stop at the 256th H 1 1 : Stop at the 128th H	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		0	R	—

Fig. 63. Structure of Wipe Mode Register

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(11) CRT Output Pin Control

The CRT output pins R, G, B, I and OUT can also function as ports P52, P53, P54, P55 and P56. Set the corresponding bit of the port P5 control register (address 00CB16) to "0" to specify these pins as CRT output pins, or set it to "1" to specify it as a general-purpose port P5 pins.

The input polarity of signals HSYNC and VSYNC and output polarity of signals R, G, B, I and OUT can be specified with the bits of the CRT port control register (address 00EC16). Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity.

The CRT clock I/O pins OSC1, OSC2 are controlled with the port control register (address 020616).

The CRT port control register is shown in Figure 64.

The port control register is shown in Figure 65.

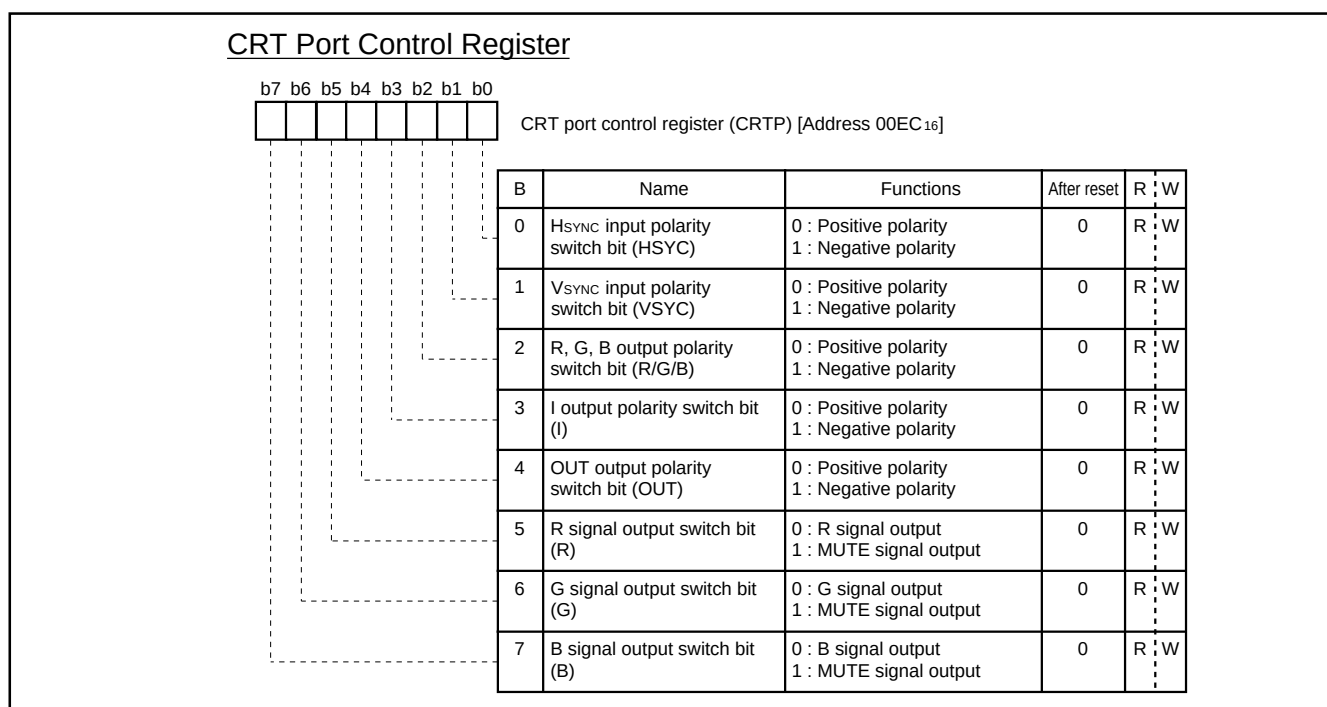


Fig. 64. CRT Port Control Register

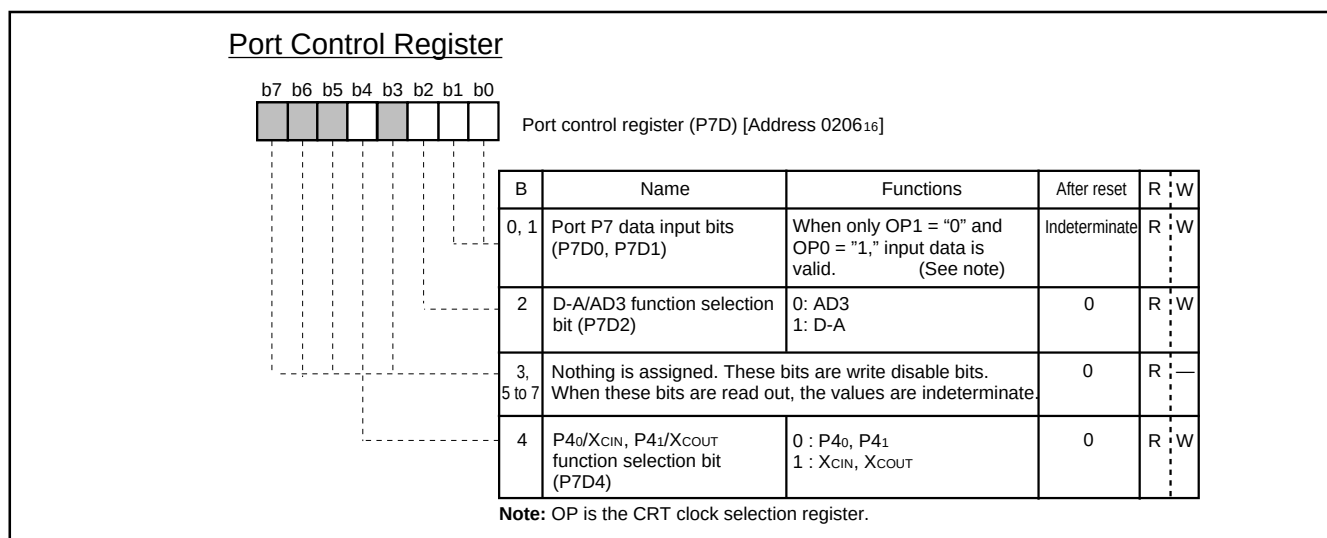


Fig. 65. Port Control Register

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(12) Raster Coloring Function

An entire screen (raster) can be colored by switching each of the R, G, and B pins to MUTE output. R, G, B are controlled with the CRT port control register; I is controlled with the CRT control register 2; OUT is controlled with the character size register. 15 raster colors can be obtained.

If the OUT pin has been set to raster coloring output, a raster coloring signal is always output during 1 horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, and B pins have been set to MUTE signal output, a raster coloring signal is output in the part except a no-raster colored character (in Figure 66, a character "O") during 1 horizontal scanning period. This ensures that character colors do not mix with the raster color. In this case, MUTE signal is output from the OUT pin.

An example in which a magenta character "I" and a red character "O" are displayed with blue raster coloring is shown in Figure 66.

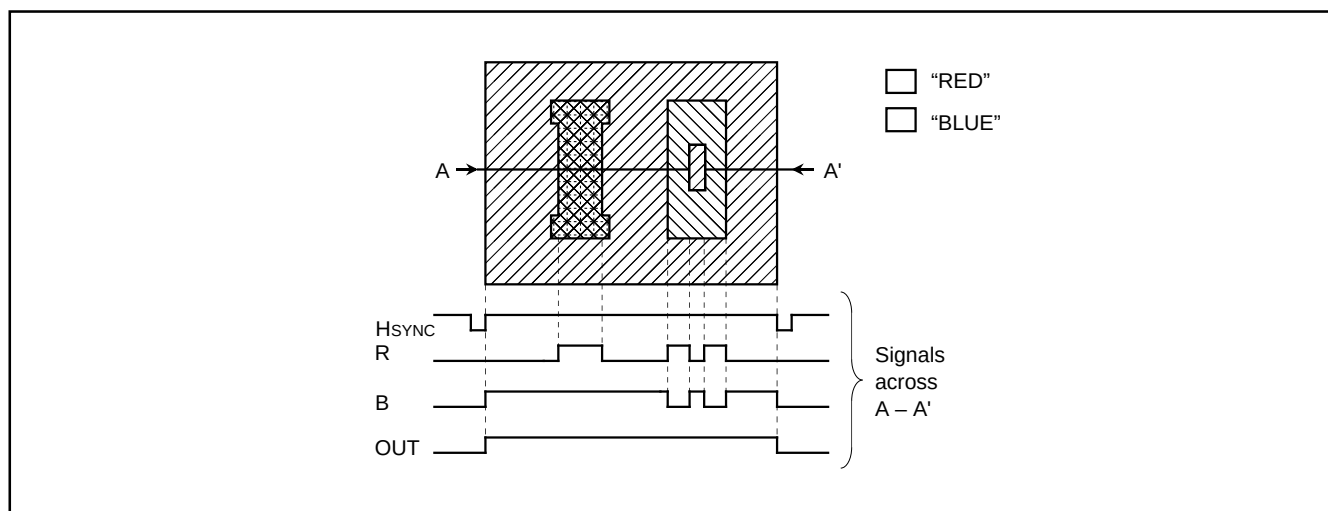


Fig. 66. Example of Raster Coloring

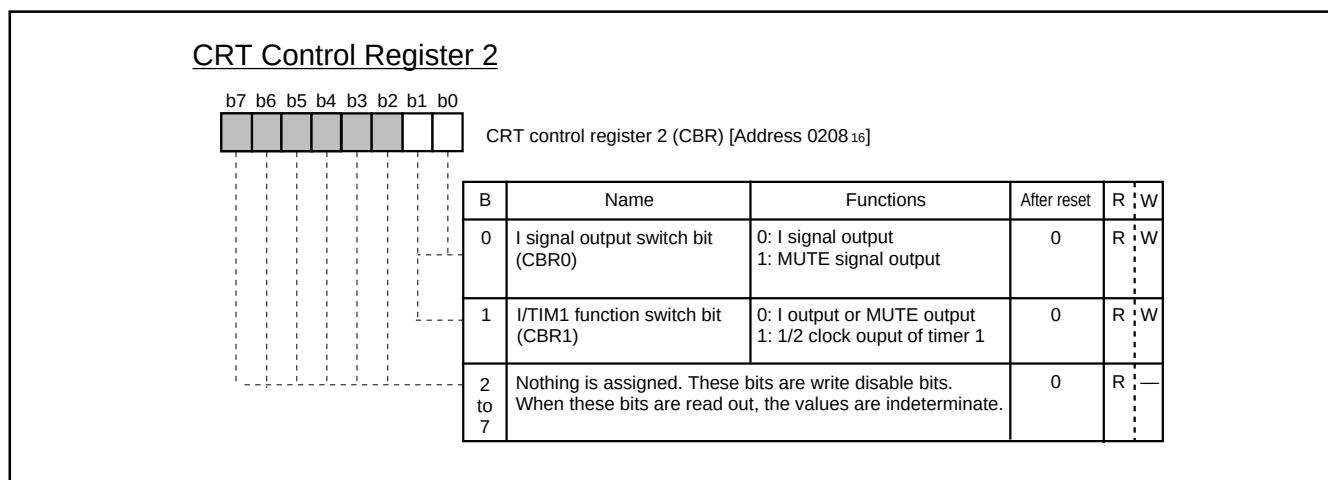


Fig. 67. CRT Control Register 2

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(13) Clock for Display

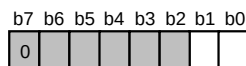
As a clock for display to be used for CRT display, it is possible to select one of the following 3 types.

- Main clock supplied from the X_{IN} pin
- Clock from the LC or RC supplied from the pins OSC1 and OSC2.
- Clock from the ceramic resonator or quartz-crystal oscillator supplied from the pins OSC1 and OSC2.

This clock for display can be selected for each block by the CRT clock selection register (address 0209₁₆).

When selecting the main clock, set the oscillation frequency to 8 MHz.

CRT Clock Selection Register



CRT clock selection register (OP) [Address 0209₁₆]

B	Name	Functions	After reset	R	W
0, 1	CRT clock selection bits (OP0, OP1)	b1 b0 Functions	0	R	W
		1 0 The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.			
		0 1 Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports P7 ₀ and P7 ₁ respectively.			
		1 0 Do not set.			
		1 1 The clock for display is supplied by connecting the following across the pins OSC1 and OSC2. • a ceramic resonator only for CRT display and a feedback resistor • a quartz-crystal oscillator only for CRT display and a feedback resistor (See note)			
2 to 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
7	Fix this bits to "0."		0	R	W

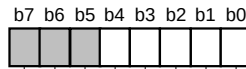
Notes 1: It is necessary to connect other ceramic resonator or quartz-crystal oscillator across the pins X_{IN} and X_{OUT} .
2: CC6 is the scanning line double count mode flag.

Fig. 68. CRT Clock Selection Register

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Interrupt Interval Determination Control Register



interrupt interval determination control register (RE) [Address 00D8₁₆]

B	Name	Functions	After reset	R	W
0	Interrupt interval determination circuit operation control bit (RE0)	0 : Stopped 1 : Operating	0	R	W
1	Reference clock selection bit (RE1)	0 : 16 μ s 1 : 32 μ s (at $f(X_{IN}) = 8$ MHz)	0	R	W
2	External interrupt input pin selection bit (RE2)	0 : INT1 input 1 : INT2 input	0	R	W
3	INT1 pin input polarity switch bit (RE3)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
4	INT2 pin input polarity switch bit (RE4)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 70. Interrupt Interval Determination Control Register

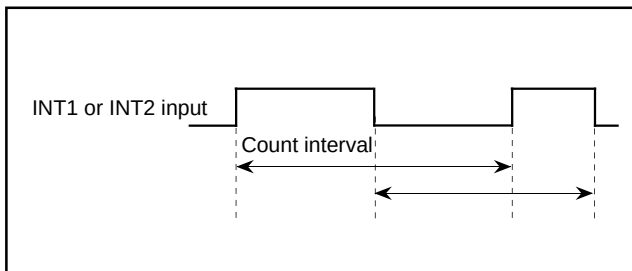


Fig. 71. Measuring Interval

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ROM CORRECTION FUNCTION

This can correct program data in ROM. Up to 2 addresses (2 blocks) can be corrected, a program for correction is stored in the ROM correction memory in RAM. The ROM memory for correction is 32 bytes X2 blocks.

Block 1 : addresses 02C0₁₆ to 02DF₁₆

Block 2 : addresses 02E0₁₆ to 02FF₁₆

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. When the blocks 1 and 2 are used in series, the above instruction is not needed at the end of the block 1.

The ROM correction function is controlled by the ROM correction enable register.

Notes 1 : Specify the first address (op code address) of each instruction as the ROM correction address.

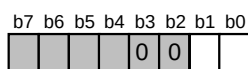
2 : Use the JMP instruction (total of 3 bytes) to return from the correction program to the main program.

3 : Do not set the same ROM correction address to the blocks 1 and 2.

ROM correction address 1 (high-order)	0217 ₁₆
ROM correction address 1 (low-order)	0218 ₁₆
ROM correction address 2 (high-order)	0219 ₁₆
ROM correction address 2 (low-order)	021A ₁₆

Fig. 72. ROM Correction Address Registers

ROM Correction Enable Register



ROM correction enable register (RCR) [Address 021B₁₆]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RC0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RC1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 73. ROM Correction Enable Register

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RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is $5\text{ V} \pm 10\%$, hold the $\overline{\text{RESET}}$ pin at LOW for $2\text{ }\mu\text{s}$ or more, then return it to HIGH. Then, as shown in Figure 75, reset is released and the program starts from the address formed by using the content of address FFFF_{16} as the high-order address and the content of the address FFFE_{16} as the low-order address. The internal state of microcomputer at reset are shown in Figure 75.

An example of the reset circuit is shown in Figure 74.

The reset input voltage must be kept 0.6 V or less until the power source voltage surpasses 4.5 V .

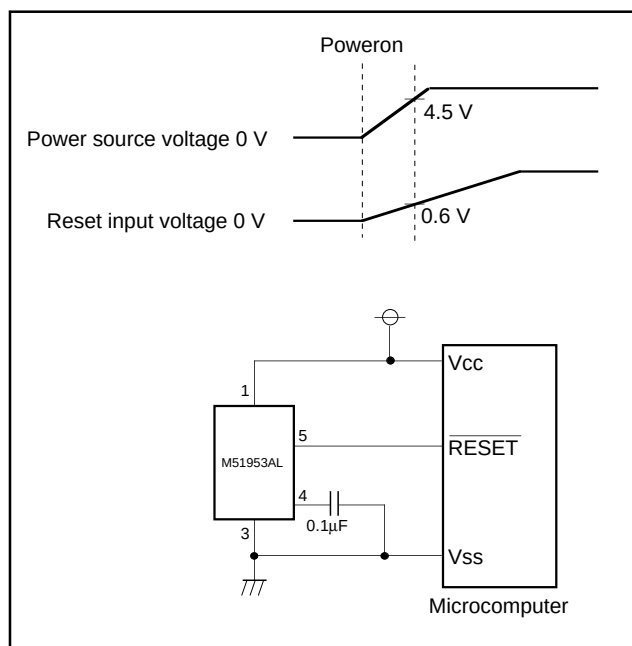


Fig. 74. Example of Reset Circuit

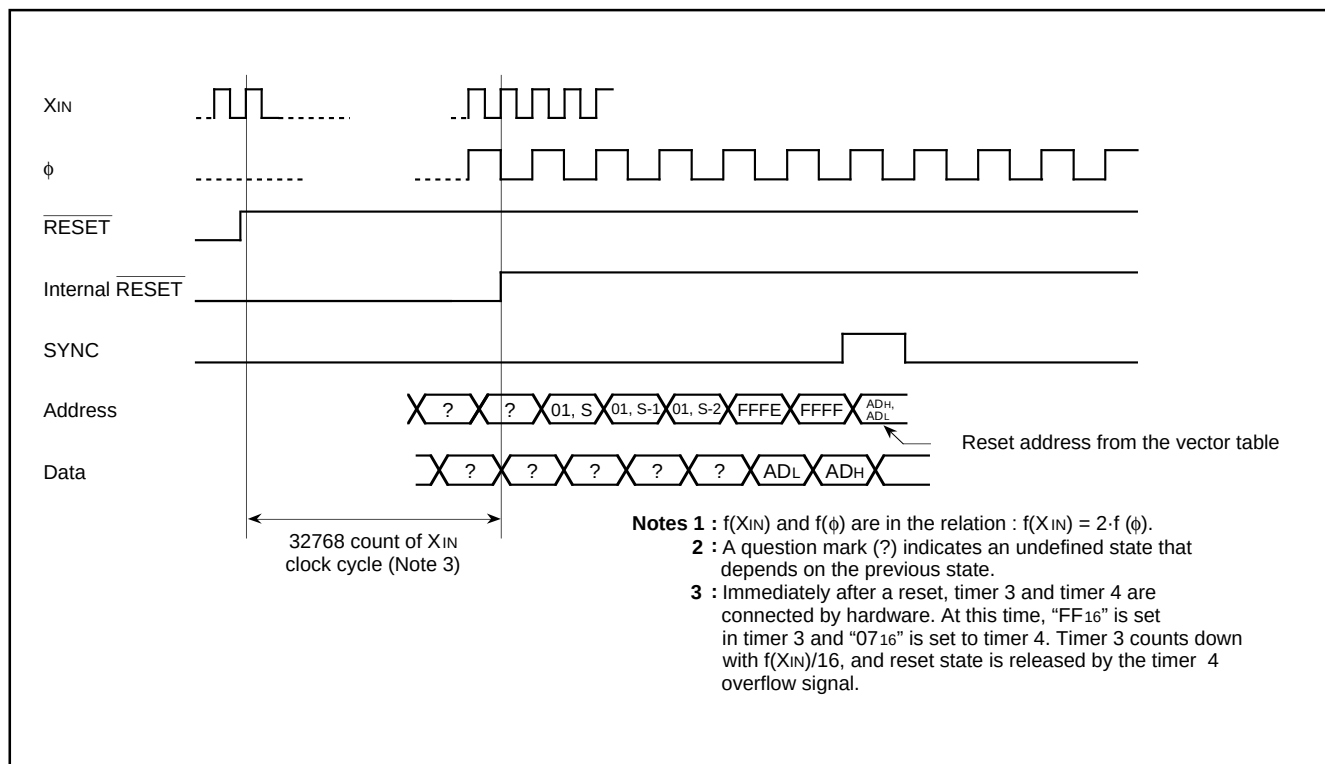


Fig. 75. Reset Sequence

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CLOCK GENERATING CIRCUIT

This microcomputer has 2 built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between X_{CIN} and X_{COUT} . When using X_{CIN} - X_{COUT} as sub-clock, clear bits 7 and 6 of the mixing control register to "0." To supply a clock signal externally, input it to the X_{IN} (X_{CIN}) pin and make the X_{OUT} (X_{COUT}) pin open. When not using X_{CIN} clock, connect the X_{CIN} to VSS and make the X_{COUT} pin open.

After reset has completed, the internal clock ϕ is half the frequency of X_{IN} . Immediately after poweron, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address 00FB16) to "1."

Oscillation Control

(1) Stop mode

The built-in clock generating circuit is shown in Figure 78. When the STP instruction is executed, the internal clock ϕ stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF16" is set in timer 3 and "0716" is set in the timer 4. Select $f(X_{IN})/16$ or $f(X_{CIN})/16$ as the timer 3 count source (set bit 0 of the timer mode register 2 to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. The oscillator restarts when external interrupt is accepted. However, the internal clock ϕ keeps its HIGH until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

(2) Wait mode

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is released at reset or when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once.

Note: In the wait mode, the following interrupts are invalid.

- (1) VSYNC interrupt
- (2) CRT interrupt
- (3) $f(X_{IN})/4096$ interrupt
- (4) Timer 1 and 2 interrupts using TIM2 pin input as count source
- (5) Timer 1 interrupt using $f(X_{IN})/4096$ or $f(X_{CIN})/4096$ as count source
- (6) Timer 3 interrupt using TIM3 pin input as count source
- (7) Multi-master I²C-BUS interface interrupt
- (8) Timer 4 interrupt using $f(X_{IN})/2$ or $f(X_{CIN})/2$ as count source

(3) Low-Speed Mode

If the internal clock is generated from the sub-clock (X_{CIN}), a low power consumption operation can be realized by stopping only the main clock X_{IN} . To stop the main clock, set bit 6 (CM6) of the CPU mode register (00FB16) to "1." When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize. Note that in low-power-consumption mode the X_{CIN} - X_{COUT} drivability can be reduced, allowing even lower power consumption (20 μ A with $f(X_{CIN}) = 32$ kHz). To reduce the X_{CIN} - X_{COUT} drivability, clear bit 5 (CM5) of the CPU mode register (00FB16) to "0." At reset, this bit is set to "1" and strong drivability is selected to help the oscillation to start. When an STP instruction is executed, set this bit to "1" by software before executing.

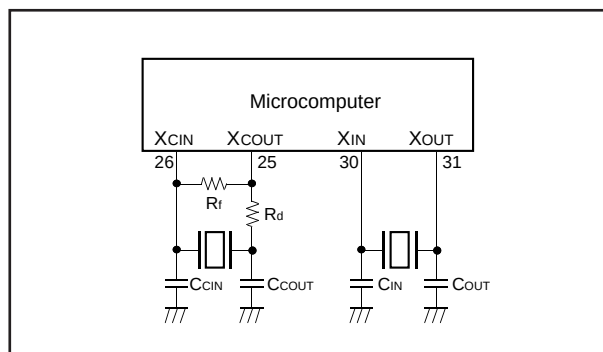


Fig. 76. Ceramic Resonator Circuit Example

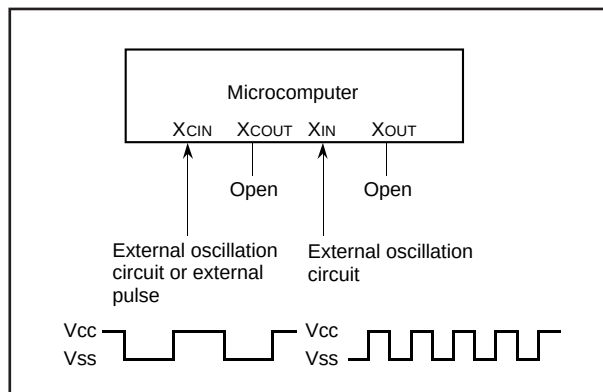


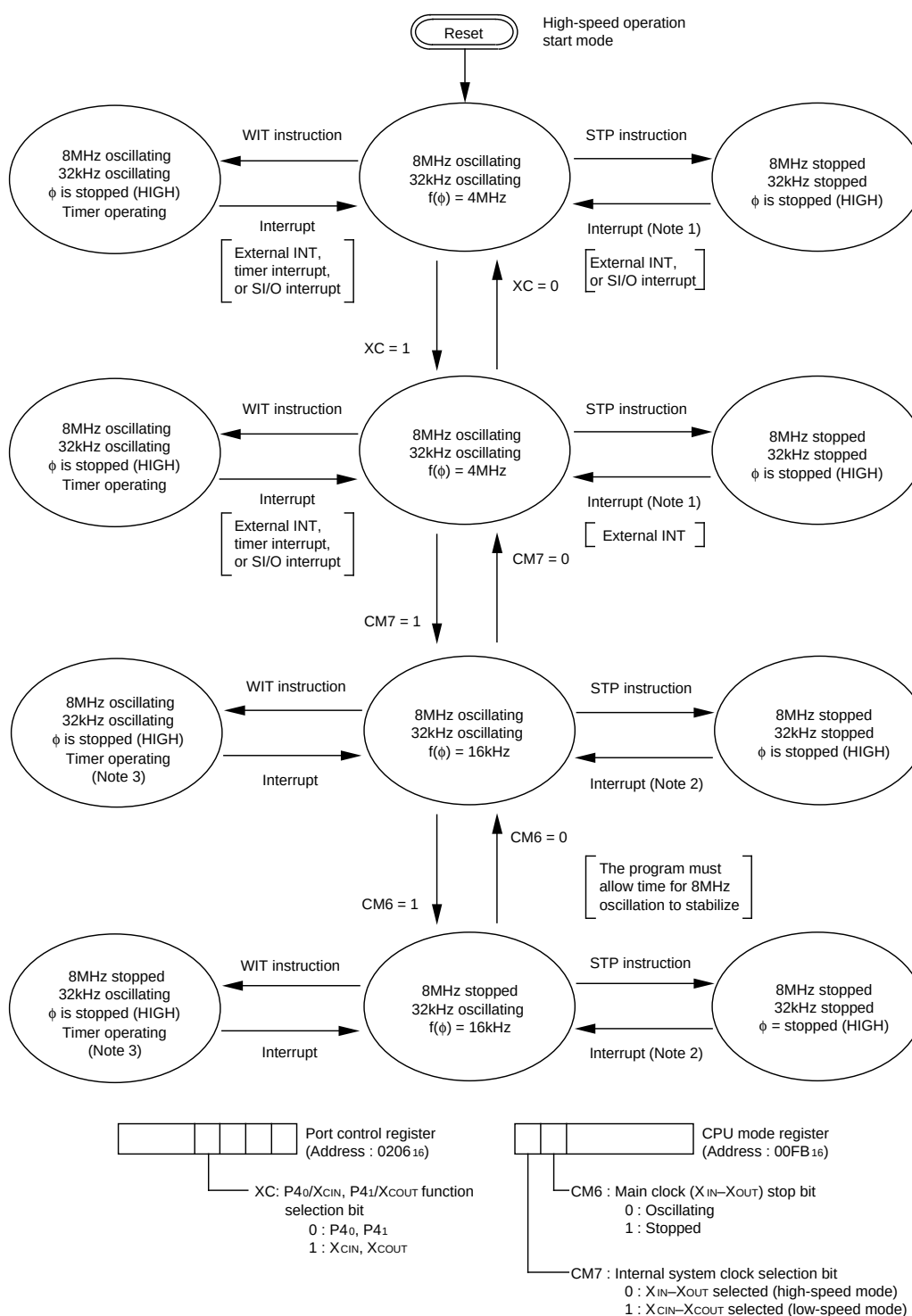
Fig. 77. External Clock Input Circuit Example

Notes 1: The value at reset is "0."
2: Refer to the structure of timer mode register 2.
3: Refer to the structure of CPU mode register (next page).
4: Refer to the structure of port control register.



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The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. The ϕ indicates the internal clock.

Notes 1: When the STP state is ended, a delay of approximately 8ms is automatically generated by timer 3 and timer 4.

2: The delay after the STP state ends is approximately 2s.

3: When the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is 2kHz.

Fig. 79. State Transitions of System Clock

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DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has a built-in clock oscillation circuits, so that a clock for CRT display can be obtained simply by connecting an LC, an RC, a quartz-crystal oscillator or a ceramic resonator across the pins OSC1 and OSC2. Which of the sub-clock or the display oscillation circuit is selected by setting bits 0 and 1 of the CRT clock selection register (address 020916).

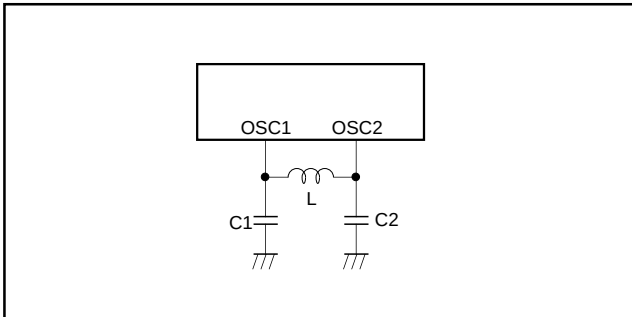


Fig. 80. Display Oscillation Circuit

AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the RESET pin.

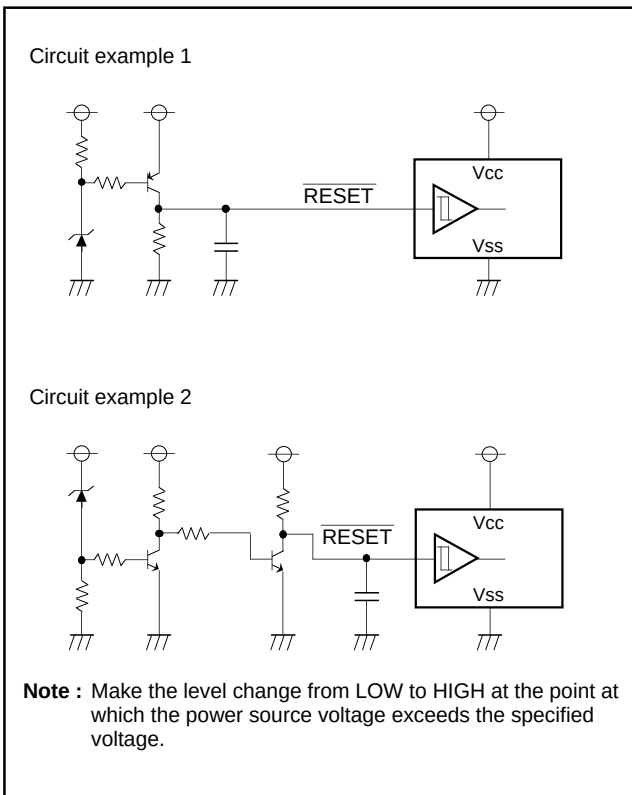


Fig. 81. Auto-clear Circuit Example

ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User's Manual for details.

MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Software> User's Manual for details.

PROGRAMMING NOTES

- (1) The divide ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- (4) An NOP instruction is needed immediately after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1 \mu\text{F}$) directly between the Vcc pin-Vss pin and the Vcc pin-CNVss pin, using a thick wire.

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DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form (32-pin DIP type 27C101, three identical copies)

PROM Programming Method

The built-in PROM of the One Time PROM version (blank) and the built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37207EFSP	PCA4762
M37207EFP	PCA7417

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process nor any following processes. To ensure proper operation after programming, the procedure shown in Figure 82 is recommended to verify programming.

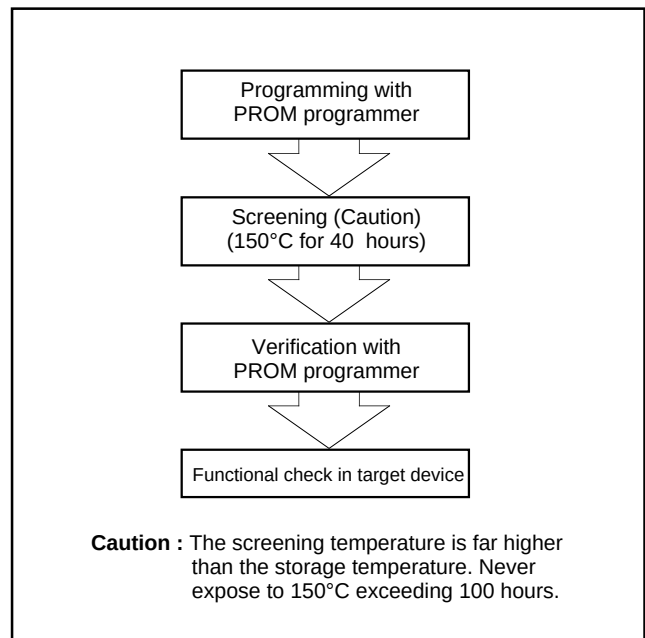


Fig. 82. Programming and Testing of One Time PROM Version

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage V _{CC}	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 6	V
V _I	Input voltage C _{NVSS}		−0.3 to 6	V
V _I	Input voltage P00–P07, P10–P17, P20–P27, P30–P36, P40–P47, P60–P67, P70, P71, OSC1, X _{IN} , H _{SYNC} , V _{SYNC} , RESET, X _{CIN} , AD1–AD8		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage P00–P07, P10–P17, P20–P27, P30–P36, P40–P45, R, G, B, I, OUT, D-A, X _{OUT} , X _{COUT} , OSC2		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage P46, P47, P60–P67		−0.3 to 13	V
I _{OH}	Circuit current R, G, B, I, OUT, P00–P07, P10–P17, P20–P27, P30, P31, D-A		0 to 1 (Note 1)	mA
I _{OL1}	Circuit current R, G, B, I, OUT, P00–P07, P10–P17, P20–P23, P30–P36, D-A		0 to 2 (Note 2)	mA
I _{OL2}	Circuit current P46, P47, P60–P67		0 to 1 (Note 2)	mA
I _{OL3}	Circuit current P24–P27		0 to 10 (Note 3)	mA
I _{OL4}	Circuit current P40–P45		0 to 6 (Note 2)	mA
P _d	Power dissipation		550	mW
T _{opr}	Operating temperature	T _a = 25 °C	−10 to 70	°C
T _{stg}	Storage temperature		−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −10 °C to 70 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Power source voltage (Note 4), During CPU, CRT operation	4.5	5.0	5.5	V
V _{SS}	Power source voltage	0	0	0	V
V _{IH1}	HIGH input voltage P00–P07, P10–P17, P20–P27, P30–P36, P60–P67, P70, P71, H _{SYNC} , V _{SYNC} , RESET, X _{IN} , X _{CIN} , OSC1, P40–P47 (including when using serial I/O)	0.8V _{CC}		V _{CC}	V
V _{IH2}	HIGH input voltage SDA3, SCL3, SDA2, SCL2, SDA1, SCL1 (When using I ² C-BUS)	0.7V _{CC}		V _{CC}	V
V _{IL1}	LOW input voltage P00–P07, P10–P17, P20–P27, P30, P31, P35, P40–P47, P70, P71	0		0.4 V _{CC}	V
V _{IL2}	LOW input voltage SDA3, SCL3, SDA2, SCL2, SDA1, SCL1 (When using I ² C-BUS)	0		0.3 V _{CC}	V
V _{IL3}	LOW input voltage H _{SYNC} , V _{SYNC} , RESET, P32–P34, P36, P41, P42, P44–P46, X _{IN} , X _{CIN} , OSC1 When using serial I/O; SOUT2, SCLK2, SIN2, SOUT1, SCLK1, SIN1	0		0.2 V _{CC}	V
I _{OH}	HIGH average output current (Note 1) R, G, B, I, OUT, D-A, P00–P07, P10–P17, P20–P27, P30, P31			1	mA
I _{OL1}	LOW average output current (Note 2) R, G, B, I, OUT, D-A, P00–P07, P10–P17, P20–P23, P30–P36			2	mA
I _{OL2}	LOW average output current (Note 2) P46, P47, P60–P67			1	mA
I _{OL3}	LOW average output current (Note 3) P24–P27			10	mA
I _{OL4}	LOW average output current (Note 2) P40–P45			6	mA
f(X _{IN})	Oscillation frequency (for CPU operation) (Note 5) X _{IN}	7.9	8.0	8.1	MHz
f(X _{CIN})	Oscillation frequency (for sub-clock operation) (Note 7) X _{CIN}	29	32	35	kHz
f _{osc}	Oscillation frequency (for CRT display) (Note 6) OSC1	6.0		13	MHz
f _{hs1}	Input frequency TIM2, TIM3, INT1, INT2			100	kHz
f _{hs2}	Input frequency SCLK1, SCLK2			1	MHz
f _{hs3}	Input frequency SCL1, SCL2, SCL3			400	kHz

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
I _{CC}	Power source current	System operation	V _{CC} = 5.5 V, f(X _{IN}) = 8 MHz	CRT OFF		15	30	mA
				CRT ON		30	45	
			V _{CC} = 5.5 V, f(X _{IN}) = 0, f(X _{CIN}) = 32kHz, CRT OFF, Low-power dissipation mode set (CM5 = "0," CM6 = "1")			100	200	μA
		Wait mode	V _{CC} = 5.5 V, f(X _{IN}) = 8 MHz			2	4	mA
			V _{CC} = 5.5 V, f(X _{IN}) = 0, f(X _{CIN}) = 32kHz, Low-power dissipation mode set (CM5 = "0," CM6 = "1")			60	100	
		Stop mode	V _{CC} = 5.5 V, f(X _{IN}) = 0, f(X _{CIN}) = 0			1	10	
V _{OH}	HIGH output voltage	R, G, B, I, OUT, P00–P07, P10–P17, P20–P27, D-A, P30, P31	V _{CC} = 4.5 V I _{OH} = -0.5 mA		2.4			V
V _{OL}	LOW output voltage	R, G, B, I, OUT, P00–P07, P10–P17, P20–P23, P30–P36, D-A	V _{CC} = 4.5 V I _{OL} = 0.5 mA				0.4	V
	LOW output voltage	P46, P47, P60–P67	V _{CC} = 4.5 V I _{OL} = 0.5 mA				0.4	
	LOW output voltage	P24–P27	V _{CC} = 4.5 V I _{OL} = 10.0 mA				3.0	
	LOW output voltage	P40–P45	V _{CC} = 4.5 V	I _{OL} = 3 mA			0.4	
				I _{OL} = 6 mA			0.6	
V _{T+} –V _{T-}	Hysteresis	RESET	V _{CC} = 5.0 V			0.5	0.7	V
	Hysteresis (Note 8)	HSYNC, VSYNC, P32, P33, P34, P36, P40–P46,	V _{CC} = 5.0 V			0.5	1.3	
I _{IzH}	HIGH input leak current	RESET, P00–P07, P10–P17, P20–P27, P30–P36, P40–P47, AD1–AD8	V _{CC} = 5.5 V V _I = 5.5 V				5	μA
I _{IzL}	LOW input leak current	RESET, P00–P07, P10–P17, P20–P27, P30–P36, P40–P46, P60–P67, AD1–AD8	V _{CC} = 5.5 V V _I = 0 V				5	μA
I _{OzH}	HIGH output leak current	P46, P47, P60–P67	V _{CC} = 5.5 V V _O = 12 V				10	μA
R _{BS}	I ² C-BUS·BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V _{CC} = 4.5 V				130	Ω

Notes 1: The total current that flows out of the IC must be 20 mA or less.

2: The total input current to IC (I_{OL1} + I_{OL2} + I_{OL4}) must be 30 mA or less.

3: The total average input current for ports P24–P27 to IC must be 20 mA or less.

4: Connect 0.022 m F or more capacitor externally between the power source pins V_{CC}–V_{SS} so as to reduce power source noise.

Also connect 0.068 m F or more capacitor externally between the pins V_{CC}–CNV_{SS}.

5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.

6: Use a RC or an LC for the CRT oscillation circuit.

7: When using the sub-clock, set f_{CLK} < f_{CPU}/3.

8: P32–P34 ,P36 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P40–P46 have the hysteresis when these pins are used as serial I/O pins.

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

A-D COMPARATOR CHARACTERISTICS

($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $f(X_{IN}) = 8\text{ MHz}$, $T_a = -10\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Absolute accuracy		0	± 1	± 2	LSB

Note: When $V_{CC} = 5\text{ V}$, 1 LSB = $5/64\text{ V}$.

MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		μs
$t_{HD:STA}$	Hold time for START condition	4.0		0.6		μs
t_{LOW}	"L" period of SCL clock	4.7		1.3		μs
t_R	Rising time of both SCL and SDA signals		1000	$20 + 0.1C_b$	300	ns
$t_{HD:DAT}$	Data hold time	0		0	0.9	μs
t_{HIGH}	"H" period of SCL clock	4.0		0.6		μs
t_F	Falling time of both SCL and SDA signals		300	$20 + 0.1C_b$	300	ns
$t_{SU:DAT}$	Data set-up time	250		100		ns
$t_{SU:STA}$	Set-up time for repeated START condition	4.7		0.6		μs
$t_{SU:STO}$	Set-up time for STOP condition	4.0		0.6		μs

Note: C_b = total capacitance of 1 bus line

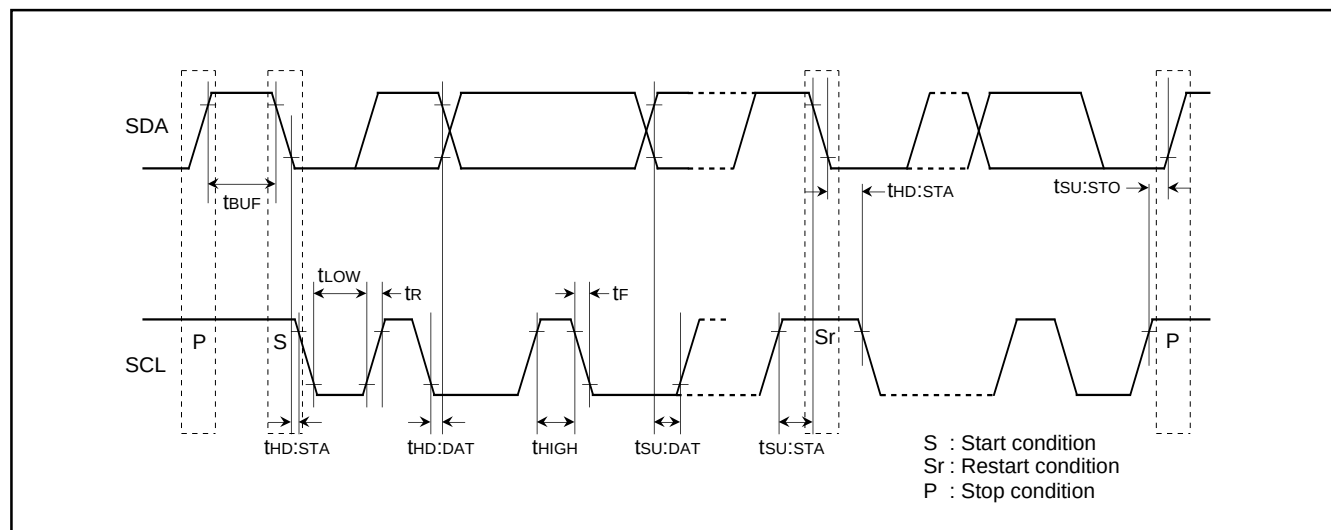


Fig. 83. Definition diagram of timing on multi-master I²C-BUS

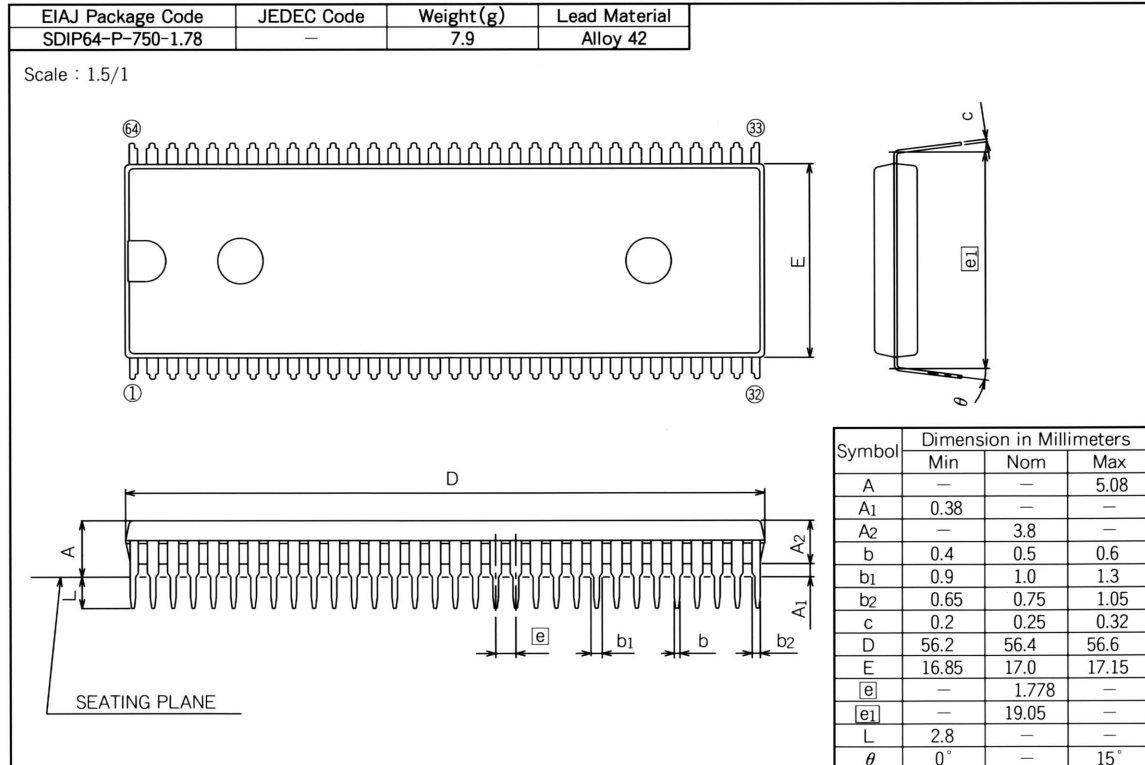
M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

PACKAGE OUTLINE

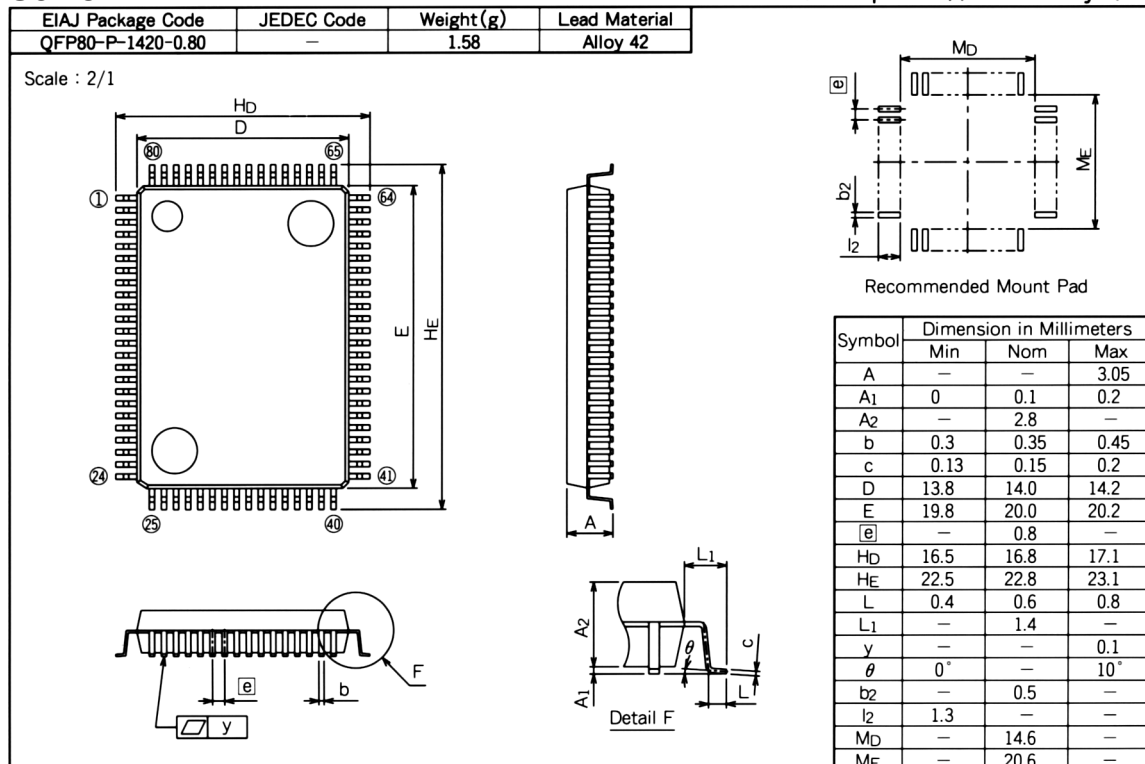
64P4B

Plastic 64pin 750mil SDIP



80P6N-A

Plastic 80pin 14×20mm body QFP



M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

GZZ-SH08-83B < 48B0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37207MF-XXXSP/FP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

*	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37207MF-XXXSP ☐ M37207MF-XXXFP

Checksum code for entire EPROM

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 (hexadecimal notation)

EPROM type (indicate the type used)

☐	27C101
EPROM address	
0000 ₁₆	Product name ASCII code : 'M37207MF-'
000F ₁₆	
0800 ₁₆	data
FFFF ₁₆	ROM 62K bytes
10000 ₁₆	Character ROM 1-a
10800 ₁₆	Character ROM 1-b
11000 ₁₆	Character ROM 2-a
11800 ₁₆	Character ROM 2-b
12000 ₁₆	Character ROM 3-a
12800 ₁₆	Character ROM 3-b
13000 ₁₆	
1FFFF ₁₆	

(1) Set "FF₁₆" in the shaded area.

(2) Write the ASCII codes that indicates the product name of "M37207MF-" to addresses 0000₁₆ to 000F₁₆.

EPROM data check item (Refer the EPROM data and check "✓" in the appropriate box)

- Do you set "FF₁₆" in the shaded area (set "F₁₆" in the low-order 4-bit shaded area) ? → Yes ☐
- Do you write the ASCII codes that indicates the product name of "M37207MF-" to addresses 0000₁₆ to 000F₁₆ ? → Yes ☐

* 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37207MF-XXXSP, 80P6N for M37207MF-XXXFP) and attach to the mask ROM confirmation form.

M37207MF-XXXSP/FP, M37207M8-XXXSP
M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

GZZ-SH08-83B <48B0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37207MF-XXXSP/FP
MITSUBISHI ELECTRIC

Writing the product name and character ROM data onto EPROMs

Addresses 0000₁₆ to 000F₁₆ store the product name, and addresses 10000₁₆ to 12FFF₁₆ store the character pattern.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code
ASCII codes 'M37207MF-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	FF ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	FF ₁₆
0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆	FF ₁₆
0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆	FF ₁₆
0005 ₁₆	'7' = 3 7 ₁₆	000D ₁₆	FF ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	FF ₁₆
0007 ₁₆	'F' = 4 6 ₁₆	000F ₁₆	FF ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1, character ROM2 and character ROM3. For the character ROM data, see the next page and on.

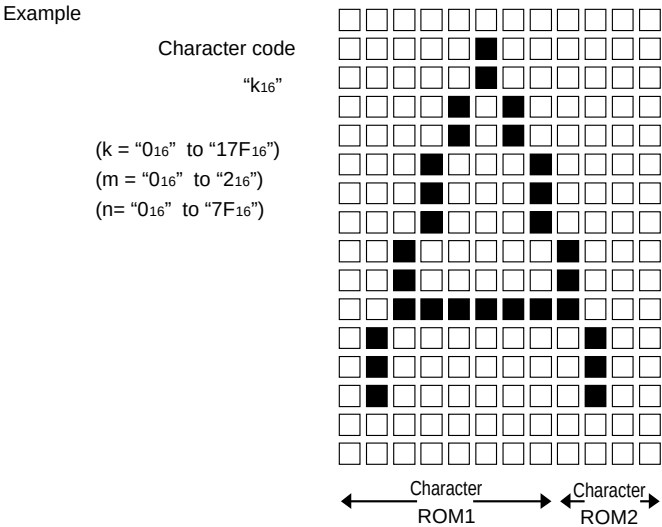
M37207MF-XXXSP/FP, M37207M8-XXXSP
M37207EFSP/FP

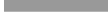
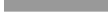
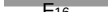
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

GZZ-SH08-83B< 48B0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37207MF-XXXSP/FP
MITSUBISHI ELECTRIC

The structure of character ROM (divided of 12 X16 dots font)



Character ROM address									Character ROM data	Character ROM address									Character ROM data				
	b7	b6	b5	b4	b3	b2	b1	b0			b7	b6	b5	b4	b3	b2	b1	b0					
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +0 ₁₆									00 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +0 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +1 ₁₆									04 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +1 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +2 ₁₆									04 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +2 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +3 ₁₆									0A ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +3 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +4 ₁₆									0A ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +4 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +5 ₁₆									11 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +5 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +6 ₁₆									11 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +6 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +7 ₁₆									11 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +7 ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +8 ₁₆									20 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +8 ₁₆													F8 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +9 ₁₆									20 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +9 ₁₆												F8 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +A ₁₆									3F ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +A ₁₆												F8 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +B ₁₆									40 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +B ₁₆												F4 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +C ₁₆									40 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +C ₁₆												F4 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +D ₁₆									40 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +D ₁₆												F4 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +E ₁₆									00 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +E ₁₆												F0 ₁₆	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +F ₁₆									00 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +F ₁₆												F0 ₁₆	

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

GZZ-SH10-49B < 61A0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37207M8-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

*	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37207M8-XXXSP

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type (indicate the type used)

☐	27C101
EPROM address	
0000 ₁₆	Product name ASCII code : 'M37207M8 -'
000F ₁₆	
8000 ₁₆	data
FFFF ₁₆	ROM 32 K bytes
10000 ₁₆	Character ROM 1-a
10800 ₁₆	Character ROM 1-b
11000 ₁₆	Character ROM 2-a
11800 ₁₆	Character ROM 2-b
12000 ₁₆	
1FFFF ₁₆	

(1) Set "FF₁₆" ("F₁₆" in the high-order 4-bit shaded area) in the shaded area.

(2) Write the ASCII codes that indicate the product name of "M37207M8-" to addresses 0000₁₆ to 000F₁₆.

EPROM data check item (Confirm the EPROM data and check "✓" the appropriate box)

● Is "FF₁₆" in the shaded area (set "F₁₆" in the high-order 4-bit shaded area) ? → Yes ☐

● Are the ASCII codes that indicates the product name of "M37207M8-" to addresses 0000₁₆ to 000F₁₆ ? → Yes ☐

* 2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered. Fill out the appropriate mark specification form (64P4B for M37207M8-XXXSP) and attach to the mask ROM confirmation form.

M37207MF-XXXSP/FP, M37207M8-XXXSP
M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

GZZ-SH10-49B <61A0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37207M8-XXXSP
MITSUBISHI ELECTRIC

How to Write the Product Name and Character ROM Data onto EPROMs

Addresses 0000₁₆ to 000F₁₆ store the product name, and addresses 10000₁₆ to 11FFF₁₆ store the character pattern.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Please make sure the data is written correctly.

1. How to input the name of the product with the ASCII code :	Address		Address
ASCII codes 'M37207M8-' are listed on the right.	0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆
The addresses and data are in hexadecimal notation.	0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆
	0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆
	0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆
	0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆
	0005 ₁₆	'7' = 3 7 ₁₆	000D ₁₆
	0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆
	0007 ₁₆	'8' = 3 8 ₁₆	000F ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data, see the next page and on.

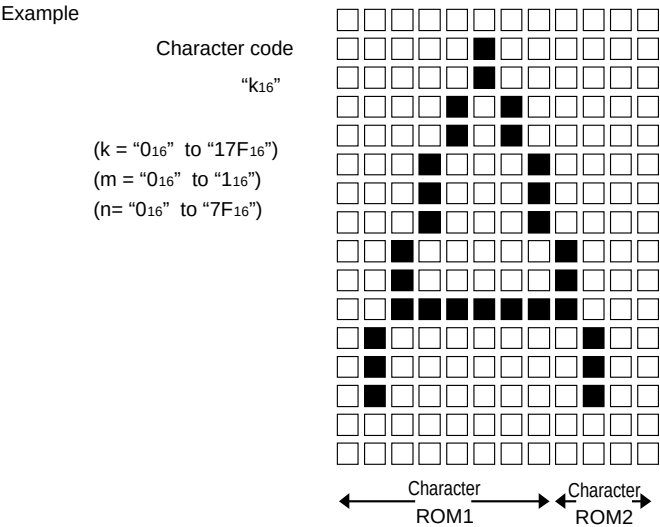
M37207MF-XXXSP/FP, M37207M8-XXXSP
M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

GZZ-SH10-49B< 61A0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37207M8-XXXSP
MITSUBISHI ELECTRIC

The structure of character ROM (divided of 12 X16 dots font)



Character ROM address								Character ROM data	Character ROM address								Character ROM data	
	b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0	
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +0 ₁₆									00 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +0 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +1 ₁₆									04 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +1 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +2 ₁₆									04 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +2 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +3 ₁₆									0A ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +3 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +4 ₁₆									0A ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +4 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +5 ₁₆									11 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +5 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +6 ₁₆									11 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +6 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +7 ₁₆									11 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +7 ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +8 ₁₆									20 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +8 ₁₆								F8 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +9 ₁₆									20 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +9 ₁₆								F8 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +A ₁₆									3F ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +A ₁₆								F8 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +B ₁₆									40 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +B ₁₆								F4 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +C ₁₆									40 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +C ₁₆								F4 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +D ₁₆									40 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +D ₁₆								F4 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +E ₁₆									00 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +E ₁₆								F0 ₁₆
10000 ₁₆ +m000 ₁₆ +n0 ₁₆ +F ₁₆									00 ₁₆	10800 ₁₆ +m000 ₁₆ +n0 ₁₆ +F ₁₆								F0 ₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

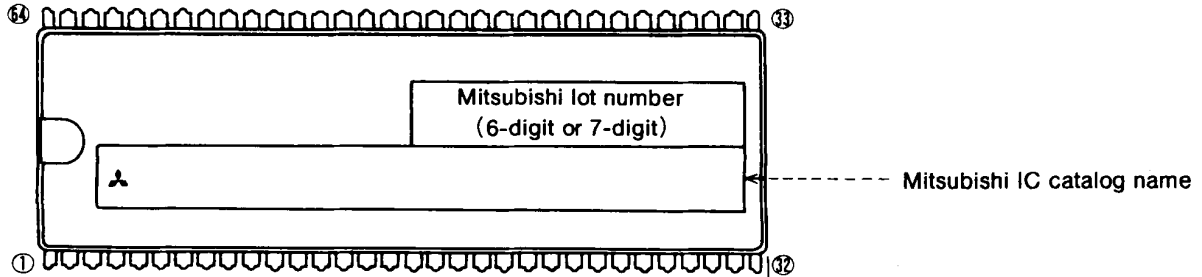
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 and ON-SCREEN DISPLAY CONTROLLER

64P4B (64-PIN SHRINK DIP) MARK SPECIFICATION FORM

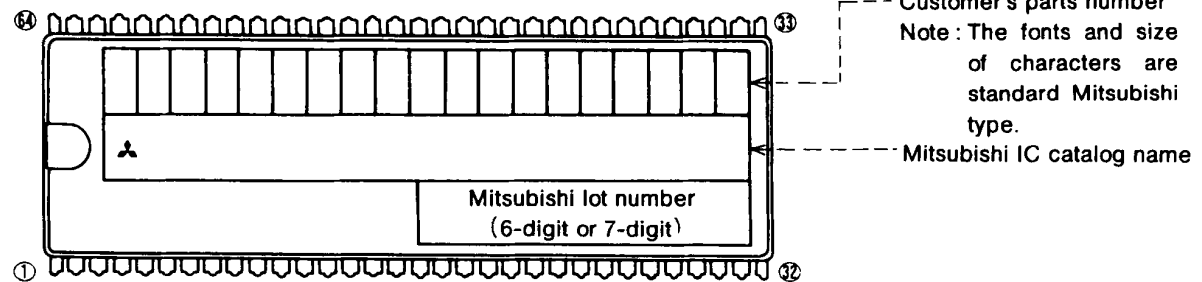
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

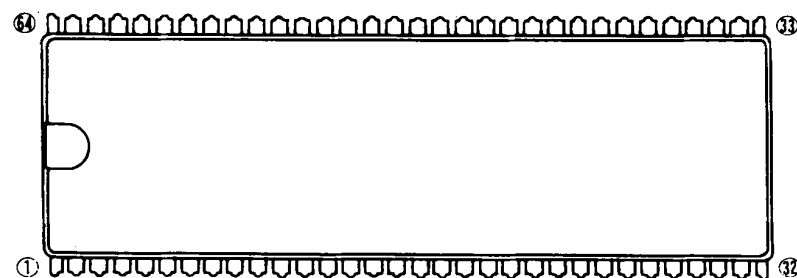
3 : Customer's parts number can be up to 19 characters :

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo is not required, check the box on the right.

☐ Mitsubishi logo is not required

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

☐ Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

☐

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

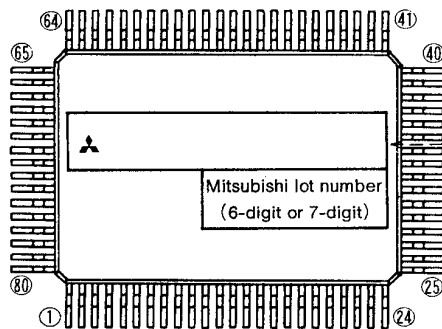
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 and ON-SCREEN DISPLAY CONTROLLER

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

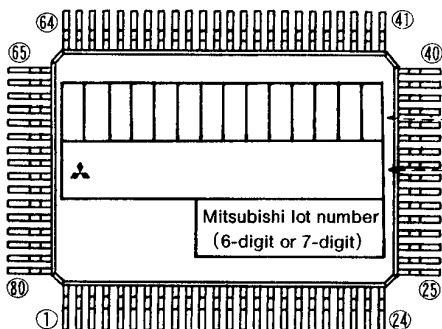
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number

Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note3: Customer's parts number can be up to 14 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

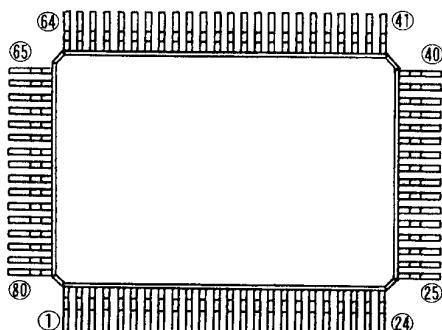
☐ Mitsubishi logo is not required

☐

Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

☐ Special logo required

☐

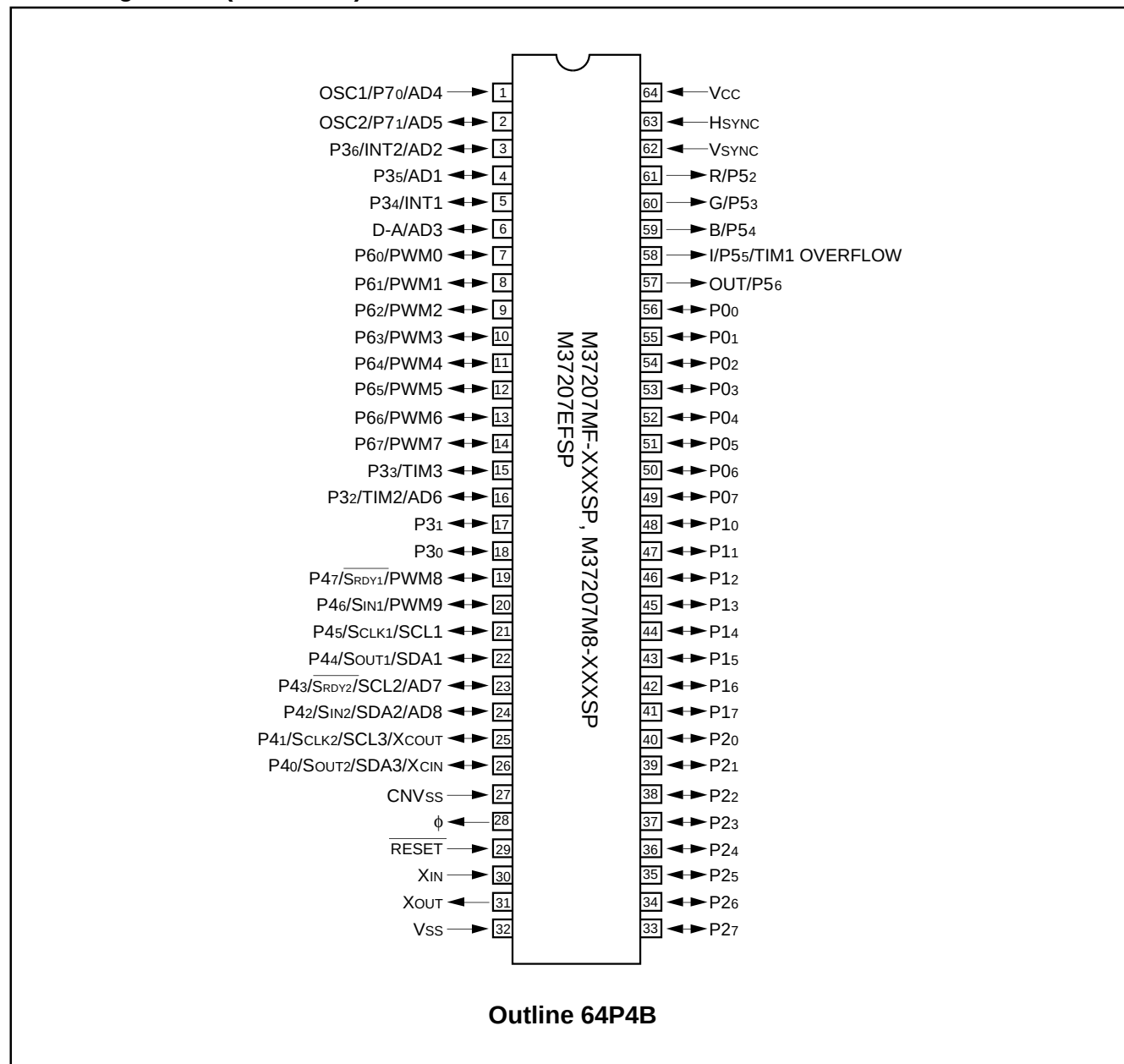
The standard Mitsubishi font is used for all characters except for a logo.

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

APPENDIX

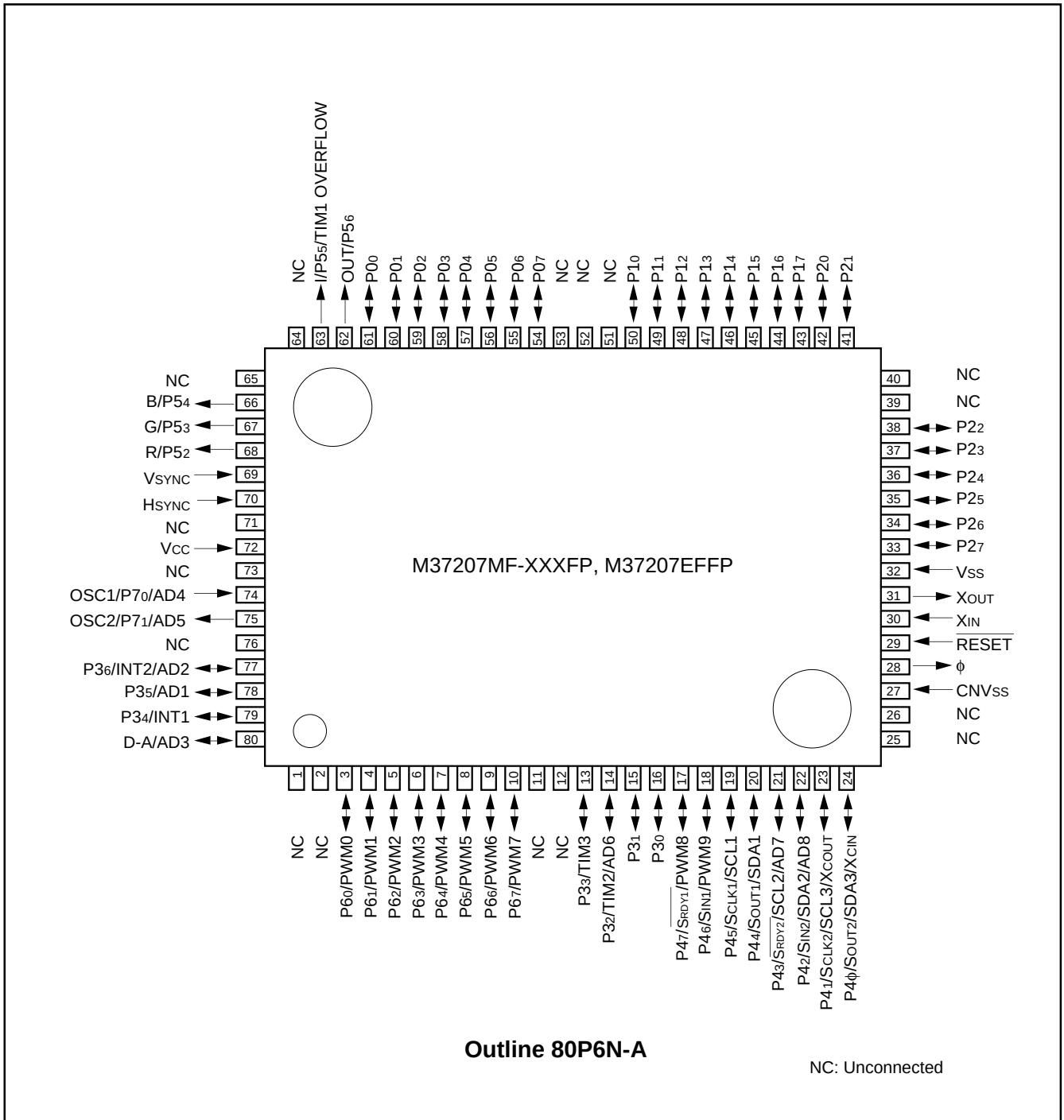
Pin Configuration (TOP VIEW)



M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

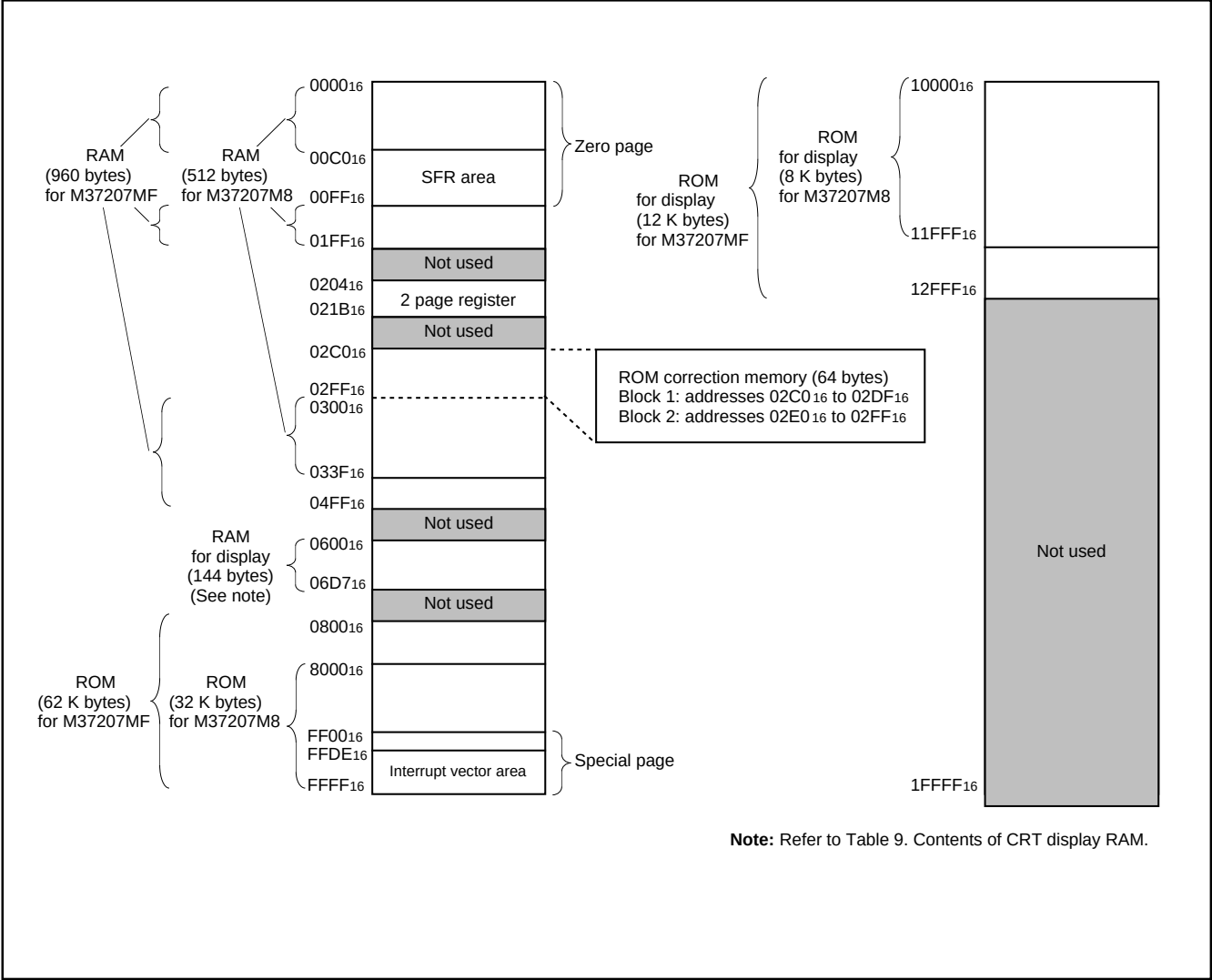
Pin Configuration (TOP VIEW)



M37207MF-XXXSP/FP, M37207M8-XXXSP
 M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 and ON-SCREEN DISPLAY CONTROLLER

Memory Map



M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Memory Map of Special Function Register (SFR)

■SFR Area (addresses C0₁₆ to DF₁₆)

< Bit allocation >

☐ : } Function bit
Name :

☐ : No function bit

☒ 0 : Fix this bit to "0"
(do not write "1")

☒ 1 : Fix this bit to "1"
(do not write "0")

< State immediately after reset >

☐ 0 : "0" immediately after reset

☐ 1 : "1" immediately after reset

☐ ? : Undefined immediately
after reset

Address	Register	Bit allocation	State immediately after reset
		b7	b0
C0 ₁₆	Port P0 (P0)		?
C1 ₁₆	Port P0 direction register (D0)		00 ₁₆
C2 ₁₆	Port P1 (P1)		?
C3 ₁₆	Port P1 direction register (D1)		00 ₁₆
C4 ₁₆	Port P2 (P2)		?
C5 ₁₆	Port P2 direction register (D2)		00 ₁₆
C6 ₁₆	Port P3 (P3)		0 ? ? ? ? ? ? ?
C7 ₁₆	Port P3 direction register (D3)		00 ₁₆
C8 ₁₆	Port P4 (P4)		?
C9 ₁₆	Port P4 direction register (D4)		?
CA ₁₆	Port P5 (P5)		0 ? ? ? ? ? ? ?
CB ₁₆	Port P5 control register (D5)		00 ₁₆
CC ₁₆	Port P6 (P6)		?
CD ₁₆	Port P6 direction register (D6)		00 ₁₆
CE ₁₆	DA-H register (DA-H)		?
CF ₁₆	DA-L register (DA-L)		0 0 ? ? ? ? ? ?
D0 ₁₆	PWM0 register (PWM0)		?
D1 ₁₆	PWM1 register (PWM1)		?
D2 ₁₆	PWM2 register (PWM2)		?
D3 ₁₆	PWM3 register (PWM3)		?
D4 ₁₆	PWM4 register (PWM4)		?
D5 ₁₆	PWM output control register 1 (PW)	PW7 PW6 PW5 PW4 PW3 PW2 PW1 PW0	00 ₁₆
D6 ₁₆	PWM output control register 2 (PN)	PN4 PN3 PN2 PN1 PN0	00 ₁₆
D7 ₁₆	Interrupt interval determination register (??)		?
D8 ₁₆	Interrupt interval determination control register (RE)	RE5 RE4 RE3 RE2 RE1 RE0	00 ₁₆
D9 ₁₆	I ² C data shift register (S0)	D7 D6 D5 D4 D3 D2 D1 D0	?
DA ₁₆	I ² C address register (S0D)	SAD6 SAD5 SAD4 SAD3 SAD2 SAD1 SAD0 RBW	00 ₁₆
DB ₁₆	I ² C status register (S1)	MST TRX BB PIN AL AAS AD0 LRB	0 0 0 1 0 0 0 ?
DC ₁₆	I ² C control register (S1D)	BSEL1 BSEL0 10BIT SAD ALS ESO BC2 BC1 BC0	00 ₁₆
DD ₁₆	I ² C clock control register (S2)	ACK ACK BIT FAST MODE CCR4 CCR3 CCR2 CCR1 CCR0	00 ₁₆
DE ₁₆	Serial I/O mode register (SM)	SM6 SM5 0 SM3 SM2 SM1 SM0	00 ₁₆
DF ₁₆	Serial I/O register (SIO)		?

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

■ SFR Area (addresses E0₁₆ to FF₁₆)

<Bit allocation>

☐	:	Function bit
☐	:	No function bit
☒	:	Fix this bit to "0" (do not write "1")
☒	:	Fix this bit to "1" (do not write "0")

<State immediately after reset>

☐	:	"0" immediately after reset
☐	:	"1" immediately after reset
☐	:	Undefined immediately after reset

Address	Register	Bit allocation	State immediately after reset
		b7 b0	b7 b0
E0 ₁₆	Horizontal register (HR)	☒ HR5 HR4 HR3 HR2 HR1 HR0	00 ₁₆
E1 ₁₆	Vertical register 1 (CV1)	CV16 CV15 CV14 CV13 CV12 CV11 CV10	0 ? ? ? ? ? ? ?
E2 ₁₆	Vertical register 2 (CV2)	CV26 CV25 CV24 CV23 CV22 CV21 CV20	0 ? ? ? ? ? ? ?
E3 ₁₆	Vertical register 3 (CV3)	CV36 CV35 CV34 CV33 CV32 CV31 CV30	0 ? ? ? ? ? ? ?
E4 ₁₆	Character size register (CS)	CS7 CS31 CS30 CS21 CS20 CS11 CS10	0 0 ? ? ? ? ? ?
E5 ₁₆	Border selection register (MD)	MD31 MD30 MD21 MD20 MD11 MD10	0 0 ? ? ? ? ? ?
E6 ₁₆	Color register 0 (CO0)	CO07 CO06 CO05 CO04 CO03 CO02 CO01 CO00	00 ₁₆
E7 ₁₆	Color register 1 (CO1)	CO17 CO16 CO15 CO14 CO13 CO12 CO11 CO10	00 ₁₆
E8 ₁₆	Color register 2 (CO2)	CO27 CO26 CO25 CO24 CO23 CO22 CO21 CO20	00 ₁₆
E9 ₁₆	Color register 3 (CO3)	CO37 CO36 CO35 CO34 CO33 CO32 CO31 CO30	00 ₁₆
EA ₁₆	CRT control register 1 (CC)	☒ CC6 CC5 CC4 CC3 CC2 CC1 CC0	00 ₁₆
EB ₁₆	Display block counter (CBC)		00 ₁₆
EC ₁₆	CRT port control register (CRTP)	B G R I R/G/B VSYNC HSYNC	00 ₁₆
ED ₁₆	Wipe mode register (SL)	SL6 SL5 SL4 SL3 SL2 SL1 SL0	00 ₁₆
EE ₁₆	Wipe start register (??)		00 ₁₆
EF ₁₆	A-D control register 1 (ADM)	ADM4 ADM2 ADM1 ADM0	0 0 0 ? 0 0 0 0
F0 ₁₆	Timer 1 (TM1)		FF ₁₆
F1 ₁₆	Timer 2 (TM2)		07 ₁₆
F2 ₁₆	Timer 3 (TM3)		FF ₁₆
F3 ₁₆	Timer 4 (TM4)		07 ₁₆
F4 ₁₆	Timer mode register 1 (TMR1)	TMR17 TMR16 TMR15 TMR14 TMR13 TMR12 TMR11 TMR10	00 ₁₆
F5 ₁₆	Timer mode register 2 (TMR2)	TMR27 TMR26 TMR25 TMR24 TMR23 TMR22 TMR21 TMR20	00 ₁₆
F6 ₁₆	PWM5 register (PWM5)		?
F7 ₁₆	PWM6 register (PWM6)		?
F8 ₁₆	PWM7 register (PWM7)		?
F9 ₁₆	PWM8 register (PWM8)		?
FA ₁₆	PWM9 register (PWM9)		?
FB ₁₆	CPU mode register (CPUM)	CM7 CM6 CM5 ☒ ☒ CM2 ☒ ☒	0 0 1 1 1 1 0 0
FC ₁₆	Interrupt request register 1 (IREQ1)	IICR VSCR CRTR TM4R TM3R TM2R TM1R	00 ₁₆
FD ₁₆	Interrupt request register 2 (IREQ2)	☒ TM56R MSR S1R IT2R IT1R	00 ₁₆
FE ₁₆	Interrupt control register 1 (ICON1)	IICE VSCE CRTE TM4E TM3E TM2E TM1E	00 ₁₆
FF ₁₆	Interrupt control register 2 (ICON2)	TM56C ☒ TM56E MSE ☒ SIE IT2E IT1E	00 ₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

■SFR Area (addresses 204₁₆ to 21B₁₆)

< Bit allocation >

☐ : } Function bit
Name :

☐ : No function bit

☒ 0 : Fix this bit to "0"
(do not write "1")

☒ 1 : Fix this bit to "1"
(do not write "0")

< State immediately after reset >

☐ 0 : "0" immediately after reset

☐ 1 : "1" immediately after reset

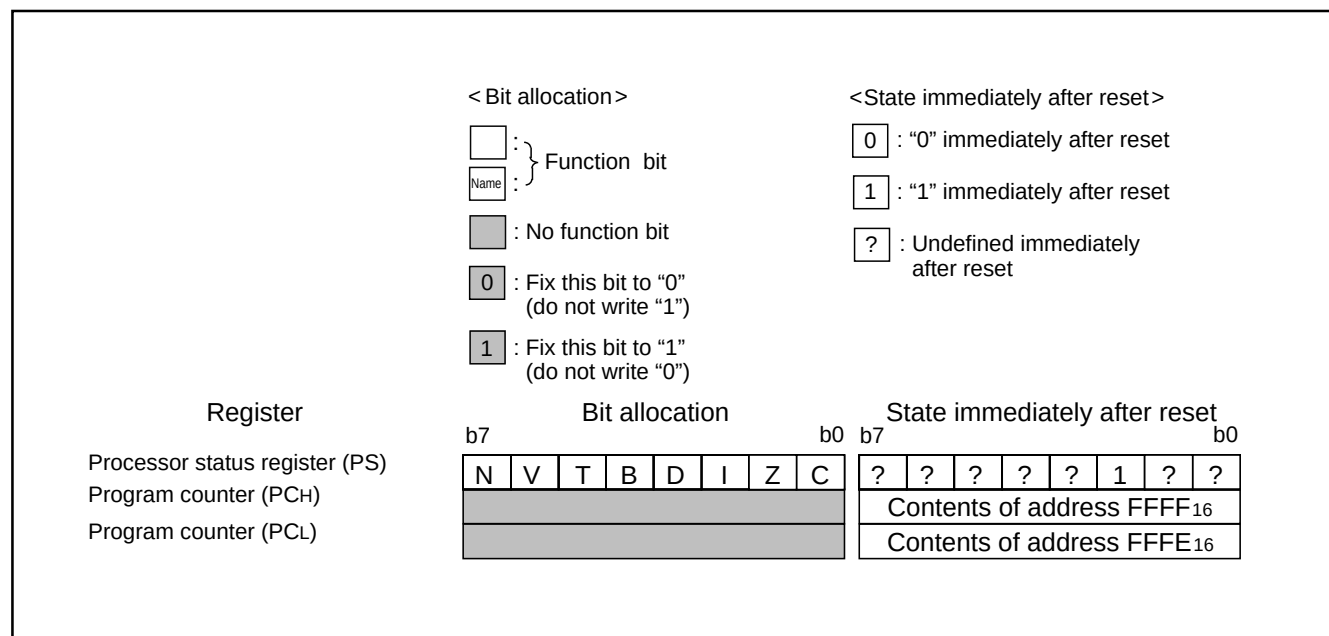
☐ ? : Undefined immediately
after reset

Address	Register	Bit allocation								State immediately after reset							
		b7							b0	b7							b0
204 ₁₆	Timer 5 (T5)									00 ₁₆							
205 ₁₆	Timer 6 (T6)									00 ₁₆							
206 ₁₆	Port control register (P7D)				P7D4		P7D2	P7D1	P7D0	0	0	0	0	0	0	?	?
207 ₁₆	Serial I/O control register (SIC)	SIC7	SIC8	SIC5	SIC4	SIC3	SIC2	SIC1	SIC0	00 ₁₆							
208 ₁₆	CRT control register 2 (CBR)							CBR1	CBR0	00 ₁₆							
209 ₁₆	CRT clock selection register (OP)	0						OP1	OP0	00 ₁₆							
20A ₁₆	A-D control register (ADC)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	0	0	?	?	?	?	?	?
20B ₁₆	Timer mode register (TMR3)								TMR30	00 ₁₆							
20C ₁₆										?							
20D ₁₆										?							
20E ₁₆										?							
20F ₁₆										?							
210 ₁₆										?							
211 ₁₆										?							
212 ₁₆										?							
213 ₁₆										?							
214 ₁₆										?							
215 ₁₆										?							
216 ₁₆										?							
217 ₁₆	ROM correction address 1 (high-order)									00 ₁₆							
218 ₁₆	ROM correction address 1 (low-order)									00 ₁₆							
219 ₁₆	ROM correction address 2 (high-order)									00 ₁₆							
21A ₁₆	ROM correction address 2 (low-order)									00 ₁₆							
21B ₁₆	ROM correction enable register (RCR)					0	0	RC1	RC0	?	?	?	?	0	0	0	0

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Internal State of Processor Status Register and Program Counter at Reset

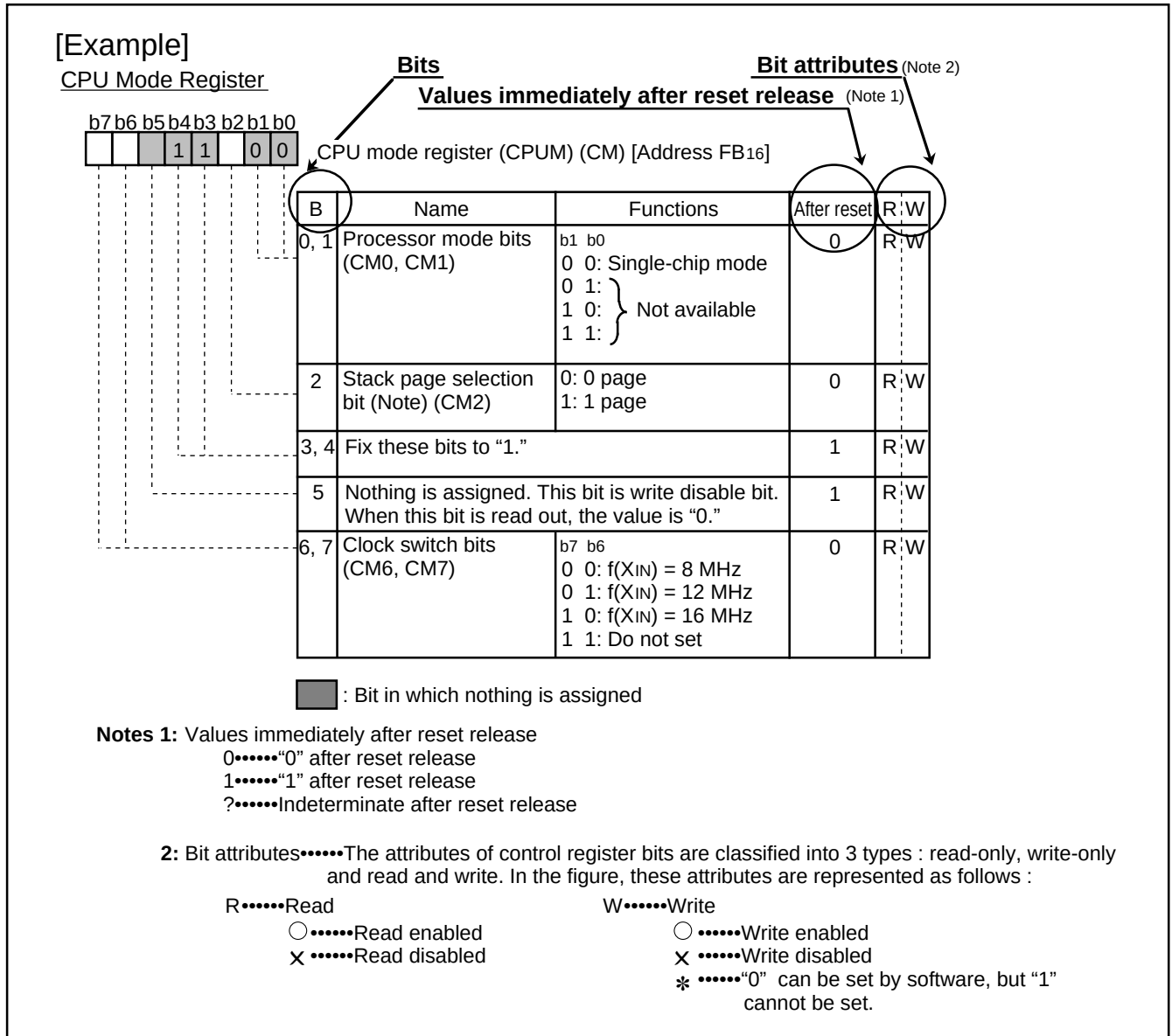


M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

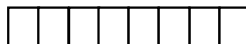


M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Port Pi Direction Register

b7 b6 b5 b4 b3 b2 b1 b0



Port Pi direction register (Di) (i=0,1,2, 6) [Addresses 00C1₁₆, 00C3₁₆, 00C5₁₆, 00CD₁₆]

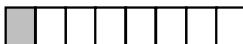
B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port P _{i0} input mode 1 : Port P _{i0} output mode	0	R	W
1		0 : Port P _{i1} input mode 1 : Port P _{i1} output mode	0	R	W
2		0 : Port P _{i2} input mode 1 : Port P _{i2} output mode	0	R	W
3		0 : Port P _{i3} input mode 1 : Port P _{i3} output mode	0	R	W
4		0 : Port P _{i4} input mode 1 : Port P _{i4} output mode	0	R	W
5		0 : Port P _{i5} input mode 1 : Port P _{i5} output mode	0	R	W
6		0 : Port P _{i6} input mode 1 : Port P _{i6} output mode	0	R	W
7		0 : Port P _{i7} input mode 1 : Port P _{i7} output mode	0	R	W

Port Pi Direction Register

Addresses 00C1₁₆, 00C3₁₆, 00C5₁₆, 00CD₁₆

Port P3 Direction Register

b7 b6 b5 b4 b3 b2 b1 b0



Port P3 direction register (D3) [Address 00C7₁₆]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port P ₃₀ input mode 1 : Port P ₃₀ output mode	0	R	W
1		0 : Port P ₃₁ input mode 1 : Port P ₃₁ output mode	0	R	W
2		0 : Port P ₃₂ input mode 1 : Port P ₃₂ output mode	0	R	W
3		0 : Port P ₃₃ input mode 1 : Port P ₃₃ output mode	0	R	W
4		0 : Port P ₃₄ input mode 1 : Port P ₃₄ output mode	0	R	W
5		0 : Port P ₃₅ input mode 1 : Port P ₃₅ output mode	0	R	W
6		0 : Port P ₃₆ input mode 1 : Port P ₃₆ output mode	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Port P3 Direction Register

Address 00C7₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Port P5 Control Register

b7 b6 b5 b4 b3 b2 b1 b0



Port P5 control register (D5) [Address 00CB₁₆]

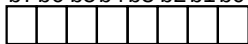
B	Name	Functions	After reset	R	W
0, 1, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
2	Port P5 ₂ output signal selection bit (R)	0 : R signal output 1 : Port P5 ₂ output	0	R	W
3	Port P5 ₃ output signal selection bit (G)	0 : G signal output 1 : Port P5 ₃ output	0	R	W
4	Port P5 ₄ output signal selection bit (B)	0 : B signal output 1 : Port P5 ₄ output	0	R	W
5	Port P5 ₅ output signal selection bit (I)	0 : I/TIM1 OVERFLOW signal output 1 : Port P5 ₅ output	0	R	W
6	Port P5 ₆ output signal selection bit (OUT)	0 : OUT signal output 1 : Port P5 ₆ output	0	R	W

Port P5 Control Register

Address 00CB₁₆

PWM Output Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0



PWM output control register 1 (PW) [Address 00D5₁₆]

B	Name	Functions	After reset	R	W
0	DA, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA/PN4 output selection bit (PW1)	0 : DA output 1 : PN4 output	0	R	W
2	P6 ₀ /PWM0 output selection bit (PW2)	0: P6 ₀ output 1: PWM0 output	0	R	W
3	P6 ₁ /PWM1 output selection bit (PW3)	0: P6 ₁ output 1: PWM1 output	0	R	W
4	P6 ₂ /PWM2 output selection bit (PW4)	0: P6 ₂ output 1: PWM2 output	0	R	W
5	P6 ₃ /PWM3 output selection bit (PW5)	0: P6 ₃ output 1: PWM3 output	0	R	W
6	P6 ₄ /PWM4 output selection bit (PW6)	0: P6 ₄ output 1: PWM4 output	0	R	W
7	P6 ₅ /PWM5 output selection bit (PW7)	0: P6 ₅ output 1: PWM5 output	0	R	W

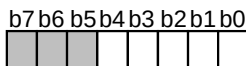
PWM Output Control Register 1

Address 00D5₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

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and ON-SCREEN DISPLAY CONTROLLER

PWM Output Control Register 2



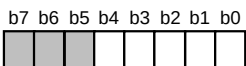
PWM output control register 2 (PN) [Address 00D6₁₆]

B	Name	Functions	After reset	R	W
0	P66/PWM6 output selection bit (PN0)	0 : P66 output 1 : PWM6 output	0	R	W
1	P67/PWM7 output selection bit (PN1)	0 : P67 output 1 : PWM7 output	0	R	W
2	DA output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN4)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA general-purpose output bit (PN5)	0 : Output LOW 1 : Output HIGH	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

PWM Output Control Register

Address 00D6₁₆

Interrupt Interval Determination Control Register



interrupt interval determination control register (RE) [Address 00D8₁₆]

B	Name	Functions	After reset	R	W
0	Interrupt interval determination circuit operation control bit (RE0)	0 : Stopped 1 : Operating	0	R	W
1	Reference clock selection bit (RE1)	0 : 16 μ s 1 : 32 μ s (at $f(X_{IN}) = 8$ MHz)	0	R	W
2	External interrupt input pin selection bit (RE2)	0 : INT1 input 1 : INT2 input	0	R	W
3	INT1 pin input polarity switch bit (RE3)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
4	INT2 pin input polarity switch bit (RE4)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

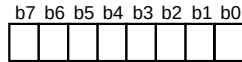
Interrupt Interval Determination Control Register

Address 00D8₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 and ON-SCREEN DISPLAY CONTROLLER

I²C Data Shift Register



I²C data shift register1(S0) [Address 00D9₁₆]

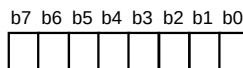
B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

I²C Data Shift Register

Address 00D9₁₆

I²C Address Register



I²C address register (S0D) [Address 00DA₁₆]

B	Name	Functions	After reset	R	W
0	Read/write bit (RBW)	0: Read 1: Write	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	The address data transmitted from the master is compared with the contents of these bits.	0	R	W

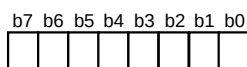
I²C Adress Register

Address 00DA₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

I²C Status Register



I²C status register (S1) [Address 00DB₁₆]

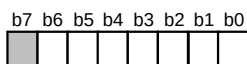
B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1"	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected	0	R	—
4	I ² C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	0	R	—
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave receive mode 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannot be written.

I²C Status Register

Address 00DB₁₆

I²C Control Register



I²C control register (S1D : address 00DC₁₆)

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/receive bits) (BC0 to BC2)	b2 b1 b0 0 0 0 : 8 0 0 1 : 7 0 1 0 : 6 0 1 1 : 5 1 0 0 : 4 1 0 1 : 3 1 1 0 : 2 1 1 1 : 1	0	R	W
3	I ² C-BUS interface use enable bit (ESO)	0 : Disabled 1 : Enabled	0	R	W
4	Data format selection bit (ALS)	0 : Addressing mode 1 : Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0 : 7-bit addressing format 1 : 10-bit addressing format	0	R	W
6, 7	Connection control bits between I ² C-BUS interface and ports	b7 b6 Connection port (See note) 0 0 : None 0 1 : SCL1, SDA1 1 0 : SCL2, SDA2 1 1 : SCL1, SDA1 SCL2, SDA2	0	R	W

Note: When using ports P11-P14 as I²C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

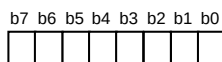
I²C Control Register

Address 00DC₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

I²C Clock Control Register



I²C clock control register (S2 : address 00DD₁₆)

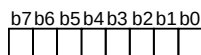
B	Name	Functions		After reset	R : W	
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4-CCR0	Standard clock mode	High speed clock mode	0	R : W
		00 to 02	Setup disabled	Setup disabled		
		03	Setup disabled	333		
		04	Setup disabled	250		
		05	100	400 (See note)		
		06	83.3	166		
		⋮	500/CCR value	1000/CCR value		
		1D	17.2	34.5		
		1E	16.6	33.3		
		1F	16.1	32.3		
(at $\phi = 4$ MHz, unit : kHz)						
5	SCL mode specification bit (FAST MODE)	0 : Standard clock mode 1 : High-speed clock mode		0	R : W	
6	ACK bit (ACK BIT)	0 : ACK is returned. 1 : ACK is not returned.		0	R : W	
7	ACK clock bit (ACK)	0 : No ACK clock 1 : ACK clock		0	R : W	

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
 "0" period : "1" period = 3 : 2
 In the other cases, the duty is as below.
 "0" period : "1" period = 1 : 1

I²C Clock Control Register

Address 00DD₁₆

Serial I/O Mode Register



Serial I/O mode register (SM) [Address 00DE₁₆]

B	Name	Functions	After reset	R	W										
0, 1	Internal synchronous clock selection bits (SM0, SM1) (See note 1)	b1 b0 0 0: f(XIN)/4 or f(XCIN)/4 0 1: f(XIN)/16 or f(XCIN)/16 1 0: f(XIN)/32 or f(XCIN)/32 1 1: f(XIN)/64 or f(XCIN)/64	0	R	W										
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W										
3, 7	Ports P40, P41 function selection bits (SM3, SM7) (See note 2)	b7 b3 <table><tr><td>P40/SOUT2/ SDA3/XCIN</td><td>P41/SCLK2/ SCL3/XCOUT</td></tr><tr><td>X 0</td><td>P40 P41</td></tr><tr><td>0 1</td><td>SOUT2 SCLK2</td></tr><tr><td>1 1</td><td>SDA3 SCL3</td></tr></table>	P40/SOUT2/ SDA3/XCIN	P41/SCLK2/ SCL3/XCOUT	X 0	P40 P41	0 1	SOUT2 SCLK2	1 1	SDA3 SCL3	0	R	W		
P40/SOUT2/ SDA3/XCIN	P41/SCLK2/ SCL3/XCOUT														
X 0	P40 P41														
0 1	SOUT2 SCLK2														
1 1	SDA3 SCL3														
4, 6	Ports P42, P43 function selection bits (SM4, SM6) (See note 2)	b6 b4 <table><tr><td>P42/SIN2/ SDA2/AD8</td><td>P43/SRDY2/ SCL2/AD7</td></tr><tr><td>0 0</td><td>P42 P43</td></tr><tr><td>1 0</td><td>SDA2 SRDY2</td></tr><tr><td>0 1</td><td>P42 SRDY2</td></tr><tr><td>1 1</td><td>SDA2 SDA2</td></tr></table>	P42/SIN2/ SDA2/AD8	P43/SRDY2/ SCL2/AD7	0 0	P42 P43	1 0	SDA2 SRDY2	0 1	P42 SRDY2	1 1	SDA2 SDA2	0	R	W
P42/SIN2/ SDA2/AD8	P43/SRDY2/ SCL2/AD7														
0 0	P42 P43														
1 0	SDA2 SRDY2														
0 1	P42 SRDY2														
1 1	SDA2 SDA2														
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W										

Notes 1: Either $f(X_{IN})$ or $f(X_{CIN})$ is selected by bit 7 of the CPU mode register.

2: When using ports P40–P43 as serial I/O pins, set bit 1 of the serial control register to "1."

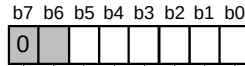
Serial I/O Mode Register

Address 00DE₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Horizontal Position Register



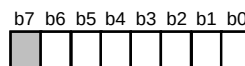
Horizontal position register (HR) [Address 00E0₁₆]

B	Name	Functions	After reset	R	W
0 to 5	Horizontal display start positions (HR0 to HR5)	64 steps (00 ₁₆ to 3F ₁₆)	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
7	Fix this bit to "0."		0	R	W

Horizontal Position Register

Address 00E0₁₆

Vertical Position Register i



Vertical position register i (CVi) (i = 1 to 3) [Addresses 00E1₁₆ to 00E3₁₆]

B	Name	Functions	After reset	R	W
0 to 6	Vertical display start positions (CVi : CVi0 to CVi6)	128 steps (00 ₁₆ to 7F ₁₆)	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

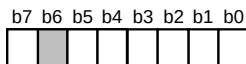
Vertical Position Register i

Addresses 00E1₁₆, 00E3₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Character Size Register



Character size register (CS) [Address 00E4₁₆]

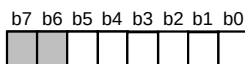
B	Name	Functions	After reset	R	W
0, 1	Character size of block 1 selection bits (CS10, CS11)	b1 b0 0 0 : Minimum size 0 1 : Medium size 1 0 : Large size 1 1 : Extra large size	Indeterminate	R	W
2, 3	Character size of block 2 selection bits (CS20, CS21)	b3 b2 0 0 : Minimum size 0 1 : Medium size 1 0 : Large size 1 1 : Extra large size	Indeterminate	R	W
4, 5	Character size of block 2 selection bits (CS30, CS31)	b5 b4 0 0 : Minimum size 0 1 : Medium size 1 0 : Large size 1 1 : Extra large size	Indeterminate	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
7	OUT signal output switch bit (CS7)	0 : OUT signal output 1 : MUTE signal output (See note)	Indeterminate	R	W

Note: This erases a video signal on an entire screen.

Character Size Register

Address 00E4₁₆

Border Selection Register



Border selection register (MD) [Address 00E5₁₆]

B	Name	Functions	After reset	R	W
0	Block 1 OUT output border selection bit (MD10)	0 : Same output as character output 1 : Border output	Indeterminate	R	W
1	Block 1 OUT output switch bit (MD11)	0 : Border including character 1 : Border only	Indeterminate	R	W
2	Block 2 OUT output border selection bit (MD20)	0 : Same output as character output 1 : Border output	Indeterminate	R	W
3	Block 2 OUT output switch bit (MD21)	0 : Border including character 1 : Border only	Indeterminate	R	W
4	Block 3 OUT output border selection bit (MD30)	0 : Same output as character output 1 : Border output	Indeterminate	R	W
5	Block 3 OUT output switch bit (MD31)	0 : Border including character 1 : Border only	Indeterminate	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

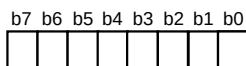
Border Selection Register

Address 00E5₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Color Register n



Color register n (CO0 to CO3) (n = 0 to 3) [Addresses 00E6₁₆ to 00E9₁₆]

B	Name	Functions	After reset	R	W
0	I signal output selection bit (CO _n 0)	0 : No character is output 1 : Character is output	0	R	W
1	B signal output selection bit (CO _n 1)	0 : No character is output 1 : Character is output	0	R	W
2	G signal output selection bit (CO _n 2)	0 : No character is output 1 : Character is output	0	R	W
3	R signal output selection bit (CO _n 3)	0 : No character is output 1 : Character is output	0	R	W
4	B signal output (background) selection bit (CO _n 4)	0 : No background color is output 1 : Background color is output (See notes 1,2)	0	R	W
5	OUT signal output control bit (CO _n 5)	0 : Character is output 1 : Blank is output (See notes 1, 2)	0	R	W
6	G signal output (background) selection bit (CO _n 6)	0 : No background color is output 1 : Background color is output	0	R	W
7	R signal output (background) selection bit (CO _n 7)	0 : No background color is output 1 : Background color is output	0	R	W

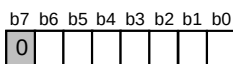
Notes 1: When bit 5 = "0" and bit 4 = "1," there is output same as a character or border output from the OUT pin.

2: When bit 5 = "0" and bit 4 = "0," there is no output from the OUT pin.

Color Register n

Addresses 00E6₁₆, 00E9₁₆

CRT Control Register 1



CRT control register 1 (CC) [Address 00EA₁₆]

B	Name	Functions	After reset	R	W
0	All-blocks display control bit (CC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Block 1 display control bit (CC1)	0 : Block 1 display off 1 : Block 1 display on	0	R	W
2	Block 2 display control bit (CC2)	0 : Block 2 display off 1 : Block 2 display on	0	R	W
3	Block 3 display control bit (CC3)	0 : Block 3 display off 1 : Block 3 display on	0	R	W
4	Block 1 color specification mode switch bit (CC4)	0 : Ordinary mode 1 : 1/2-character unit color specification mode	0	R	W
5	Display oscillation stop bit (CC5)	0 : Oscillation stopped 1 : Oscillation enabled	0	R	W
6	Scanning line double count mode flag(CC6)	0 : Ordinary 256 count mode 1 : Double count mode	0	R	W
7	Fix this bit to "0."		0	R	W

Note: Display is controlled by logical product (AND) between the all-blocks display control bit and each block control bit.

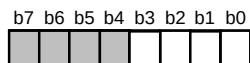
CRT Control Register 1

Address 00EA₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Display Block Counter



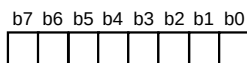
Display block counter (CBC) [Address 00EB₁₆]

B	Name	Functions	After reset	R	W
0 to 3	Number of blocks which are being displayed or has displayed (Incremented each time a block is displayed)		Indeterminate	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Display Block Counter

Address 00EB₁₆

CRT Port Control Register



CRT port control register (CRTP) [Address 00EC₁₆]

B	Name	Functions	After reset	R	W
0	H _{SYNC} input polarity switch bit (H _{SYC})	0 : Positive polarity 1 : Negative polarity	0	R	W
1	V _{SYNC} input polarity switch bit (V _{SYC})	0 : Positive polarity 1 : Negative polarity	0	R	W
2	R, G, B output polarity switch bit (R/G/B)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	I output polarity switch bit (I)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	OUT output polarity switch bit (OUT)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	R signal output switch bit (R)	0 : R signal output 1 : MUTE signal output	0	R	W
6	G signal output switch bit (G)	0 : G signal output 1 : MUTE signal output	0	R	W
7	B signal output switch bit (B)	0 : B signal output 1 : MUTE signal output	0	R	W

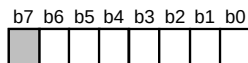
CRT Port Control Register

Address 00EC₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Wipe Mode Register



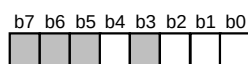
Wipe mode register (SL) [Address 00ED₁₆]

B	Name	Functions	After reset	R	W
0, 1	Wipe mode selection bits (SL0, SL1)	b1 b0 0 0 : Wipe is not available 0 1 : Mode 1 1 0 : Mode 2 1 1 : Mode 3	0	R	W
2	Direction mode selection bits (SL2)	0: DOWN mode 1: UP mode	0	R	W
3, 4	Wipe unit selection bits (SL3, SL4)	b4 b3 0 0 : 1H unit 0 1 : 2H unit 1 0 : 3H unit 1 1 : Do not set	0	R	W
5, 6	Stop mode selection bits (SL5, SL6)	b6 b5 0 0 : Stop at the 312nd H 0 1 : Stop at the 156th H 1 0 : Stop at the 256th H 1 1 : Stop at the 128th H	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		0	R	—

Wipe Mode Register

Address 00ED₁₆

A-D Control Register 1



A-D control register 1 (ADM) [Address 00EF₁₆]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADM0 to ADM2)	b2 b1 b0 0 0 0 : AD1 0 0 1 : AD2 0 1 0 : AD3 0 1 1 : AD4 1 0 0 : AD5 1 0 1 : AD6 1 1 0 : AD7 1 1 1 : AD8	0	R	W
3, 5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	—

A-D Control Register 1

Address 00EF₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Timer Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 1 (TMR1) [Address 00F4₁₆]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TMR10, TMR15)	b5 b0 0 0: f(X _{IN})/16 or f(X _{CIN})/16 (See note) 0 1: f(X _{IN})/4096 or f(X _{CIN})/4096 (See note) 1 0: f(X _{CIN}) 1 1: External clock from TIM2 pin	0	R	W
1	Timer 2 count source selection bit 1 (TMR11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TMR12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TMR13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TMR14)	0: f(X _{IN})/16 or f(X _{CIN})/16 (See note) 1: Timer 1 overflow	0	R	W
6	Timer 5 count source selection bit 2 (TMR16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 internal count source selection bit (TMR17)	0: f(X _{IN})/16 or f(X _{CIN})/16 (See note) 1: Timer 5 overflow	0	R	W

Note: Either f(X_{IN}) or f(X_{CIN}) is selected by bit 7 of the CPU mode register.

Timer Mode Register 1

Address 00F4₁₆

Timer Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 2 (TMR2) [Address 00F5₁₆]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TMR20)	0: f(X _{IN})/16 or f(X _{CIN})/16 (See note) 1: External clock from TIM3 pin	0	R	W
1	Timer 4 count source selection bit 2 (TMR21)	0: Timer 3 overflow signal 1: f(X _{IN})/16 or f(X _{CIN})/16 (See note)	0	R	W
2	Timer 3 count stop bit (TMR22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TMR23)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit 1 (TMR24)	0: Count source selected by bit 1 of TMR2 1: f(X _{IN})/2 or f(X _{CIN})/2 (See note)	0	R	W
5	Timer 5 count stop bit (TMR25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TMR26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TMR27)	0: Count source selected by bit 0 of TMR3 1: Count source selected by bit 6 of TMR1	0	R	W

Note: Either f(X_{IN}) or f(X_{CIN}) is selected by bit 7 of the CPU mode register.

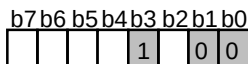
Timer Mode Register 2

Address 00F5₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0


CPU mode register (CPUM) (CM) [Address 00FB₁₆]

B	Name	Functions	After reset	R/W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R/W
2	Stack page selection bit (CM2) (See note 1)	0: 0 page 1: 1 page	1	R/W
3	Fix these bits to "1."		1	R/W
4	Internal system clock output selection bit (CM4) (See note 2)	0: Output is stopped 1: Internal system clock ϕ output	1	R/W
5	XCOUNT drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R/W
6	Main Clock (XIN-XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R/W
7	Internal system clock selection bit (CM7)	0: XIN-XOUT selected (high-speed mode) 1: XCIN-XCOUT selected (high-speed mode)	0	R/W

Notes 1: This bit is set to "1" after the reset release.
 2: The internal system clock ϕ stops at HIGH.

CPU Mode Register

Address 00FB₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	CRT interrupt request bit (CRTR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Vsync interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Multi-master I ² C-BUS interface interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Interrupt Request Register 1

Address 00FC16

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (IT1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	INT2 interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (SIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3,6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

*: "0" can be set by software, but "1" cannot be set.

Interrupt Request Register 2

Address 00FD16

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address 00FE₁₆]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	CRT interrupt enable bit (CRTE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VS _{SYNC} interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Multi-master I ² C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Interrupt Control Register 1

Address 00FE₁₆

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2 (ICON2) [Address 00FF₁₆]

B	Name	Functions	After reset	R	W
0	INT1 interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3, 6	Fix these bits to "0."		0	R	W
4	f(X _{IN})/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56C)	0 : Timer 5 1 : Timer 6	0	R	W

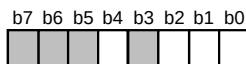
Interrupt Control Register 2

Address 00FF₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

Port Control Register



Port control register (P7D) [Address 0206₁₆]

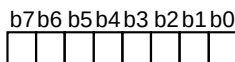
B	Name	Functions	After reset	R	W
0, 1	Port P7 data input bits (P7D0, P7D1)	When only OP1 = "0" and OP0 = "1," input data is valid. (See note)	Indeterminate	R	W
2	D-A/AD3 function selection bit (P7D2)	0: AD3 1: D-A	0	R	W
3, 5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		0	R	—
4	P40/XCIN, P41/XCOUT function selection bit (P7D4)	0 : P40, P41 1 : XCIN, XCOUT	0	R	W

Note: OP is the CRT clock selection register.

Port Control Register

Address 0206₁₆

Serial I/O Control Register



Serial I/O control register (SIC) [Address 0207₁₆]

B	Name	Functions	After reset	R	W																
0	Input signal to sift register selection bit (SIC0)	CSIO b0 0 0: Input signal from S _{IN1} 0 1: Input signal from S _{OUT1} (See note 1) 1 0: Input signal from S _{IN2} 1 1: Input signal from S _{OUT2} (See note 1)	0	R	W																
1	Serial I/O pin switch bit (CSIO)	0: S _{OUT1} , S _{CLK1} , S _{IN1} , $\overline{\text{SRDY1}}$ 1: S _{OUT2} , S _{CLK2} , S _{IN2} , $\overline{\text{SRDY2}}$	0	R	W																
2	I ² C-BUS connection ports switch bit (SIC2)	0: SDA2, SCL2, SDA1, SCL1 1: SDA3, SCL3	0	R	W																
3, 7	Ports P47 function selection bits (SM3, SM7) (See note 2)	<table><tr><td>b7</td><td>b3</td><td colspan="2">P47/$\overline{\text{SRDY1}}$/PWM8</td></tr><tr><td>0</td><td>X</td><td colspan="2">P47</td></tr><tr><td>1</td><td>0</td><td colspan="2">$\overline{\text{SRDY1}}$</td></tr><tr><td>1</td><td>1</td><td colspan="2">PWM8</td></tr></table>	b7	b3	P47/ $\overline{\text{SRDY1}}$ /PWM8		0	X	P47		1	0	$\overline{\text{SRDY1}}$		1	1	PWM8		0	R	W
b7	b3	P47/ $\overline{\text{SRDY1}}$ /PWM8																			
0	X	P47																			
1	0	$\overline{\text{SRDY1}}$																			
1	1	PWM8																			
4, 5	Ports P44, P45 function selection bits (SM4, SM6) (See note 2)	<table><tr><td>b5</td><td>b4</td><td>P44/S_{OUT1}/SDA1</td><td>P45/S_{CLK1}/SCL1</td></tr><tr><td>0</td><td>X</td><td>P44</td><td>P45</td></tr><tr><td>1</td><td>0</td><td>S_{OUT1}</td><td>S_{CLK1}</td></tr><tr><td>1</td><td>1</td><td>SDA1</td><td>SCL1</td></tr></table>	b5	b4	P44/S _{OUT1} /SDA1	P45/S _{CLK1} /SCL1	0	X	P44	P45	1	0	S _{OUT1}	S _{CLK1}	1	1	SDA1	SCL1	0	R	W
b5	b4	P44/S _{OUT1} /SDA1	P45/S _{CLK1} /SCL1																		
0	X	P44	P45																		
1	0	S _{OUT1}	S _{CLK1}																		
1	1	SDA1	SCL1																		
6	Ports P46 function selection bits (SIC6) (See note 2)	<table><tr><td>b6</td><td colspan="3">P46/S_{IN1}/PWM9</td></tr><tr><td>0</td><td colspan="3">P46</td></tr><tr><td>1</td><td colspan="3">PWM9</td></tr></table>	b6	P46/S _{IN1} /PWM9			0	P46			1	PWM9			0	R	W				
b6	P46/S _{IN1} /PWM9																				
0	P46																				
1	PWM9																				

Notes 1: When inputting data from the S_{out} pin, set "FF₁₆" to the serial I/O register.

2: When using ports P44–P47 as serial I/O pins, set bit 1 of the serial I/O control register to "0."

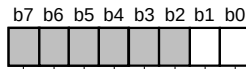
Serial I/O Control Register

Address 0207₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

CRT Control Register 2



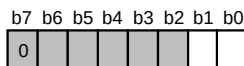
CRT control register 2 (CBR) [Address 0208₁₆]

B	Name	Functions	After reset	R	W
0	I signal output switch bit (CBR0)	0: I signal output 1: MUTE signal output	0	R	W
1	I/TIM1 function switch bit (CBR1)	0: I output or MUTE output 1: 1/2 clock output of timer 1	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		0	R	—

CRT Control Register 2

Address 0208₁₆

CRT Clock Selection Register



CRT clock selection register (OP) [Address 0209₁₆]

B	Name	Functions	After reset	R	W
0, 1	CRT clock selection bits (OP0, OP1)	b1 b0 Functions	0	R	W
		1 0 The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.			
		0 1 Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports P7 ₀ and P7 ₁ respectively.			
		1 0 Do not set.			
2 to 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
7	Fix this bits to "0."		0	R	W

Notes 1: It is necessary to connect other ceramic resonator or quartz-crystal oscillator across the pins X_{IN} and X_{OUT}.
2: CC6 is the scanning line double count mode flag.

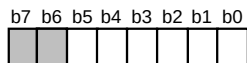
CRT Clock Selection Register

Address 0209₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

A-D Control Register 2



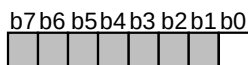
A-D control register 2(ADC) [Address 020A₁₆]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC0 to ADC5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc : 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	Indeterminate	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

A-D Control Register 2

Address 020A₁₆

Timer Mode Register 3



Timer mode register 3 (TMR3) [Address 020B₁₆]

B	Name	Functions	After reset	R	W
0	Timer 5 count source selection bit 3 (TMR30)	0 : f(X _{IN})/16 or f(X _{CIN})/16 (See note) 1 : f(X _{CIN})	0	R	W
1 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Note: Either f(X_{IN}) or f(X_{CIN}) is selected by bit 7 of the CPU mode register.

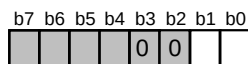
Timer Mode Register 3

Address 020B₁₆

M37207MF-XXXSP/FP, M37207M8-XXXSP M37207EFSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
and ON-SCREEN DISPLAY CONTROLLER

ROM Correction Enable Register



ROM correction enable register (RCR) [Address 021B₁₆]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RC0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RC1)	0: Disabled 1: Enabled	0	R	W
2, 3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

ROM Correction Enable Register

Address 021B₁₆

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REVISION DESCRIPTION LIST	M37207MF-XXXSP/FP, M37207M8-XXXSP, M37207EFSP/FP DATA SHEET
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Rev. No.	Revision Description	Rev. date
1.0	First Edition	971212
1.1	Correct note (P76)	980731