Instantly Available PCI Card Power Management

Introduction

Today, PCs need to remain constantly connected to the outside world, but at the same time consume minimum power. Even when looking "idle", it is still possible to receive a message from the Internet or an incoming fax or phone call. The PC must automatically go from "sleep" mode to "on" mode; in other words, an "Instantly Available" PC (IAPC). The challenge is to maintain a system's modem or Local Area Network (LAN) connectivity on a desktop PC/workstation while at the same time minimizing power consumption. These power management features are called Wake-on-Ring (or Wake-on-Modem), Wake-on-LAN, and Wake-on-PME (Power Management Event).

The main qualities/benefits of such a system are:

- Listening: available anytime to receive messages from the outside world, and
- Reacting: responding anytime to do a specific operation (maintenance…), and
- Saving energy and being silent in the idle mode.

The "OnNow" initiative by Microsoft® defined the new requirements for the system that affect both software and hardware aspects of the PC: Windows® operating system, applications, device drivers, and hardware within the system. All these elements must work together in order to provide a fully transparent power management system. This note will focus only on the hardware aspects.

ACPI System Design

An instantly available PC appears to be "off", yet it can snap back to its full ready state within seconds and respond to the phone ringing in time to service the call.

In order to meet these requirements a recommendation, the Advanced Configuration and Power Interface specification (ACPI), has been defined by Intel®, Microsoft®, and Toshiba®.

Instantly available motherboards include: ACPI BIOS, ACPI chip set, and PCI slots that are compliant to the PCI-PM specification. The Intel chip set supports the power management features to define the ACPI sleep states and also generates the signals to control power planes to turn the main power supplies on and off.

The implementation includes multiple power sources and uses separate power planes in the system. Each power source is selected depending on the required state demanded by the system, and one of the major requirements is to switch between power sources continuously, automatically, and without interruption.

The "sleep" state of an instantly available PC is called "Suspend to RAM". This is implemented by using:

- split power planes in the system design, and
- an auxiliary power source (V_{AUX}) for dual mode power distribution.

Let's focus on the PCI (Peripheral Component Interface) cards, where California Micro Device's products have their primary applications. By definition, all PCI add-on cards are connected to the motherboard through the PCI bus. On the PCI connector, several pins have been reserved in order to support the instantly available functionality.

- PME# (Power Management Event) pin (pin #A19) is used to wake the system in response to a PCI power management wake event such as the phone ringing.
- 3.3Vaux pin (pin #A14) is used to deliver the auxiliary power of 3.3V to all the wake-up PCI cards in the system. This power is always available to keep the card active even when the rest of the PCI bus is without power.

Three different independent voltage sources are now available on the PCI bus: $3.3V_{AUX}$, $3.3V_{CC}$, and $5V_{CC}$. In a power plane partitioning system of an instantly available PC, the $3.3V_{AUX}$ is electrically isolated from the main PCI 3.3V rail at all times. During normal operation, the $3.3V_{AUX}$ supply remains on all the time, while the other main supplies, $3.3V_{CC}$ and $5V_{CC}$, can be switched on and off as needed.

PCI Adapter Card Application

PCI Network Interface Cards (NIC) and modem cards are also designed with split power planes. Thus, they are able to operate in sleep mode with only the Vaux power supply and still be able to wake-up the system.

Some NICs that operate in "Wake on LAN" mode get a 5V standby through a cable that connects directly to a specific header on the motherboard.

Chip Set Voltage

Today, PCI card chip sets or ASICs operate at a low voltage of 3.3V. That allows much lower power consumption than with the previous 5V modem chips. However "older" PCs are still operating at 5V and do not have any $3.3V_{AUX}$ supply. "New" PCI cards must be compatible with these systems still in service, and therefore must regulate on board their own 3.3V supply from the 5V. This is made possible by using California Micro Devices' SmartOR™ power management products: the CMPWR100 and CMPWR150. In addition, there is a maximum current limitation of 375mA on the $3.3V_{AUX}$.

Power Requirements on V_{AUX}

In order to limit the power consumed by the system in the "sleep" mode, each PCI card must reduce its current consumption from the auxiliary power supply. The power operating conditions are displayed below.

Parameter	Description	MIN	TYP	MAX	UNIT
3.3 V_{AUX}	Powered by dual power circuit	3.0	3.3	3.6	Volts
Imax_enabled	Sleep state wake up enabled			375	mA
Imax_disabled	Sleep state wake up disabled			20	mA

Table 1. Power Requirements for V_{AUX}

That means that each PCI add-in card's load on $3.3V_{AUX}$ must not exceed 375mA. When the board is in a sleep state with wake up event generation disabled, it must reduce its total slot current to less than 20mA which can be done several ways:

- internally disabling as much logic as possible on the board, or
- electrically isolating the $3.3V_{AUX}$ pin from the auxiliary power plane of the board.

Dual Power Supply

A dual mode power supply is able to deliver the same reference voltage from two separate tuned (load-wise) power sources. For example, a main power source will provide a high capacity, high efficiency 3.3V source for heavy "runtime" loads, and a lower capacity auxiliary source, yet reasonably efficient, 3.3V source for lightly loaded "sleeping" states. A voltage switch is required in order to select between one of these two different sources. This can be implemented with discrete Schottky diodes, or more efficiently, with California Micro Devices' power switch, the CMPWR025.

California Micro Devices has developed a family of SmartOR™ Power Management devices to address all these requirements whose characteristics are summarized in Table 2 and will be the primary focus of this application note.

Device	Function	V_{IN} [V]	V_{OUT} [V]	I_{OUT} [mA]	Package
CMPWR100	Regulator and Switch from V_{AUX} to V_{OUT}	4.5 to 5.5	3.3 or V_{AUX}	≤ 200	8-pin SOIC
CMPWR150	Regulator	4.5 to 5.5	3.3 or V_{AUX}	≤ 500	5-pin TO-263 8-pin SOIC
CMPWR025	Dual Input Switch	2.8 to 5.5	V_{CC1} or V_{CC2}	≤ 500	8-pin SOIC 8-pin MSOP

Table 2. Summary of Power Management Devices

All these parts are general purpose smart voltage regulators and/or switches. They can be used in PCI modem, PCI LAN card, or dual power system applications.

Figures 1-3 below illustrate a simplified block diagram of each of the power management devices.

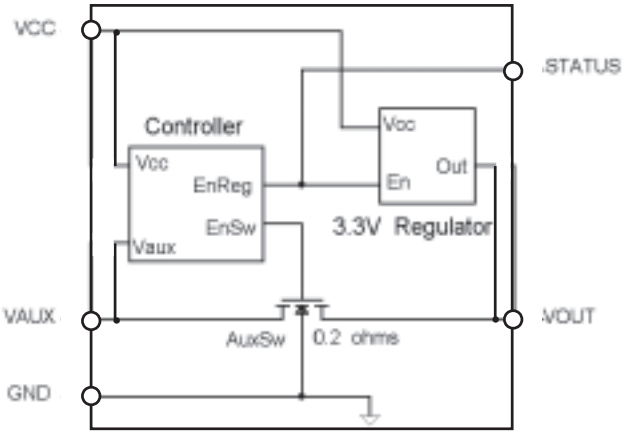


Figure 1. CM PWR-100 Block Diagram

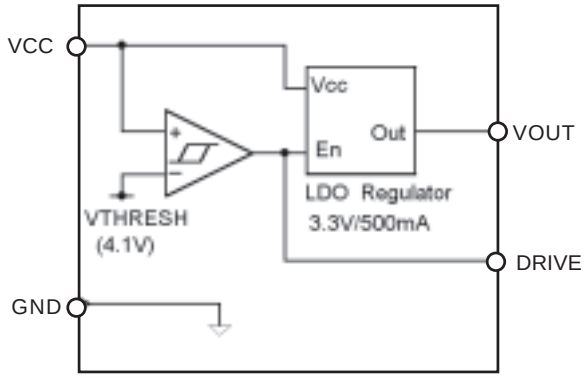


Figure 2. CM PWR-150 Block Diagram

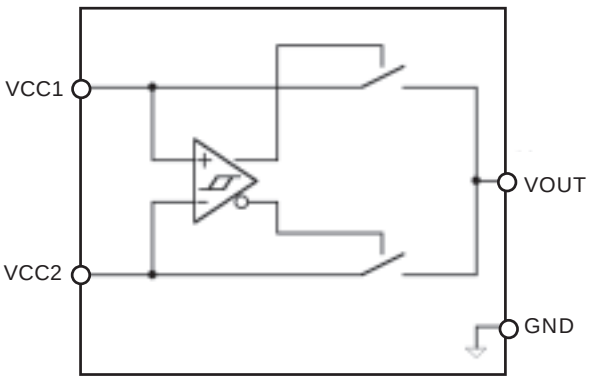


Figure 3. CMPWR025 Block Diagram

In the next sections, we will discuss specific applications for the CMPWR100 and CMPWR150. In order to facilitate the design process, California Micro Devices has available a SmartOR™ evaluation board for use in the lab and to facilitate PCB layout.

Hysteresis

Hysteresis is illustrated in Figure 4 and is defined as the difference between the enabling threshold (when the regulator turns on) and the disabling threshold (when the regulator turns off). The hysteresis level sets up the maximum level of acceptable noise or disturbance on V_{CC} or V_{AUX}. This is particularly critical during power transitions.

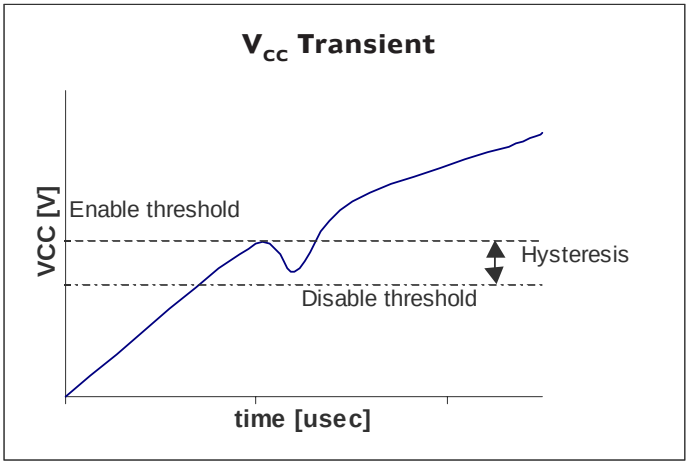


Figure 4. Input voltage transient and hysteresis

As shown in Figure 5, the voltage seen by the device is given by:

$$V_{cc\_in} = V_{cc} - (R_s \times I) - (R_t \times I) - (L_t \times dI/dt)$$

where, V_{cc} is the power supply voltage,
R_s is the power supply output impedance,
R_t is the interconnect series resistance (between supply and regulator), and
L_t is the trace (line) inductance (between supply and regulator).

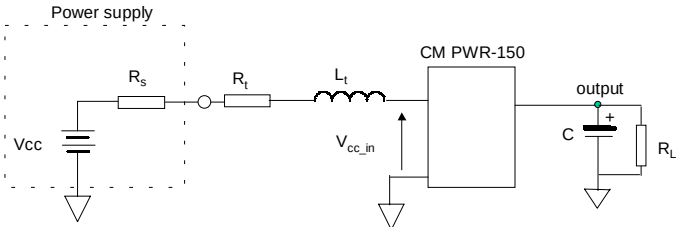


Figure 5. Equivalent circuit with line parasitic

Assuming an ideal situation where there is no parasitic inductance, the hysteresis level should follow the equation below.

$$V_{hysteresis} > (R_s \times I) + (R_t \times I)$$

Where R_s is the power supply output impedance and R_t is the interconnect series resistance (between supply and regulator).

In order to avoid disturbance and given the hysteresis of the devices, the recommended maximum total resistance is shown in Table 3.

Device	Hysteresis [mV]	Imax [mA]	Resistance [Ω]
CMPWR100	150	200	0.75
CMPWR150	250	500	0.5
CMPWR025	50 or 100	500	0.1 or 0.2

Table 3. Recommended maximum series resistances during turn off to prevent chatter

The worst case condition occurs during turn on, when there is in-rush current. During turn on, the current is rising from 0A to a high in-rush current. The in-rush current level and duration is increased when the initial output capacitor voltage is 0V, and when the capacitor value is larger. We can assume an in-rush current equal to twice the maximum DC load current of the device. Table 4 below gives a recommendation for the maximum series resistances during turn on.

Device	Hysteresis [mV]	In-rush Imax [mA]	Resistance [Ω]
CMPWR100	150	400	0.375
CMPWR150	250	1000	0.25
CMPWR025	50 or 100	1000	0.05 or 0.1

Table 4. Recommended maximum series resistances during turn on to prevent chatter

Although a filter capacitor at the input can reduce the effective source impedance for short transients, long in-rush current durations may still cause chatter.

CMPWR100 POWER MANAGEMENT APPLICATION

Device Operation

The CMPWR100 is a power management device able to generate a continuous 3.3V at 200mA from two voltage sources: a 5V main supply (V_{CC}) or a 3.3V auxiliary supply (V_{AUX}). The device integrates a low dropout voltage regulator, an integrated low impedance switch, and control circuitry to switch from the V_{CC} to V_{AUX} supply. When the 5V is present, the device automatically enables the regulator that produces 3.3V output at V_{OUT}. When only the 3.3V is present, the device provides a direct connection from the V_{AUX} pin to the V_{OUT} pin with a very low impedance of 0.2Ω typically. This will minimize power consumption when in "sleep" mode. The worst case is when a maximum current of 200mA is flowing which results in a power dissipation (loss) across the switch of only 8mW.

The CMPWR100 gives priority to the primary input V_{CC} over the secondary input V_{AUX}. It also provides an internal reference voltage at 4.1V used to set the threshold. When the primary V_{CC} drops below this threshold, V_{AUX} becomes the selected input source. To prevent chatter, the threshold logic has a built-in hysteresis of 150mV, and the primary source is only selected again when the V_{CC} level exceeds 4.25V typically.

All control circuitry needed to provide a smooth and automatic transition between supplies has been incorporated, allowing the V_{CC} to be dynamically switched without loss of output voltage. A STATUS output pin is used to indicate an acceptable V_{CC} level. Internal circuitry guarantees that high isolation is maintained between both supplies under all operating conditions.

Typical Applications

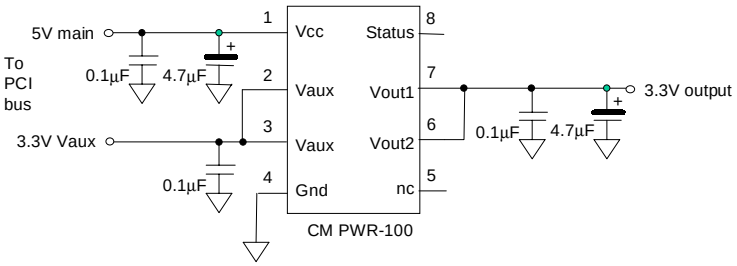


Figure 6. Dual Input Power Management Circuit

In a PCI modem application, regulator is used to provide backward compatibility for 3.3V modems with "older" systems where only 5V is provided on the PCI bus. The CMPWR100 is used to generate the 3.3V on board from a 5V source. The two Vaux input pins must be connected together to the 3.3Vaux provided on new systems.

In order to maintain regulator stability and minimize disturbance on power supplies during change over between input sources, an external 4.7µF capacitor is required between the output and ground. The external capacitor provides the necessary filtering to minimize transients during supply change over and ensures regulator stability. Most Tantalum type capacitors are recommended. But the capacitor should have a low ESR (Equivalent Series Resistance). The value of the capacitor may be increased to minimize switch over transients.

A bypass capacitor in the range of 1µF to 10µF may be connected between VCC and ground in order to filter out voltage transients. This is recommended for longer PCB trace connections between the input and the power supply, inducing large series resistance.

As stated earlier, the STATUS pin may be used to indicate the state of the regulator. It is active "High" when the regulator is turned on ($V_{CC} > V_{THRES}$), and may be used to drive the gate of an external P-channel MOSFET switch in parallel with the integrated PMOS switch for Vaux. This will provide an even lower "ON" resistance between Vaux and Vout, thus lowering power dissipation further. To be efficient, the external switch should have an on-resistance of less than 400mΩ at V_{GS} = 3V and I_D =0.2A.

CMPWR150 POWER REGULATOR APPLICATION

Device Operation

The CMPWR150 employs a circuit topology similar to the CMPWR100, but utilizes an external P-channel MOSFET to switch Vaux at current levels up to 375mA. The CMPWR150 is designed to regulate up to 500mA of continuous output current when operating from V_{CC}. The external switch handles all the V_{AUX} requirements. The CMPWR150 exceeds the PCI-defined maximum 375mA load capability.

All control circuitry needed to provide a smooth and automatic transition between supplies has been incorporated. This offers trouble-free transitions between input voltages, or between sleep and wake-up modes. Internal circuitry guarantees that high isolation is maintained between the V_{CC} supply and the output under all operating conditions. The V_{CC} to V_{AUX} isolation is achieved by disabling the external PFET when the regulator is enabled. The V_{OUT} to V_{CC} isolation is achieved by forcing the regulator pass transistor to be disabled.

The V_{CC} input is compared to a 4.1V internal threshold level. Whenever V_{CC} drops below that level, the regulator is disabled and the DRIVE output is enabled (active low). The DRIVE output is used to control an external P-channel MOSFET switch for connecting an auxiliary 3.3V voltage source to the load. When the regulator is enabled, the DRIVE output is set to V_{CC}.

1. The P-channel MOSFET must have a low "on" resistance at low voltage:

1. The P-channel MOSFET must have a low "on" resistance at low voltage:

   $V_{AUX} - (R_{DS(ON)} \times I_{Dmax}) > V_{OUTmin}$

   Typically, $R_{DS(ON)}$ must be less than 200mΩ at V_{GS} = 3V and I_D = 375mA.
   A typical 75mV voltage drop across the switch is applicable for most cases.

2. The MOSFET must typically have a gate threshold voltage of 1V.
   We recommend the Vishay Siliconix Si2301DS, Fairchild FDN338P, or equivalent.

Typical Applications

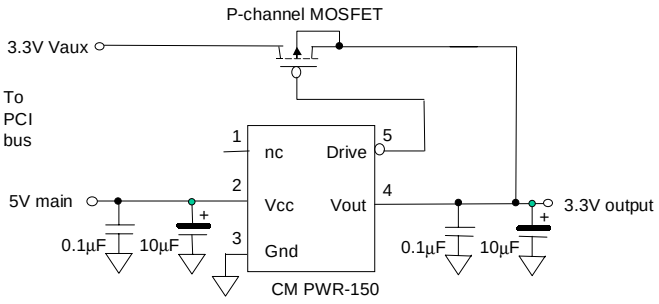


Figure 7. Power Regulator Circuit

"Cold-Start" Behavior

A "cold-start" situation occurs when a PC is powered ON. Typically, power supplies take milliseconds to reach their nominal voltage. Both the 5V and 3.3V voltage sources are ramping up together. As soon as the 5V source reaches the *regulator_enable* 4.25V threshold, the regulator turns ON. At that time the output capacitor begins to rapidly charge and pulls a large transient current which can easily exceed values of 1 ampere. It is, therefore, very important to take into consideration the parasitic series resistances and parasitic inductance between the supply voltage V_{cc} and the device. The voltage seen by the device is given by:

$$V_{CCIN} = V_{CC} - (R_s \times I) - (R_t \times I) - (L_t \times d_I / d_t)$$

where, V_{cc} is the power supply voltage,
R_s is the power supply output impedance,
R_t is the interconnect series resistance (between supply and the CMPWR150), and
L_t is the trace (line) inductance (between supply and the CMPWR150).

Clearly a large, rapidly changing current will create a significant change in $V_{cc\ in}$, and if the input level drops below the *regulator_disable* 4.1V threshold, the regulator will turn OFF. The input level will then start to rise back toward 5V, turning the regulator back ON. This results in an unstable state (motor boating) where the regulator turns on and off until the output capacitor is finally charged to the 3.3V level.

Input Capacitor

To minimize the unstable state effect, an input capacitor is required in close proximity to the V_{CC} input pin. When a transition occurs from V_{AUX} to V_{CC}, the capacitor is used as a charge reservoir to provide current to the load as well. This is especially critical when the output capacitor is not yet charged at power-up, or when the output level is much lower than 3.3V. In this case, the device will go into current limiting until VOUT goes back to its nominal level. A large Tantalum capacitor of 10µF or greater is recommended.

Output Capacitor

During power transitions, a previously charged capacitor will provide the current to the load until the regulator or the auxiliary supply take over. A larger Tantalum capacitor at the output will improve this transition, and a value of 10µF or greater is recommended.

High Frequency Capacitors

Additionally ceramic chip capacitors can be placed next to both inputs and output pins to reduce the high frequency noise. A value of 0.1µF is recommended.

Supply Transient Characteristics

A resistive load of 6.8Ω is used, setting a load current of 485mA at 3.3V.

V_{CC} power-up 0V to 5V (cold-start) with V_{AUX} open circuit

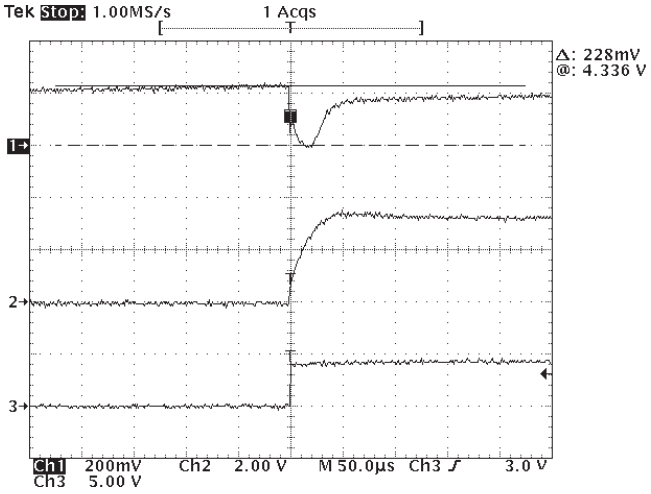
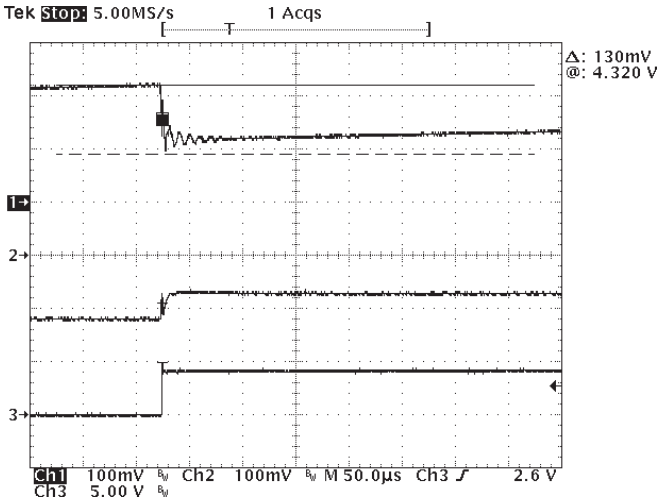


Figure 8

Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}
Ch3: DRIVE

Figure 8 shows V_{CC} approaching the enable threshold during a 0V to 5V initial power-up transition (or cold-start). V_{AUX} is left open. When V_{CC} reaches the 4.3V enable threshold, the regulator turns ON. The large in-rush current caused by the uncharged output capacitor generates a voltage drop of about 230mV on the V_{CC} pin. The 250mV hysteresis ensures the regulator remains enabled during the transient.

V_{CC} power-up with V_{AUX}=3.3V

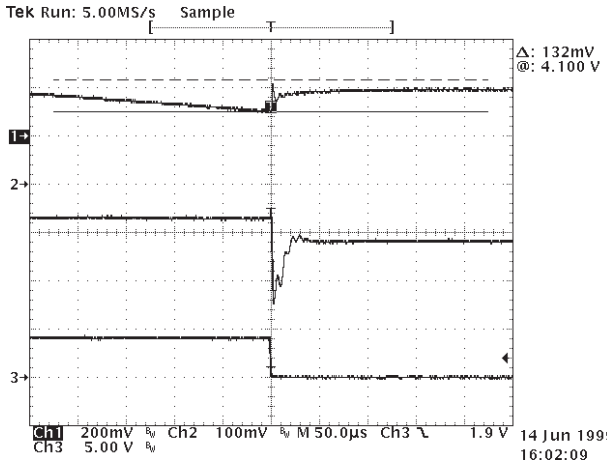


Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}, offset 3.3V
Ch3: DRIVE

Figure 9

Figure 9 shows V_{CC} approaching the enable threshold during a 0V to 5V transition. V_{AUX} is set to 3.3V DC. In this case, the output capacitor is already set to 3.3V, so that when the regulator turns ON, the in-rush current is minimized. The transition on V_{OUT} is clean. The test set-up series resistance on the V_{CC} input is estimated at about 160mΩ. At full load, the output voltage is above 3.2V.

V_{CC} power-down with V_{AUX}=3.3V

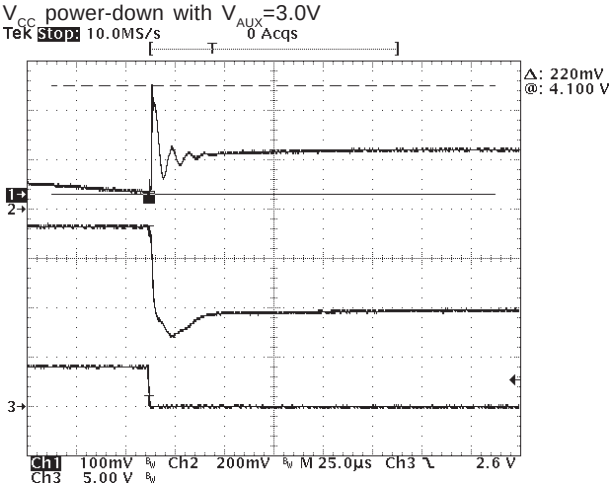


Ch1: V_{CC}, offset 4.0V
Ch2: V_{OUT}, offset 3.3V
Ch3: DRIVE

Figure 10

Figure 10 shows V_{CC} approaching the disable threshold during a 5V to 0V transition. V_{AUX} is set to 3.3V DC. When V_{CC} goes down to the 4.1V disable threshold, the regulator turns OFF. The rebound on V_{CC} is due to the step change of the voltage drop across the series resistance of the input. The output voltage V_{OUT} experiences a negative glitch due to the parasitic resistance and inductance on the V_{AUX} line. The 250mV hysteresis ensures the regulator remains enabled during the transient.

V_{CC} power-down with V_{AUX}=3.0V

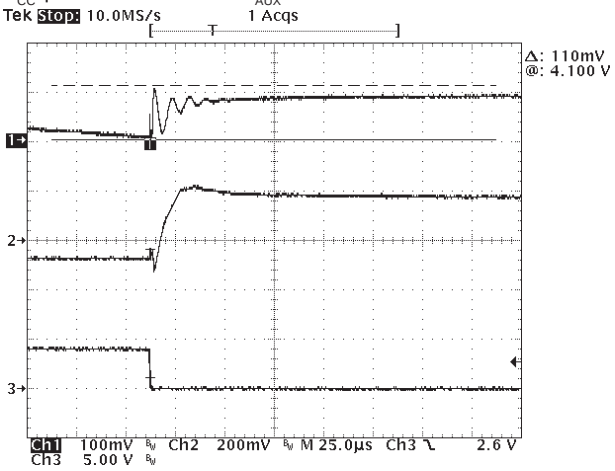


Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}, offset 3.3V
Ch3: DRIVE

Figure 11

Figures 11 - 14 show power-up and power-down transitions with V_{AUX} set to 3.0V and 3.6V.

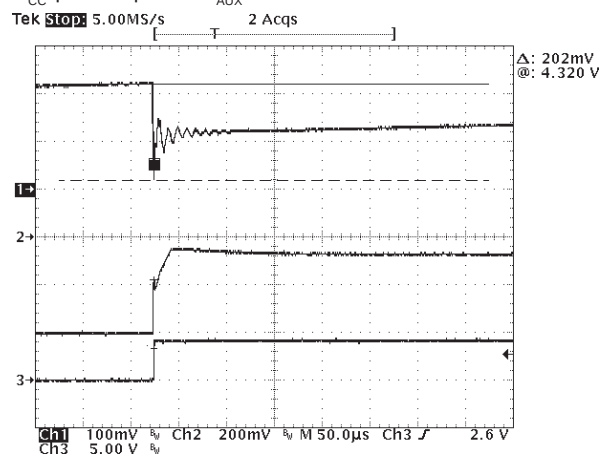
V_{CC} power-down with – V_{AUX}=3.6V



Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}, offset 3.3V
Ch3: DRIVE

Figure 12

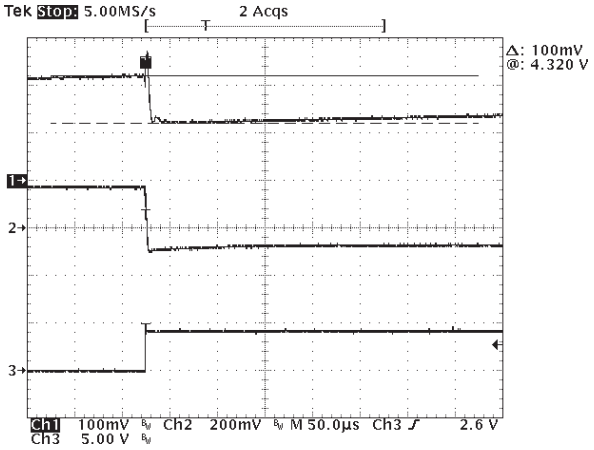
V_{CC} power-up with V_{AUX}=3.0V



Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}, offset 3.3V
Ch3: DRIVE

Figure 13

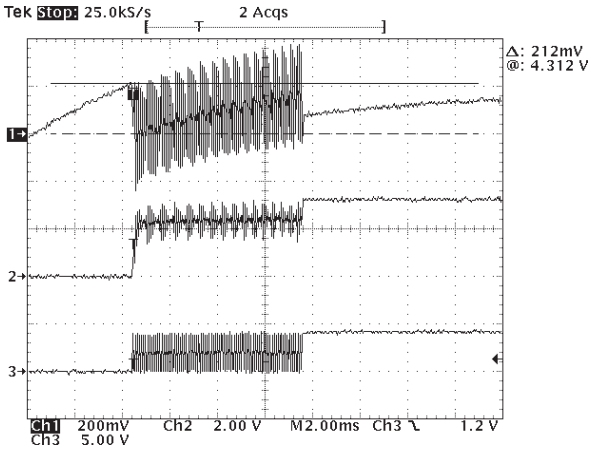
V_{CC} power-up with – V_{AUX}=3.6V



Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}, offset 3.3V
Ch3: DRIVE

Figure 14

V_{CC} power-up from 0V to 5V (cold-start) with V_{AUX} open
Bad test set-up with total series resistance of 0.7Ω on V_{CC}, by using an additional resistor of 0.5Ω.



Ch1: V_{CC}, offset 4.1V
Ch2: V_{OUT}
Ch3: DRIVE

Figure 15

Figure 15 shows a cold-start power-up transition for a test set-up with a total series resistance of 0.7Ω on V_{CC}. This is described in the "cold-start behavior" paragraph.

Evaluation Board

The SmartOR™ evaluation board is intended to facilitate the use of California Micro Devices Power Management device family, and will accommodate any individual device with installation one at a time on the board. For example, operating the CMPWR100 requires populating that device and the external capacitors around it. To obtain a board, simply contact your local California Micro Devices Sales Representative or call the Factory direct at 1-(800) 325-4966 and ask to be connected to Applications.

The board interfaces to the following signals:

- Input power supply voltages V_{CC}, V_{SBY}, V_{AUX}, and GND.
- Output voltage and signal: V_{OUT} and STATUS (or DRIVE).

It provides pad layouts for mounting two decoupling chip capacitors for each input and output of the device, as well as for a SOT-23 external P-channel MOSFET switch for the CMPWR150.

Heat spreaders are provided on the printed circuit board to improve the power dissipation for the regulator devices (i.e. CMPWR100). These are used when the devices operate under a high current load or heating condition. Various sizes of heat spreaders are provided with a copper area of up to 2 inch^2.

Conclusion

Instantly Available PCs require unique Power Management devices to provide regulated voltage sources and smart switches between power sources. California Micro Devices provides high performance integrated solutions to reduce component count and ease the design and manufacturing cycles. California Micro Devices' SmartOR™ products allow interface card manufacturers to meet the power requirements of IAPC. To find a solution to your specific requirement, call California Micro Devices for applications assistance.

References

[1] CMPWR100 data sheet, "200mA Dual Input Power Management Circuit", Rev. 9/99, California Micro Devices.

[2] CMPWR150 data sheet, "500mA / 3.3V SmartOR™ Power Regulator", Rev. 9/99, California Micro Devices.

[3] CMPWR025 data sheet, "500mA Dual Input SmartOR™ Power Switch", Rev. 9/99, California Micro Devices.

[4] "Instantly Available Power Managed Desktop PC", Design Guide, Rev. 1.2, 9/25/98, Intel Corp.

[5] "Instantly Available PC, System Power Delivery Requirements and Recommendations", Rev. 1.0, 12/30/97, Intel Corp.

[6] "PCI Bus Power Management Interface Specification" Rev. 1.1, 12/18/98, PCI Special Interest Group.