OKI Semiconductor

Oki, Network Solutions for a Global Society

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ML9228

82-Bit Duplex/Triplex VFD Controller/Driver with Digital Dimming, Keyscan

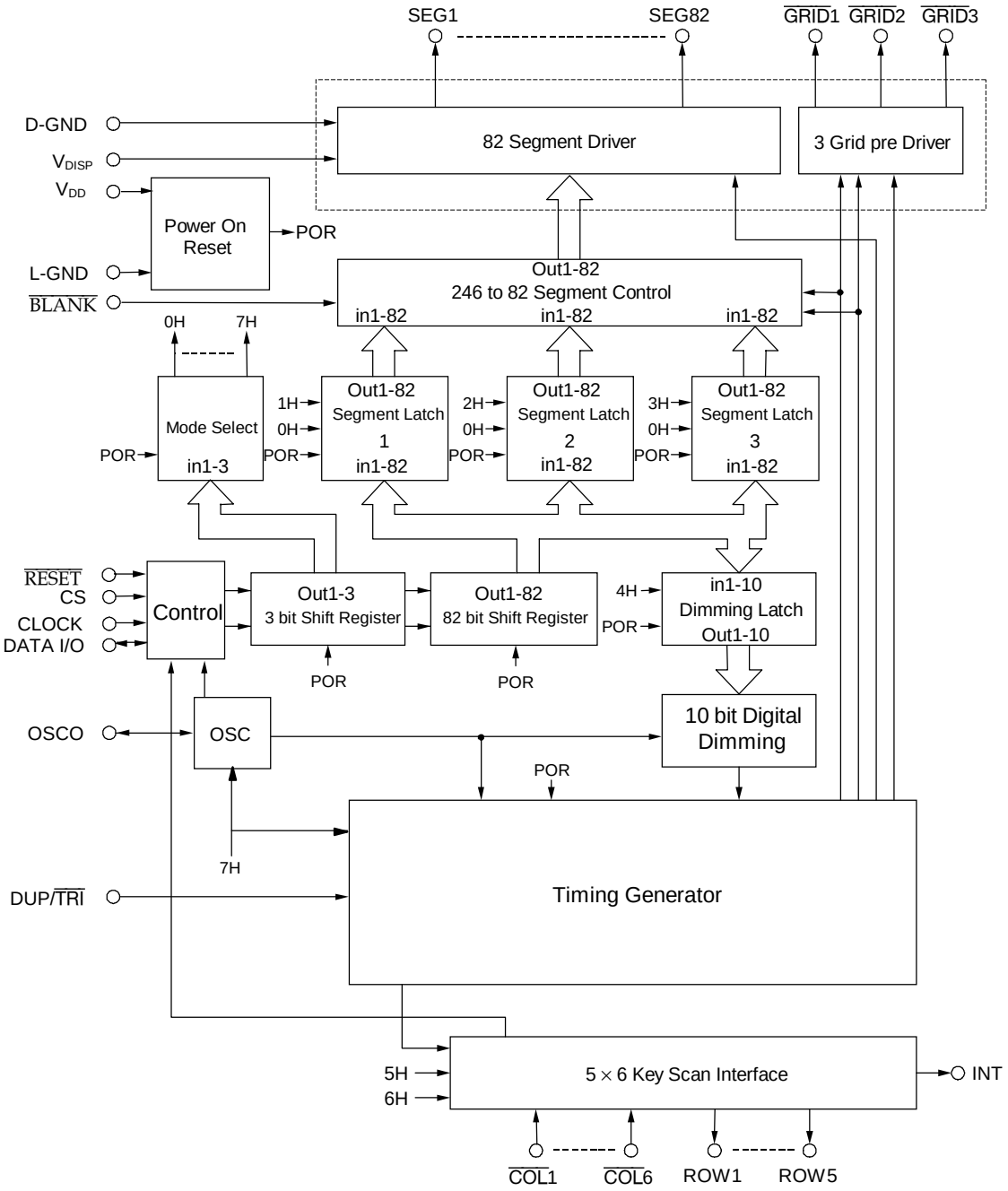
GENERAL DESCRIPTION

The ML9228 is a full CMOS controller/driver for Duplex or Triplex vacuum fluorescent display tube. It conststs of 82-segment driver outputs and 3-grid pre-driver outputs, so that it can drive directly up to 246-segment VFD. ML9228 features a digital dimming function, a 5 × 6 keyscan circuit.

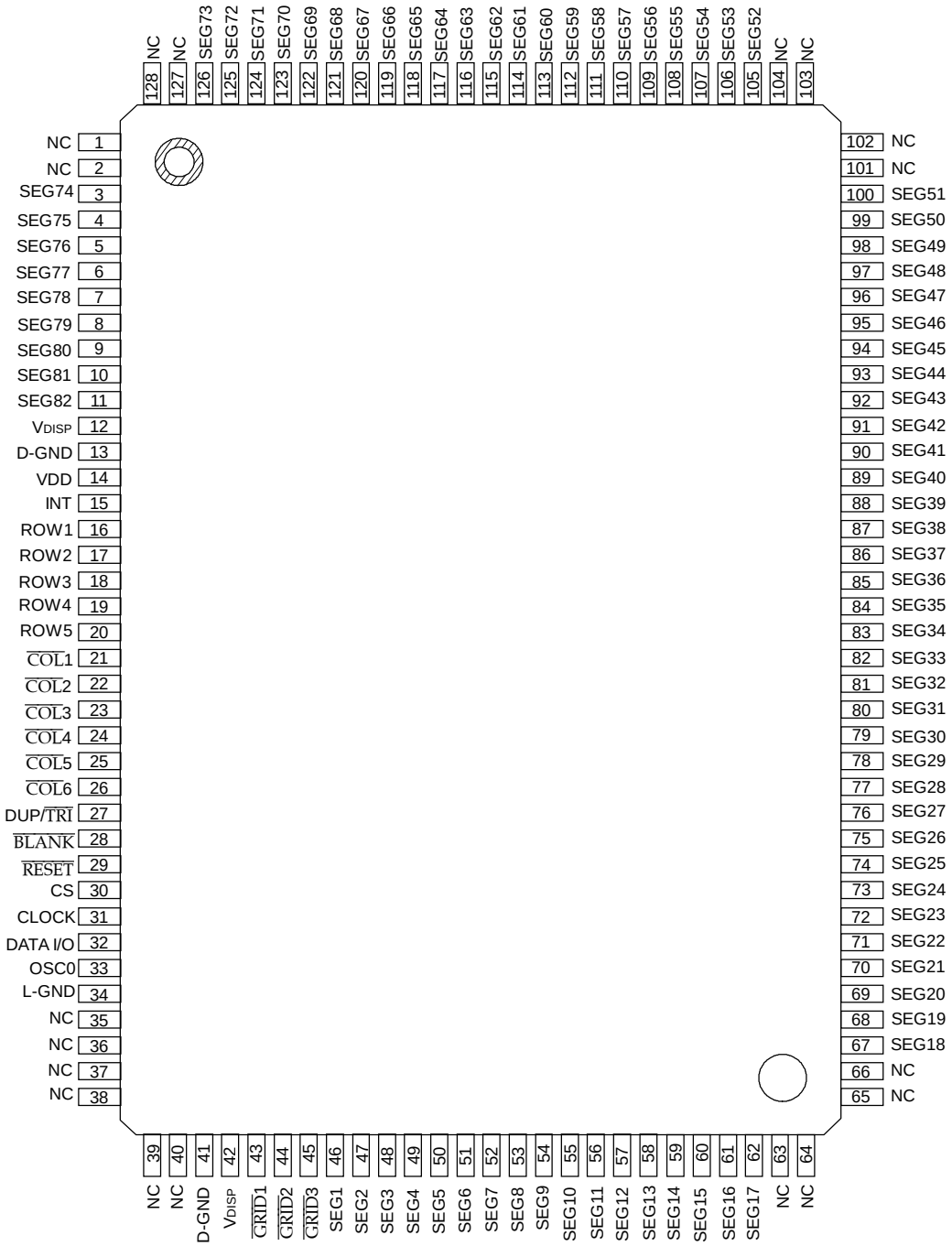
FEATURES

- Driver Supply voltage (V_{DISP}) : 8.0V to 18.5V
- Logic Supply voltage (V_{DD}) : 3.3V±10%, 5.0V±10%
- Duplex/Triplex selectable
- Applicable VFD tube : 2 Grids × 82 Anodes VFD tube
  : 3 Grids × 82 Anodes VFD tube
- 82-segment driver outputs : I_{OH} = –6 mA at V_{OH} = V_{DISP}–0.8 V (SEG1 to 82)
- 3-grid pre-driver outputs : I_{OL} = 10 mA at V_{OL} = 2 V
- Built-in digital dimming circuit (10-bit resolution)
- Built-in 5 × 6 keyscan circuit
- Built-in oscillation circuit (external R and C)
- Built-in Power-On-Reset circuit
- Package:
  128-pin plastic QFP (QFP128-P-1420-0.50-K) (ML9228 GA)

BLOCK DIAGRAM



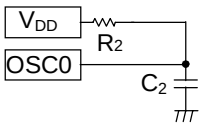
PIN CONFIGURATION (TOP VIEW)



NC : No Connection

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
12,42	V_{DISP}	—	High Level Power supply pins Pin12 and pin42 should be connected externally.
14	V_{DD}	—	Low Level Power supply pin
13,41	D-GND	—	D-GND is ground pins for the VFD driver circuit. L-GND is ground pin for the logic circuit. Pin13,Pin37 and Pin41 should be connected externally.
37	L-GND	—	
3 to 11, 46 to 62, 67 to 100, 105 to 126	SEG1 to 82	O	Segment (anode) signal output pins for a VFD tube These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OH} \leq -6$ mA, $I_{OL} \leq 500$ µA
43,44,45	$\overline{GRID}$1 to 3	O	Inverted Grid signal output pins For pre-driver, the external circuit is required. $I_{OH} \leq -6$ mA, $I_{OL} \leq 10$ mA
30	CS	I	Chip Select input pin Data input/output operation is valid when this pin is set at a High level.
31	CLOCK	I	Serial clock input pin Data is input and/or output through the DATA I/O pin at the rising edge of the serial clock.
32	DATA I/O	I/O	Serial data input/output pin Data is input to/comes out from the shift register at the rising edge of the serial clock.
15	INT	O	Interrupt signal output to microcontroller. When any key of key matrix is pressed or released, key scanning is started. After the completion of the one cycle, this pin goes to high level and keeps the high level until keyscan stop mode is selected.
27	DUP/$\overline{TRI}$	I	Duplex/Triplex operation select input pin. DUP/$\overline{TRI}$ = L(L-GND) : Triplex DUP/$\overline{TRI}$ = H(VDD) : Duplex
21 to 26	$\overline{COL}$1 to 6	I	Return inputs from the key matrix These pins are active low. When key matrix are in the inactive sate, these pins are at high level through the internal pull-up resistors. All the inputs do not have the chattering absorption function for the keyscans.
16 to 20	ROW1 to 5	O	Key switch scanning outputs Normally low level is output through these pin. When any switch of key matrix is depressed or released, key scanning is started and is continued until keyscan stop mode is selected. When keyscan stop mode is selected, all outputs of ROW1 to 5 go back to low level.
28	$\overline{BLANK}$	I	Display off control input. $\overline{BLANK}$ = L(L-GND) : Display off(SEG1-82 = L) $\overline{BLANK}$ = H(VDD) : Display on

Pin	Symbol	Type	Description
29	$\overline{\text{RESET}}$	I	The contents of the shift registers and latches are set to “0”. The digital dimming duty cycle is set to “0”. All segment outputs are set to Low level. Grid1 output is set to Low level. Grid2,3 outputs are set to High level. All the ROW outputs are set to Low level. INT output is set to Low level.
33	OSC0	I/O	RC oscillator connecting pins Oscillation frequency changes with display pipes to be used. Please refer to the right figure. 
1,2,35,36, 37,38, 40,63,64, 66,65, 101,102, 127,128	NC	—	Open pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DISP}	—	–0.3 to +20	V
	V_{DD}	—	–0.3 to +6.5	
Input Voltage	V_{IN}	—	–0.3 to +6.0	
Power Dissipation	P_D	Ta = 85 °C	590	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C
Output Current	I_{O1}	SEG1 to 82	–10.0 to +2.0	mA
	I_{O3}	$\overline{GRID}$1 to 3	–7.0 to +20.0	
	I_{O4}	ROW1 to 5, DATA I/O	–2.0 to +2.0	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Driver Supply Voltage	V_{DISP}	—		8.0	13.0	18.5	V
Logic Supply Voltage	V_{DD}	Unit Supply Voltage 5.0 V (Typ)		4.5	5.0	5.5	
		Unit Supply Voltage 3.3 V (Typ)		3.0	3.3	3.6	
Oscillation Frequency	f_{OSC}	VDD = 5.0 V (Typ) R_2 = 10 kΩ ±5%, C_2 = 27 pF ±5%		2.6	3.3	4.0	MHz
		VDD = 3.3 V (Typ) R_2 = 8.2 kΩ ±5%, C_2 = 27 pF ±5%		2.6	3.3	4.0	MHz
Frame Frequency	f_{FR}	VDD=5.0 V (Typ) R_2 = 10 kΩ ±5% C_2 = 27 pF ±5%	1/3 Duty	211	269	325	Hz
			1/2 Duty	317	403	488	
		VDD=3.3 V (Typ) R_2 = 8.2 kΩ ±5% C_2 = 27 pF ±5%	1/3 Duty	211	269	325	Hz
			1/2 Duty	317	403	488	
Operating Temperature	T_{OP}	—		-40	—	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40 to +85°C, V_{DD} = 5.0 V±10%, V_{DISP} = 8.0 to 18.5 V)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1)	—		0.7 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	*1)	—		—	0.3 V_{DD}	V
High Level Input Current	I_{IH1}	*2)	V_{IH} = V_{DD}		–5.0	+5.0	µA
	I_{IH2}	*3)	V_{IH} = V_{DD}		–50	–5.0	
Low Level Input Current	I_{IL1}	*2)	V_{IL} = 0.0 V		–5.0	+5.0	µA
	I_{IL2}	*3)	V_{IL} = 0.0 V		–120	–10	
High Level Output Voltage	V_{OH1}	SEG1 to 82	V_{DISP} = 9.5V	I_{OH1} = –6 mA	V_{DISP}–0.8	—	V
	V_{OH2}	$\overline{GRID}$1 to 3		I_{OH3} = –6 mA	V_{DISP}–0.8	—	
	V_{OH3}	*4)		I_{OH4} = –120 µA	V_{DD}–0.8	—	
				Output Open	V_{DD}–0.2	—	
Low Level Output Voltage	V_{OL1}	SEG1 to 82	V_{DISP} = 9.5V	I_{OL1} = 500 µA	—	2.0	V
	V_{OL2}	$\overline{GRID}$1 to 3		I_{OL3} = 10 mA	—	2.0	
	V_{OL3}	*5)		I_{OL4} = 120 µA	—	0.8	
Supply Current	I_{DISP}	V_{DISP}	R_2 = 10 kΩ ±5%, C_2 = 27 pF ±5%, no load		—	500	µA
	I_{DD}	V_{DD}	R_2 = 10 kΩ ±5%, C_2 = 27 pF ±5%		—	5.0	mA
	I_{SLP1}	V_{DISP}	Sleep Mode		—	5.0	µA
	I_{SLP2}	V_{DD}	Sleep Mode		—	5.0	µA

*1) CS, CLOCK, DATA I/O, DUP/$\overline{TRI}$, $\overline{BLANK}$, $\overline{RESET}$, $\overline{COL}$1 to 6
*2) CS, CLOCK, DATA I/O, DUP/$\overline{TRI}$, $\overline{BLANK}$, $\overline{RESET}$
*3) $\overline{COL}$1 to 6
*4) DATA I/O, INT
*5) DATA I/O, INT, ROW1 to 5

DC Characteristics

(Ta = –40 to +85°C, V_{DD} = 3.3 V±10%, V_{DISP} = 8.0 to 18.5 V)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1)	—		0.8 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	*1)	—		—	0.2 V_{DD}	V
High Level Input Current	I_{IH1}	*2)	V_{IH} = V_{DD}		–5.0	+5.0	µA
	I_{IH2}	*3)	V_{IH} = V_{DD}		-40	-5.0	
Low Level Input Current	I_{IL1}	*2)	V_{IL} = 0.0 V		–5.0	+5.0	µA
	I_{IL2}	*3)	V_{IL} = 0.0 V		-100	-5.0	
High Level Output Voltage	V_{OH1}	SEG1 to 82	V_{DISP} = 9.5V	I_{OH1} = –6 mA	V_{DISP}–0.8	—	V
	V_{OH3}	$\overline{GRID}$1 to 3		I_{OH3} = –6 mA	V_{DISP}–0.8	—	
	V_{OH3}	*4)		I_{OH4} = –100 µA	V_{DD} –0.4	—	
				Output Open	V_{DD} –0.2	—	
Low Level Output Voltage	V_{OL1}	SEG1 to 82	V_{DISP} = 9.5V	I_{OL1} = 500 µA	—	2.0	V
	V_{OL2}	$\overline{GRID}$1 to 3		I_{OL3} = 10 mA	—	2.0	
	V_{OL3}	*5)		I_{OL4} = 100 µA	—	0.4	
Supply Current	I_{DISP}	V_{DISP}	R_2 = 8.2 kΩ ±5%, C_2 = 27 pF ±5%, no load		—	500	µA
	I_{DD}	V_{DD}	R_2 = 8.2 kΩ ±5%, C_2 = 27 pF ±5%		—	4.0	mA
	I_{SLP1}	V_{DISP}	Sleep Mode		—	5.0	µA
	I_{SLP2}	V_{DD}	Sleep Mode		—	5.0	µA

*1) CS, CLOCK, DATA I/O, DUP/$\overline{TRI}$, $\overline{BLANK}$, $\overline{RESET}$, $\overline{COL}$1 to 6
*2) CS, CLOCK, DATA I/O, DUP/$\overline{TRI}$, $\overline{BLANK}$, $\overline{RESET}$
*3) $\overline{COL}$1 to 6
*4) DATA I/O, INT
*5) DATA I/O, INT, ROW1 to 5

AC Characteristics

(Ta = –40 to +85°C, V_{DD} = 5.0 V±10%, V_{DISP} = 8.0 to 18.5 V)

Parameter	Symbol	Condition		Min.	Max.	Unit
Clock Frequency	f_C	—		—	2.0	MHz
Clock Pulse Width	t_{CW}	—		200	—	ns
Data Setup Time	t_{DS}	—		200	—	ns
Data Hold Time	t_{DH}	—		200	—	ns
CS Off Time	t_{CSL}	R_2 = 10 kΩ ±5%, C_2 = 27 pF ±5%		20	—	µs
CS Setup Time (CS-Clock)	t_{CSS}	—		200	—	ns
CS Hold Time (Clock-CS)	t_{CSH}	—		200	—	ns
DATA Output Delay Time (Clock-DATA I/O)	t_{PD}	—		—	1.0	µs
Output Slew Rate Time	t_R	C_L=100 pF	t_R = 20 to 80%	—	2.0	µs
	t_F		t_F = 80 to 20%	—	2.0	µs
V_{DD} Rise Time	t_{PRZ}	Mounted in a unit		—	100	µs
V_{DD} Off Time	t_{POF}	Mounted in a unit, V_{DD} = 0.0 V		5.0	—	ms
CS Wait Time	t_{RSOFF}	—		400	—	µs

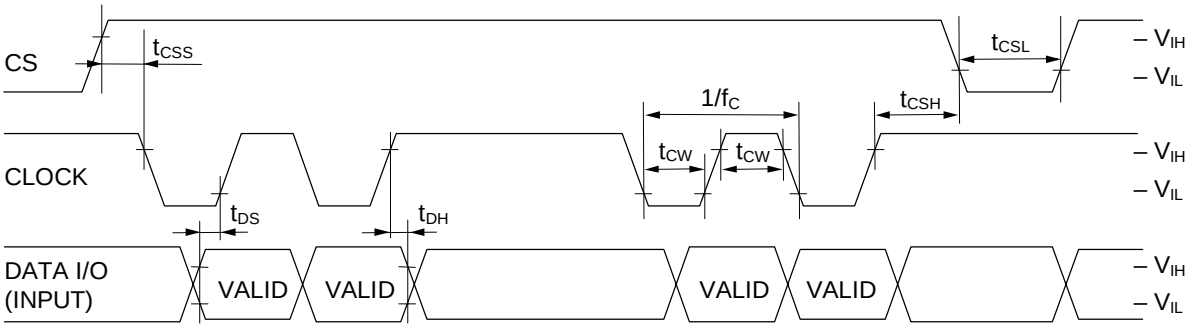
(Ta = –40 to +85°C, V_{DD} = 3.3 V±10%, V_{DISP} = 8.0 to 18.5 V)

Parameter	Symbol	Condition		Min.	Max.	Unit
Clock Frequency	f_C	—		—	1.0	MHz
Clock Pulse Width	t_{CW}	—		400	—	ns
Data Setup Time	t_{DS}	—		400	—	ns
Data Hold Time	t_{DH}	—		400	—	ns
CS Off Time	t_{CSL}	R_2 = 8.2 kΩ ±5%, C_2 = 27 pF ±5%		20	—	µs
CS Setup Time (CS-Clock)	t_{CSS}	—		400	—	ns
CS Hold Time (Clock-CS)	t_{CSH}	—		400	—	ns
DATA Output Delay Time (Clock-DATA I/O)	t_{PD}	—		—	1.0	µs
Output Slew Rate Time	t_R	C_L=100 pF	t_R = 20 to 80%	—	2.0	µs
	t_F		t_F = 80 to 20%	—	2.0	µs
V_{DD} Rise Time	t_{PRZ}	Mounted in a unit		—	100	µs
V_{DD} Off Time	t_{POF}	Mounted in a unit, V_{DD} = 0.0 V		5.0	—	ms
CS Wait Time	t_{RSOFF}	—		400	—	µs

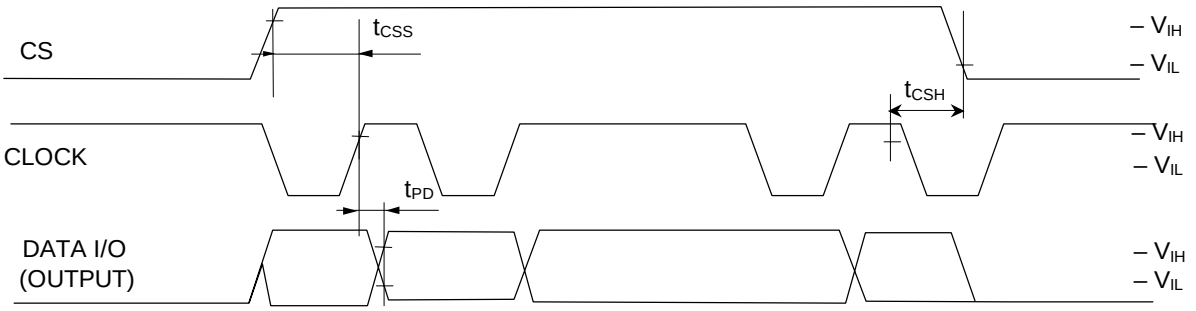
TIMING DIAGRAMS

	V_{DD} = 3.3 V±10%	V_{DD} = 5.0 V±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

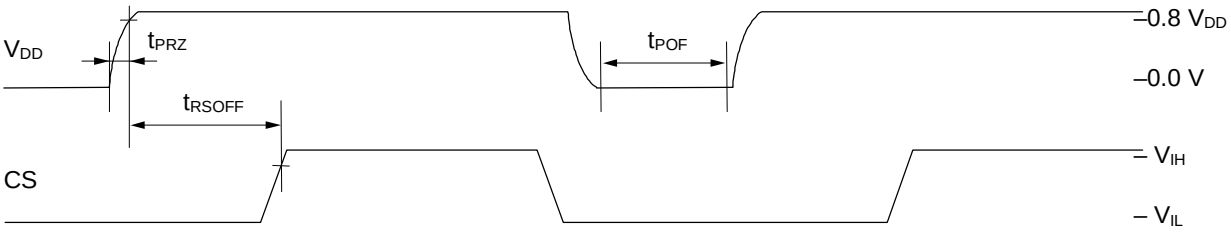
Data Input Timing



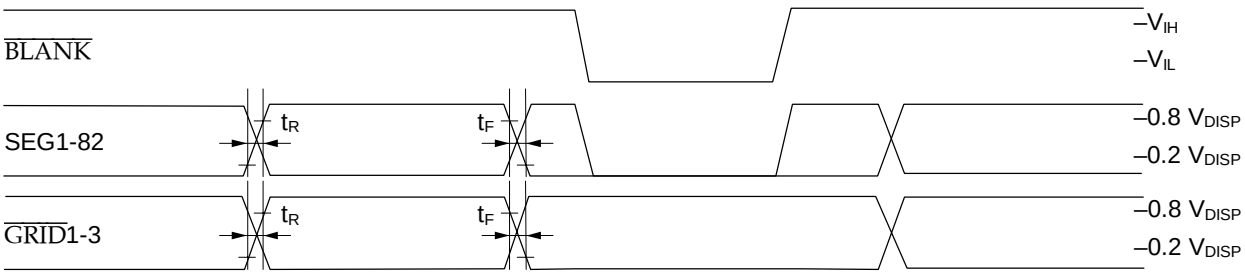
Data Output Timing



Power-On Reset Timing



Driver Output Timing



Keyscan Characteristics

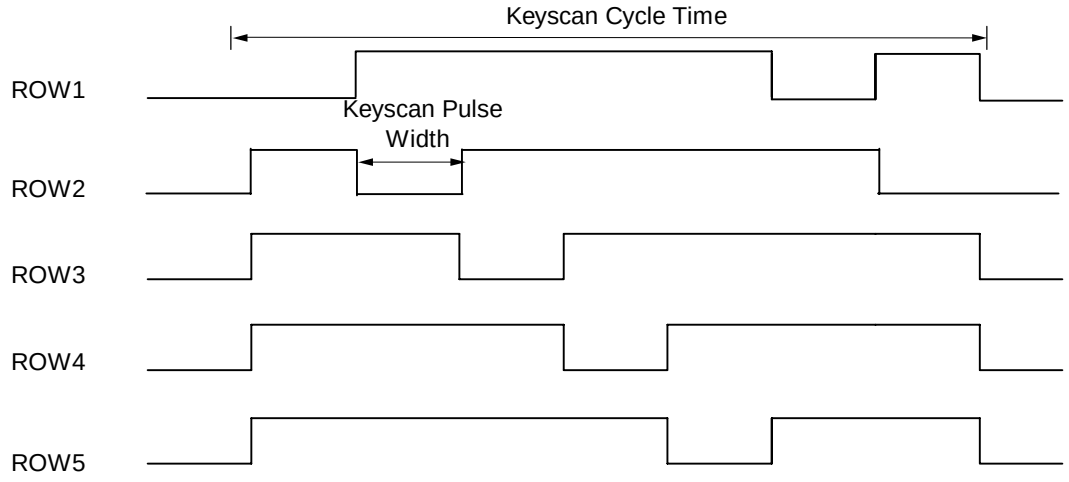
(Ta = –40 to +85°C, V_{DD} = 5.0 V±10%, V_{DISP} = 8.0 to 18.5 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	R_2 = 10 kΩ ±5%, C_2 = 27 pF ±5%	160	194	246	µs
Keyscan Pulse Width	R_2 = 10 kΩ ±5%, C_2 = 27 pF ±5%	32	39	49	µs

(Ta = –40 to +85°C, V_{DD} = 3.3 V±10%, V_{DISP} = 8.0 to 18.5 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	R_2 = 8.2 kΩ ±5%, C_2 = 27 pF ±5%	160	194	246	µs
Keyscan Pulse Width	R_2 = 8.2 kΩ ±5%, C_2 = 27 pF ±5%	32	39	49	µs

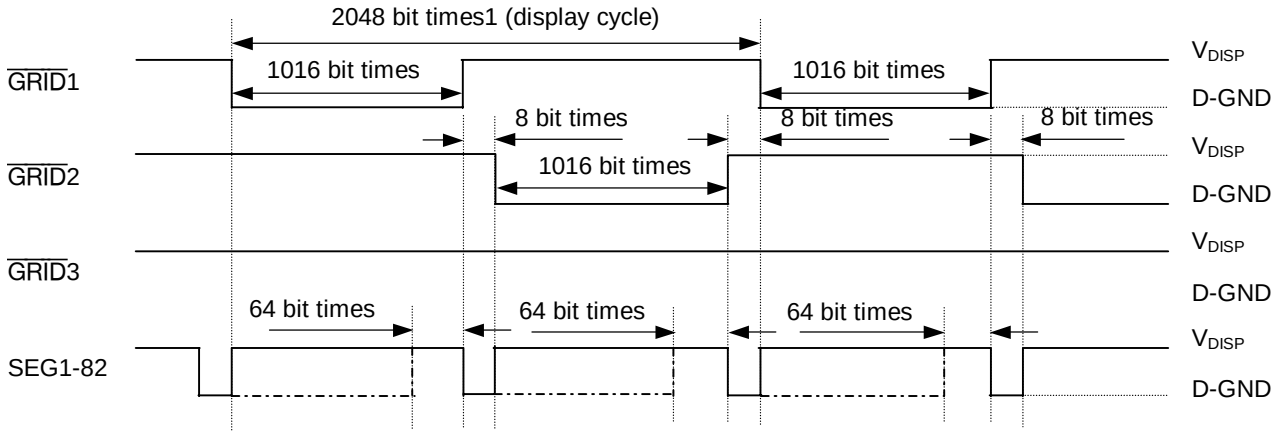
Keyscan Timing



Output Timing (Duplex Operation) *1 bit time = $4/f_{OSC}$

Solid line: When dimming data is made into 1016/1024

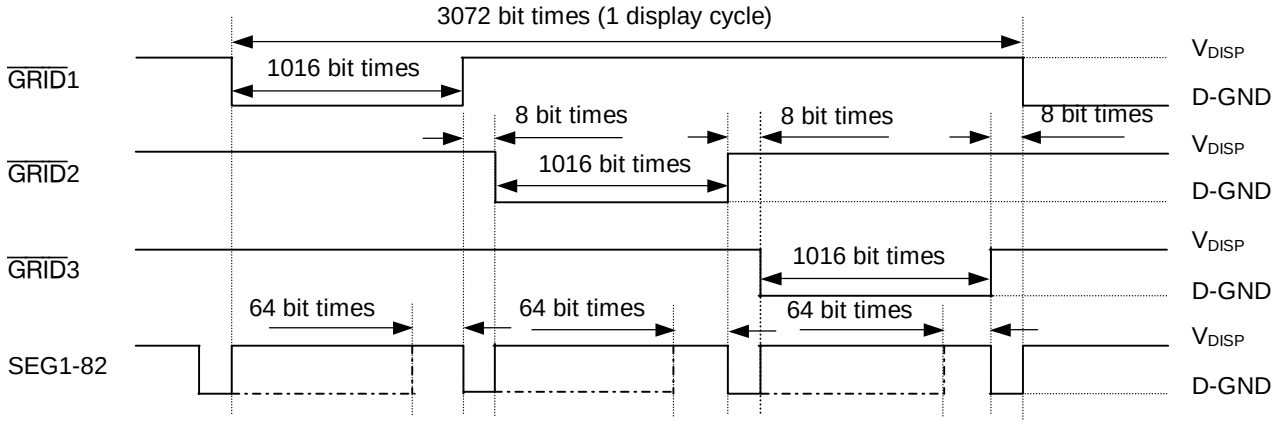
Dotted line: When dimming data is made into 64/1024



Output Timing (Triplex Operation) *1 bit time = $4/f_{OSC}$

Solid line: When dimming data is made into 1016/1024

Dotted line: When dimming data is made into 64/1024



FUNCTIONAL DESCRIPTION

Power-on Reset
When power is turned on, ML9228 is initialized by the internal power-on reset circuit.
The status of the internal circuit after initialization is as follows:

- The contents of the shift registers and latches are set to “0”.
- The digital dimming duty cycle is set to “0”.
- All segment outputs are set to Low level.
- Grid1 output is set to Low level. Grid2,3 outputs are set to High level.
- All the ROW outputs are set to Low level.
- INT output is set to Low level.

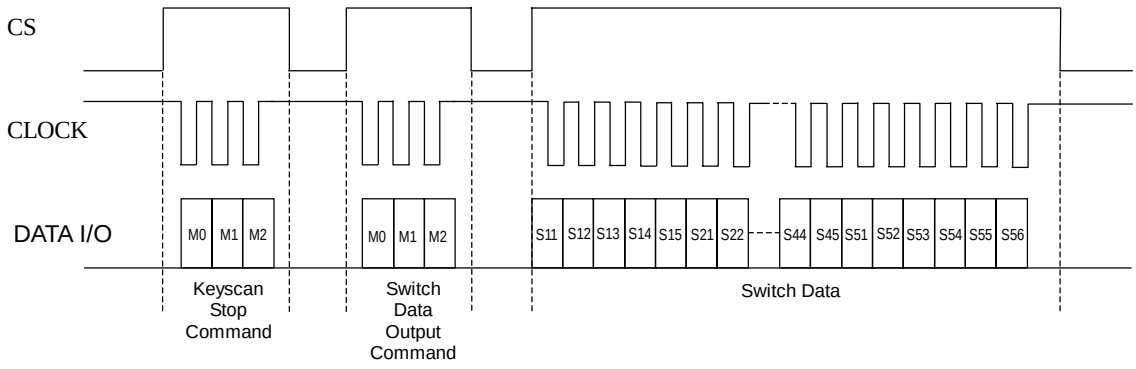
Reset
When power is turned on, ML9228 is initialized by the internal power-on reset circuit.
The status of the internal circuit after initialization is as follows:

- The contents of the shift registers and latches are set to “0”.
- The digital dimming duty cycle is set to “0”.
- All segment outputs are set to Low level.
- Grid1 output is set to Low level. Grid2,3 outputs are set to High level.
- All the ROW outputs are set to Low level.
- INT output is set to Low level.
- A command is received by the signal of Low(L-GND) level.

Blank
All segment outputs are set as a Low level.

- A command is received by the signal of Low(L-GND) level.

Data Input and Output
Data input and output through the DATA-I/O pin is valid only when the CS pin is set at a High level.
The input data to DATA I/O pin is shifted into the shift register at the rising edge of the serial clock. The data is automatically loaded to the latches when the CS pin is set at a Low level.
10-bit dimming data (D1 to D10) and 82-bit segment data (S1 to S82) are used for inputting of dimming data and display data. To transfer these two data, the mode data (M0 to M2) must be sent after each of these data succeddingly.
The output data from the DATA I/O pin is output from the shift register at the rising edge of the serial clock.
ML9228 outputs 30-bit key data (S11 to S56). To receive these data, the mode data (M0 to M2) must be sent first and then CS must be set once to Low level and set again to High level.
Then inputting serial clocks, these data are output from the DATA I/O pin.
When the CS pin is set at a Low level, the DATA I/O pin returns to an input pin.
To stop the keyscan, the only mode data (M0 to M2) must be sent. After the mode data transfer, the key scanning is stopped immediately.



Mode Data

ML9228 has the seven function modes. The function mode is selected by the mode data (M0 to M2). The relation between function mode and mode data (M0 to M2) is as follows:

FUNCTION MODE	OPERATING MODE	FUNCTION DATA		
		M0	M1	M2
0	Segment Data for $\overline{\text{GRID}}$1-3 Input	0	0	0
1	Segment Data for $\overline{\text{GRID}}$1 Input	1	0	0
2	Segment Data for $\overline{\text{GRID}}$2 Input	0	1	0
3	Segment Data for $\overline{\text{GRID}}$3 Input	1	1	0
4	Digital Dimming Data Input	0	0	1
5	Keyscan Stop	1	0	1
6	Switch Data Output	0	1	1
7	Sleep	1	1	1

Segment Data Input [Function Mode: 0 to 3]

- ML9228 receives the segment data when function mode 0 to 3 are selected.
- The same segment data is transferred to the 3 segment data latch correspond to $\overline{\text{GRID}}$1 to 3 at the same time when the function mode 0 is selected.
- The segment data is transferred to only one segment data latch that is selected by mode data, when the function mode is 1, 2 or 3 is selected.
- Segment output (SEG1 to 82) becomes High level when the segment data (S1 to S82) is High level.

[Data Format]

Input Data : 85 bits
Segment Data : 82 bits
Mode Data : 3 bits

Bit	1	2	3	4	----------	79	80	81	82	83	84	85
Input Data	S1	S2	S3	S4	----------	S79	S80	S81	S82	M0	M1	M2

Segment Data (82 bits) — Mode Data (3 bits)

[Bit correspondence between segment output and segment data]

SEG n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Segment data	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
SEG n	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Segment data	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32
SEG n	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Segment data	S33	S34	S35	S36	S37	S38	S39	S40	S41	S42	S43	S44	S45	S46	S47	S48
SEG n	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
Segment data	S49	S50	S51	S52	S53	S54	S55	S56	S57	S58	S59	S60	S61	S62	S63	S64
SEG n	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
Segment data	S65	S66	S67	S68	S69	S70	S71	S72	S73	S74	S75	S76	S77	S78	S79	S80
SEG n	81	82														
Segment data	S81	S82														

Digital Dimming Data Input [Function Mode: 4]

- ML9228 receives the digital dimming data when function mode 4 is selected.
- The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99.2%) for each grid.
- The 10-bit digital dimming data is input from LSB.

[Data Format]

Input Data : 13 bits
Digital Dimming Data : 10 bits
Mode Data : 3 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13
Input Data	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	M0	M1	M2
	LSB ← Digital Dimming Data (10 bits) → MSB										Mode Data (3 bits)		

(LSB) Dimming Data (MSB)										Duty Cycle
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
0	0	0	0	0	0	0	0	0	0	0/1024
1	0	0	0	0	0	0	0	0	0	1/1024
1	1	1	0	1	1	1	1	1	1	1015/1024
0	0	0	1	1	1	1	1	1	1	1016/1024
1	0	0	1	1	1	1	1	1	1	1016/1024
1	1	1	1	1	1	1	1	1	1	1016/1024

Keyscan Stop [Function Mode: 5]

- ML9228 stops a key scanning when function mode 5 are selected.
- To select this mode, the only mode data (M0 to M2) is needed.
- The actual time lag range between receipt of the keyscan stop command and the ceasing of scanning is 2.4 µs to 3.6 µs

[Input Data Format]

Input Data : 3 bits
Mode Data : 3 bits

Bit	83	84	85
Input Data	M0	M1	M2
	← Mode Data → (3 bits)		

Switch Data Output [Function Mode: 6]

- ML9228 output the switch data when function mode 6 is selected.
- To select this mode, the only mode data (M0 to M2) is needed.
- When ML9228 recieves this mode, the DATA I/O pin is changed to an output pin.
- 30-bit switch data come out from the DATA I/O pin synchronizing with the rise edge of the clock.
- When the CS pin is set at the low level, the DATA I/O pin returns to an input pin.
- Contact Count bits are Q1 (LSB) to Q3 (MSB)

[Input Data Format]

Input Data : 3 bits
Mode Data : 3 bits

Bit	83	84	85
Input Data	M0	M1	M2
	← Mode Data → (3 bits)		

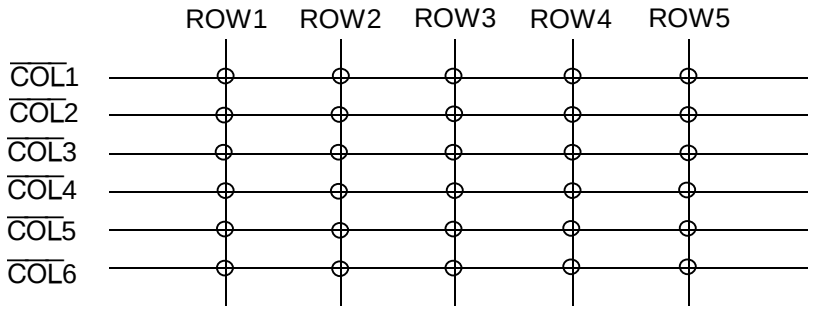
[Output Data Format]

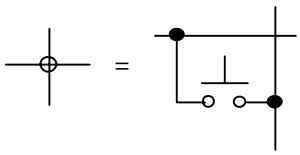
Output Data : 30 bits
5 × 6 push switch Data : 30 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12
Output Data	S11	S12	S13	S14	S15	S16	S21	S22	S23	S24	S25	S26
Bit	13	14	15	16	17	18	19	20	21	22	23	24
Output Data	S31	S32	S33	S34	S35	S36	S41	S42	S43	S44	S45	S46
Bit	25	26	27	28	29	30						
Output Data	S51	S52	S53	S54	S55	S56						

Sij: i = ROW1 to 5, j = $\overline{\text{COL}}$1 to 6
Sij = 1: Switch ON
Sij = 0: Switch OFF

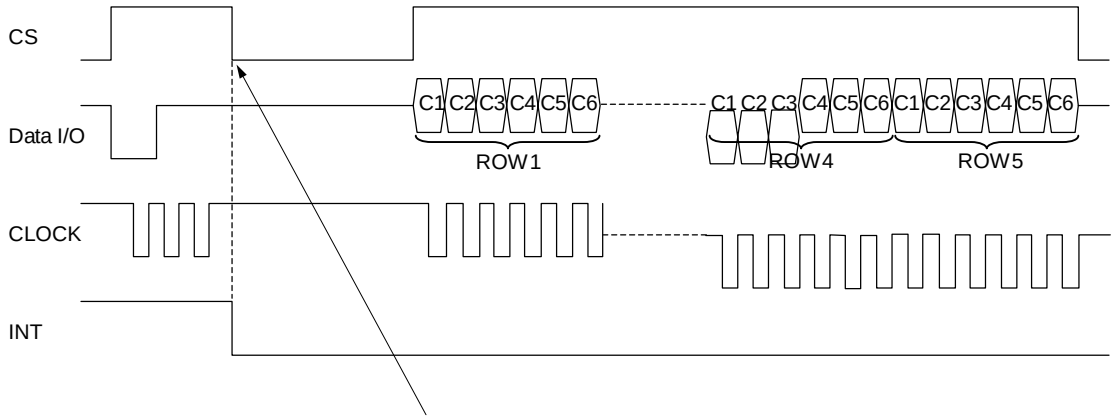
[5 × 6Push Switch]





P-in/S-out shift resistor

When the switch data output mode is selected and CS goes L, all the key data send to the shift resistor, and the up/down counter is reset and the INT signal goes “L”.

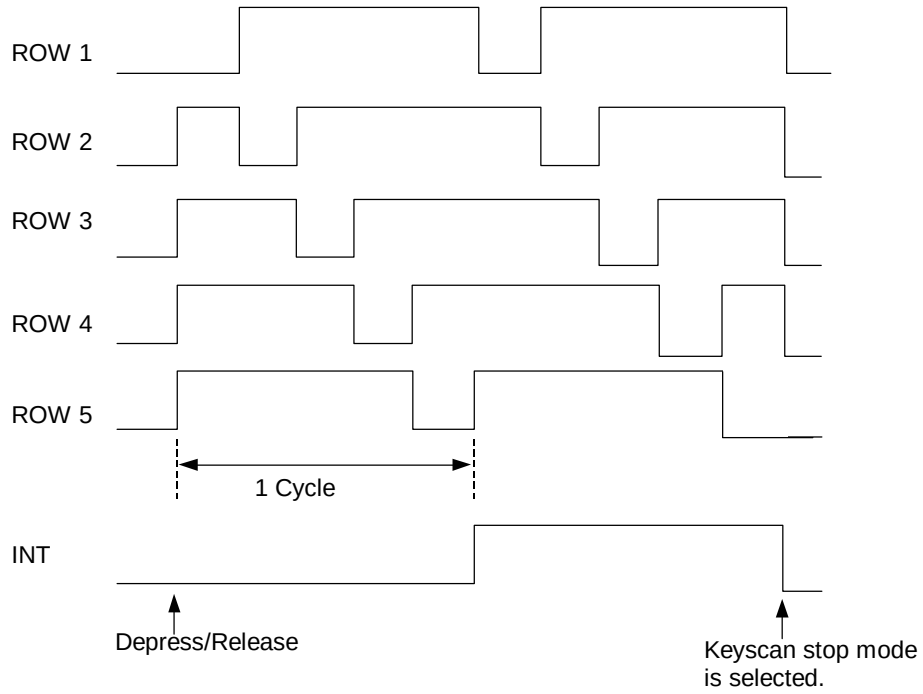


When CS goes L, the up/down counter is reset and the INT goes “L”.

Keyscan

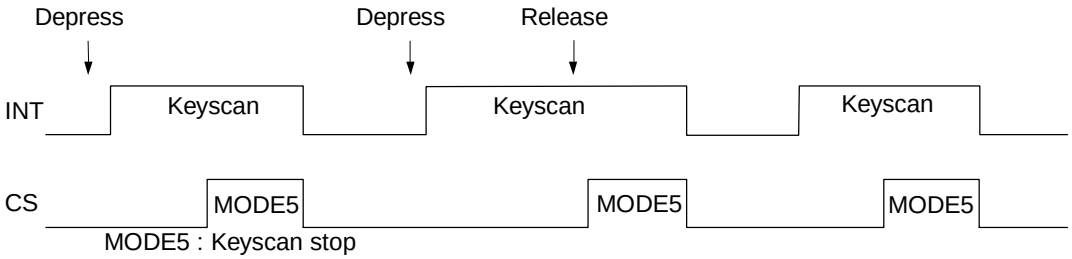
Keyscanning is started only when depression or release of any key is detected in order to minimize noise caused by scanning signal. Then, keyscanning is continued until the keyscan stop mode is sent from a microcomputer. The INT pin goes to the high level at the completion of 1-cycle scanning after the keyscan start, so the (high level) signal sent from the INT pin can be used as an interrupt signal.

[Keyscan Timing]



Note: Keyscanning cannot be stopped by selecting the keyscan stop mode only once if:
- keyscanning is started after depression or release of any key is detected, and then
- a key is depressed or released again before the keyscan stop mode is selected.

To stop keyscanning, it is required to select the keyscan stop mode once again.



Sleep [Function Mode: 7]

- ML9228 oscillation stops and segment display turns off when function mode 7 is selected.
- key matrix is pushed, this mode will be canceled and it will usually become display mode.

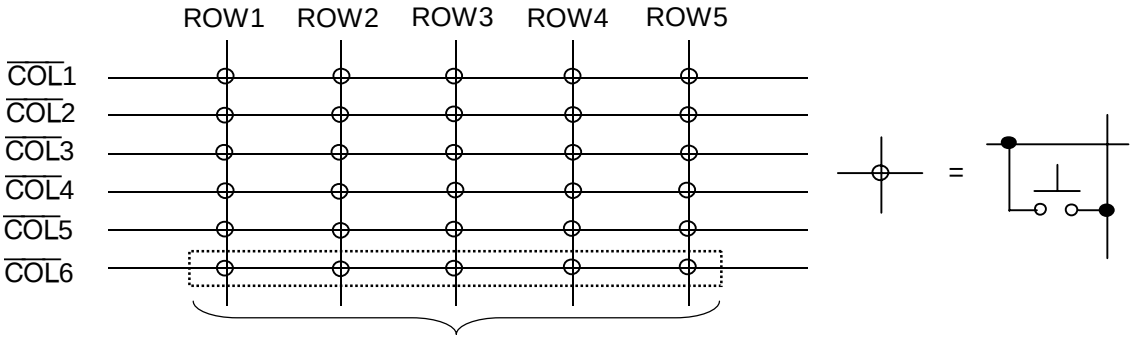
[Input Data Format]

Input Data : 3 bits
Mode Data : 3 bits

Bit	83	84	85
Input Data	M0	M1	M2
	← Mode Data → (3 bits)		

Wake up

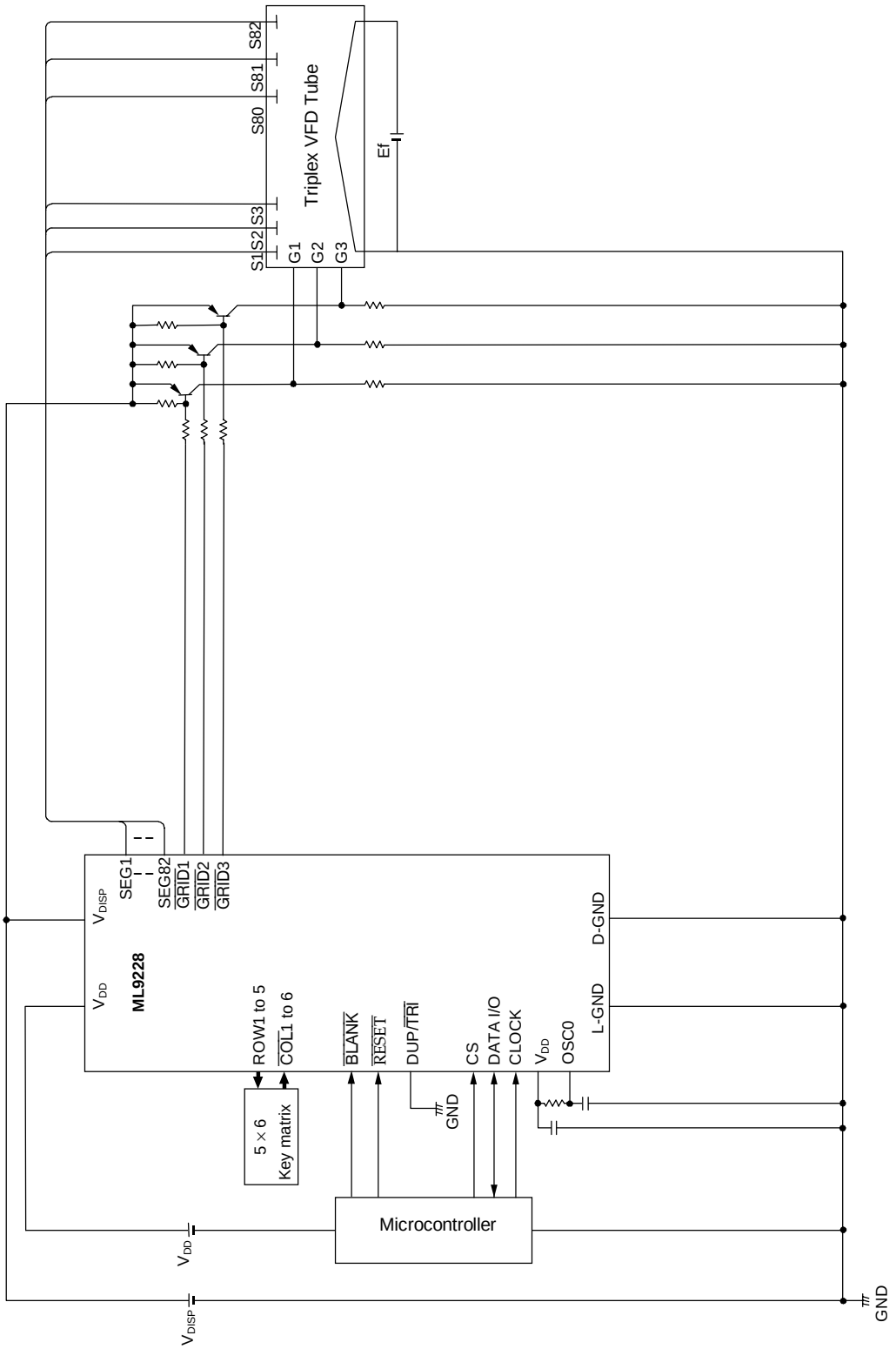
- Wake up by key press from $\overline{\text{COL}}$6. Then, key scan is performed.
- Wake up by CS assert(rising edge). Then, key scan does not carry out.
- Oscillation restarts to accept normal operation.
- Previous output for display data till updated by Each Mode.



If either of these keys is pushed, an oscillation will be started and it will usually return to operation.

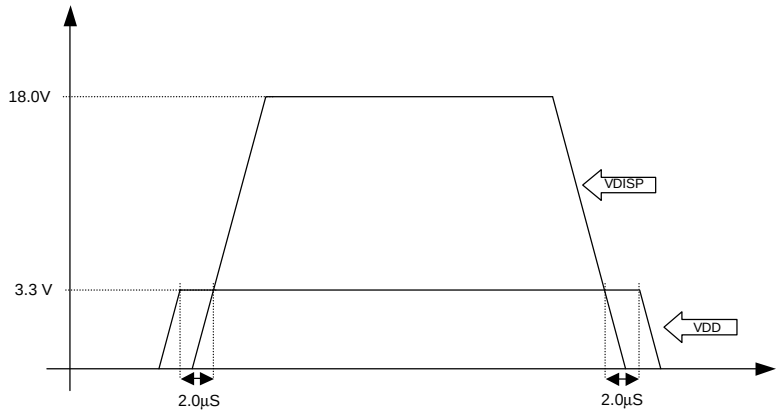
APPLICATION CIRCUITS

Circuit for the triplex VFD tube with 246 segments (3 Grid × 82 Anode)



POWER SEQUENCE

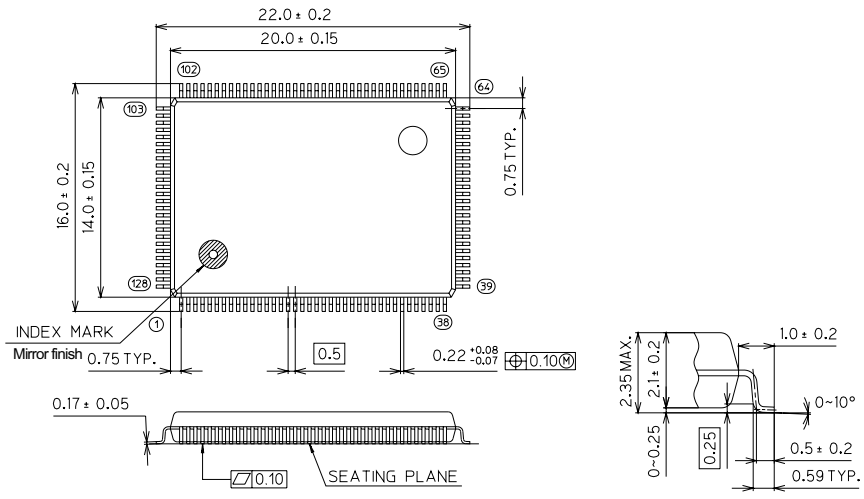
- If the power sequence (please see below) recommended by Oki is not followed,it is possible to damage internal logic transistors.
- Currently there is no definition for the time period between the point that V_{DD} = 3.3V V_{DISP} = 3.3V.
- Oki recommends the following sequence.



PACKAGE DIMENSIONS

(Unit: mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.19 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9228-01	Oct. 20, 2004	—	—	Final edition 1

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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