# VT6304

## 1394.A 4 PORT PHYSICAL LAYER CHIP

# DATA SHEET

## (Preliminary)

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**VIA TECHNOLOGIES, INC.**

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## VT6304 IEEE 1394A FOUR PORT CABLE TRANSCEIVER/ARBITER FEATURES

- Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus and the P1394a Supplement 2.0.
- Full P1394a Supplement Support includes:
  - Arbitrated short reset,
  - Connection Debounce,
  - Multispeed Concatenation,
  - Ack Accelerated Arbitration,
  - Fly-By Concatenation,
  - Programmable Port Disable, Suspend, Resume,
  - PHY IDs Do Not Increment Past 63
- Provides Four 1394a Fully Compliant Cable Ports at 100/200/400 Megabits per Second (Mbit/s)
- Single 3.3 V power supply
- Logic Performs Bus Initialization and Arbitration Functions
- Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding
- Incoming Data Resynchronized to Local Clock.
- Data Interface to Link-Layer Controller Provided Through 2/4/8 Parallel Lines at 49.152 MHz
- 24.576 MHZ Crystal Oscillator and PLL Provide TX/RX Data at 100/200/400 Mbps and Link-Layer Controller Clock at 49.152 MHZ.
- Cable Power Presence Monitoring.
- Programable Node Power Class Information for System Power Management
- Embedded Bus Holder Isolation to Link Layer Controller Interface
- Optional On-chip Resistors to Reduce Component Counts for Electrical Isolation to Link Layer Controller Interface
- Fully Compliant P1394a 2.0 PHY Map
- Separate TPBIAS for Each Port
- Fully Interoperable with IEEE Std1394-1995 Devices
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Low Power Design for Battery-Powered Applications includes: User Controlled Power-Down via PD, Automatic Device Power-Down during All Ports Suspended and Link Interface Disabled, Link Interface Power-Down via Inactive LPS, Automatic Inactive Ports Powered-Down, and Automatic Inactive Logic Power-Down
- Self Power Up Reset and Pinless PLL to Reduce Component Counts on System
- Low Cost 100-Pin PQFP package

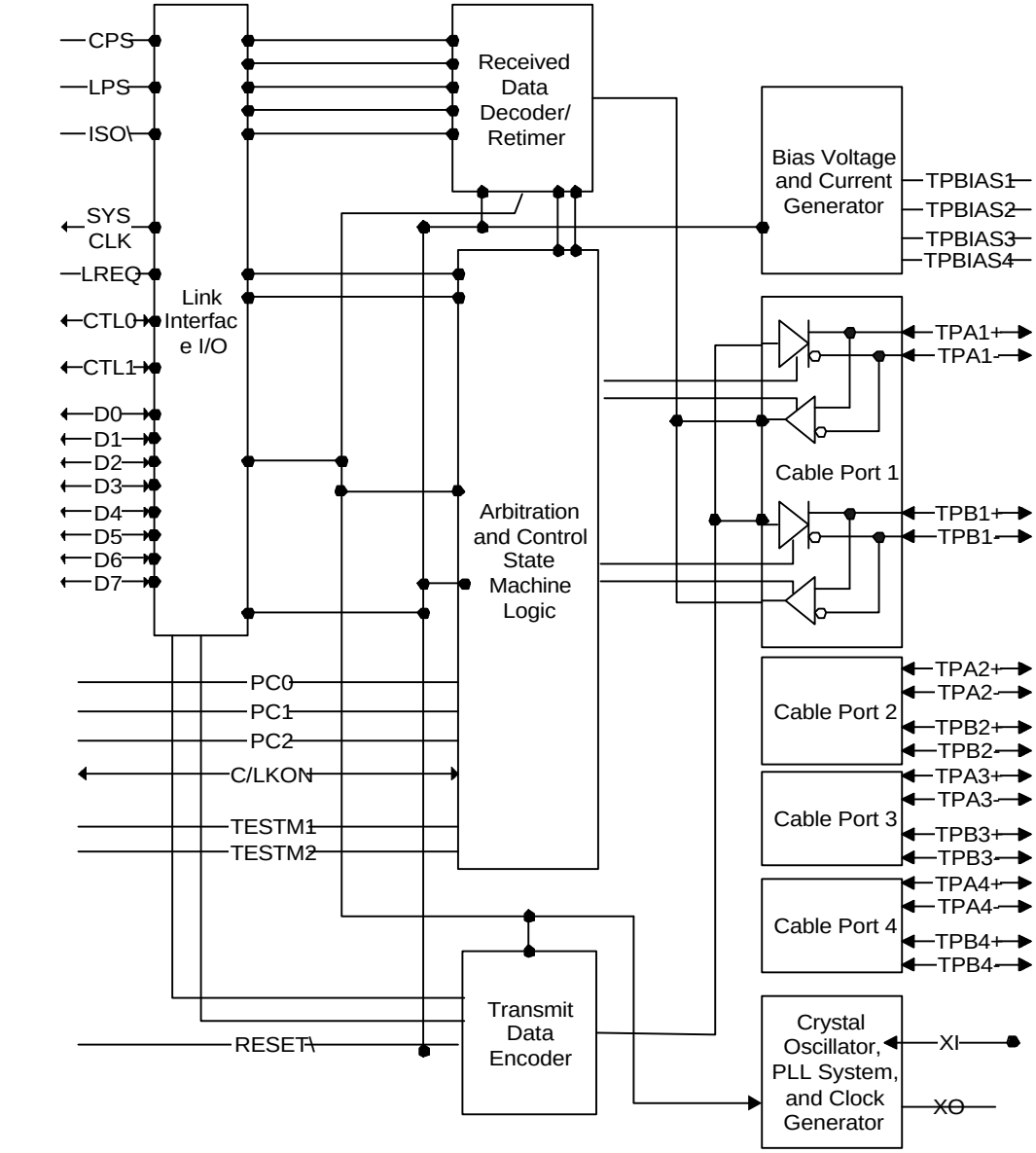
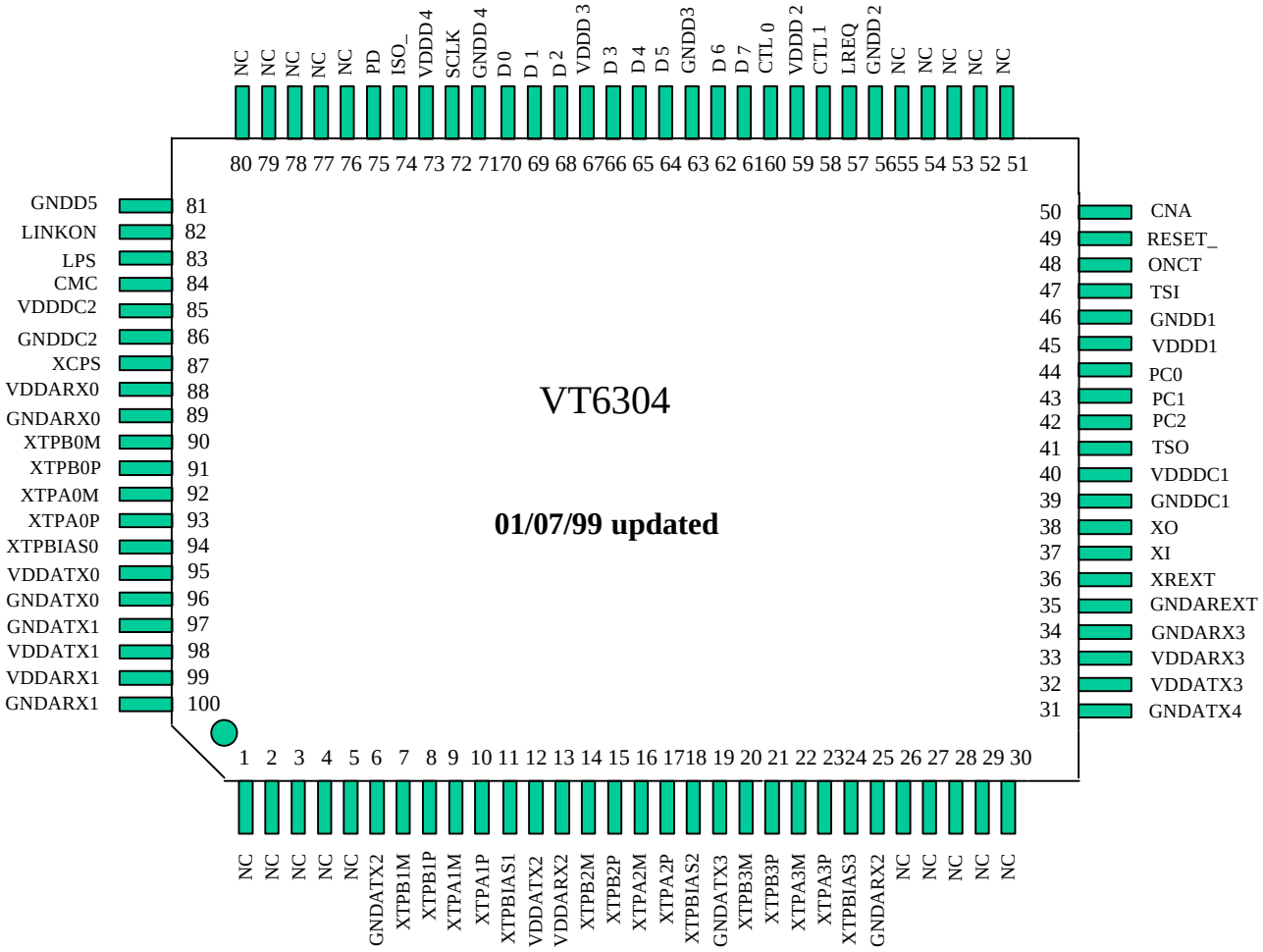



***Figure 1: Functional Block of VT6304***

## Pin Diagram


VT6304
01/07/99 updated
1 NC
2 NC
3 NC
4 NC
5 NC
6 GNDATX2
7 XTPB1M
8 XTPB1P
9 XTPA1M
10 XTPA1P
11 XTPBIAS1
12 VDDATX2
13 VDDARX2
14 XTPB2M
15 XTPB2P
16 XTPA2M
17 XTPA2P
18 XTPBIAS2
19 GNDATX3
20 XTPB3M
21 XTPB3P
22 XTPA3M
23 XTPA3P
24 XTPBIAS3
25 GNDARX2
26 NC
27 NC
28 NC
29 NC
30 NC
31 GNDATX4
32 VDDATX3
33 VDDARX3
34 GNDARX3
35 GNDAREXT
36 XREXT
37 XI
38 XO
39 GNDDC1
40 VDDDC1
41 TSO
42 PC2
43 PC1
44 PC0
45 VDDD1
46 GNDD1
47 TSI
48 ONCT
49 RESET_
50 CNA
51 NC
52 NC
53 NC
54 NC
55 NC
56 NC
57 GNDD2
58 LREQ
59 CTL1
60 VDDD2
61 CTL0
62 D7
63 D6
64 GNDD3
65 D5
66 D4
67 D3
68 VDDD3
69 D2
70 D1
71 D0
72 GNDD4
73 SCLK
74 VDDD4
75 ISO_
76 PD
77 NC
78 NC
79 NC
80 NC
81 GNDD5
82 LINKON
83 LPS
84 CMC
85 VDDDC2
86 GNDDC2
87 XCPS
88 VDDARX0
89 GNDARX0
90 XTPB0M
91 XTPB0P
92 XTPA0M
93 XTPA0P
94 XTPBIAS0
95 VDDATX0
96 GNDATX0
97 GNDATX1
98 VDDATX1
99 VDDARX1
100 GNDARX1

**PIN DESCRIPTIONS**

| No. | Name | Type | Description |
|---|---|---|---|
| **Link-PHY Interface** | | | |
| 82 | LINKON | O | Link on. Indicates the reception of a link-on packet or port event occurs by asserting a 6.114 MHZ signal. |
| 83 | LPS | I | Link power status. LPS is connected to either the VDD supplying the LINK or to a pulsed output that is active when the LINK is powered for the purpose of monitoring the LINK power status. |
| 57 | LREQ | I | Link request. LREQ is an input from the LINK that requests the PHY to perform some service. |
| 74 | ISO_ | I | Link interface isolation control input. This terminal controls the operation of output differentiation logic on the CTL[0-1] and D[0-7] signals. If an optional isolation barrier is implemented between the VT6304 and LLC the ISO_ pin should be tied low to enable the differentiation logic. If no isolation barrier is implemented, the ISO_ should be tied high to disable differentiation logics. |
| 60, 58 | CTL[0-1] | I/O | Control I/O. the CTLn terminals are bidirectional communications control signals between the PHY and LINK. |
| 70, 69, 68, 66, 65, 64, 62, 61 | D[0-7] | I/O | Data I/O. The D terminals are bidirectional and pass data between the PHY and LINK. |
| 72 | SCLK | O | System clock. SCLK provides a 49.152 MHZ clock signal, which is synchronized with the data transfers to the LINK. |
| **Analog Interface** | | | |
| 93, 10, 17, 22 | XTPA[0-3]P | I/O | Twisted-pair cable A differential positive signal pins. |
| 92, 9 , 16, 22 | XTPA[0-3]M | I/O | Twisted-pair cable A differential negative signal pins. |
| 91, 8, 15, 21 | XTPB[0-3]P | I/O | Twisted-pair cable B differential positive signal pins. |
| 90, 7, 14, 20 | XTPB[0-3]M | I/O | Twisted-pair cable B differential negative signal pins. |
| 94, 11, 18, 23 | XTPBIAS[0-3] | I/O | Twisted-pair bias voltage supply. Provide 1.85V (typical) nominal bias for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that the cable connections is active. Hi-impedance during chip reset or power down. Can be disabled via remote packets or software defined in P1394a Draft 2.0. Each of these pin must be decoupled with a 1-uF capacitor to ground. |
| **Misc.** | | | |
| 87 | XCPS | I | CPS : Cable power status. CPS is normally connected to the cable power through a 11 Kohm/1 KOhm volatge divider. This circuit drivers an internal comparator that detects the presencce of cable power. |

| | | | |
|---|---|---|---|
| 50 | CNA | O | CNA is asserted high when none of the PHY ports are connected to another active port. This circuit remains active during the powerdown mode. |
| 84 | CMC | I | Programable Contender/Bus Manager Capable. It specifies in the Self-ID packet that the node is capable of being a bus manager. |
| 44, 43, 42 | PC[0-2] | I | Power Class. These pins are used to set the three POWER_CLASS bits in the Self-ID packet. They are used to describe the power consumption and source characteristics of the node. PC0, 1, 2 are reflected in the Self-ID packet bits 21, 22, 23, respectively. |
| 47 | TSI | I | Single Self ID packet. If port 4 is unused, i.e, the resistors and capacitors for port 4 are not implemented, there is no need to send the 2nd self ID packet, and the system can get benefit by tying this pin to digital VDD to reduce self ID packet exchange time. |
| 41 | TSO | I | Test pin. Tied to VT6304 digital VDD ring for normal operations. |
| 48 | ONCT | I | On Chip Termination. If the capacitive isolation barrier is implemented between the VT6304 and LLC, tie this pin to VDD will utilize on chip resistors to replace on board 5K Ohms resistors pair for LREQ, CTL[0:1] and D[0:7] at PHY side. The resistors for LPS input at PHY side are also replaced if this pin is tied to VDD. This pin has effects on on-chip terminations only if ISO_ is tied to ground. |
| 75 | PD | I | Power Down. A logic High on this pin turns off all internal cicuitry except the connection detect circuits, which outputs the CNA signal. |
| 49 | RESET_ | I/NC | Reset (active low). The reset pin is connected to an internal 10K ohm resistor and an external 0.1 uF capacitor is used for internal reset generation at power-on. The pin can be left unconnected to save the external capacitors, and then the reset time after power-on ranges from 0.5 ms to 2 ms. This pin can also be driven by an open-drain type driver. |
| 38, 37 | XI, XO | Crystal | Crystal Oscillator, 3.3V. These pins connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shnut capacitors are dependent on the specifications of the cystal used. The resulting frequency variation is +/- 100 ppm. |
| 36, 35 | XREXT, GNDAREXT | I/O | Current setting resistor terminals. A resistor of 6.2 KOhm +/- 0.5% is required for internal operating currents generation. |
| **Power Supply & Ground** | | | |
| 88, 99, 13, 33 | VDDARX | supply | Analog receiver power. A combination of high-frequency decoupling capacitors near these pins are suggested. These pins are seperated from digital power for noise prevention. |
| 89, 100, 25, 24 | GNDARX | supply | Analog receiver ground. These pins are tied together to the low-impedance circuit board ground. |

| | | | |
|---|---|---|---|
| 95, 98, 12, 32 | VDDATX | supply | Analog transmitter power. A combination of high-frequency decoupling capacitors near these pins are suggested. These pins are seperated from digital power for noise prevention. |
| 96, 97, 6, 19, 31 | GNDATX | supply | Analog transmitter ground. These pins are tied together to the low-impedance circuit board ground. |
| 40, 85 | VDDDC | supply | Digital core power. These pin are tied to low-impdance point on the circuit board. |
| 39, 86 | GNDDC | supply | Digital core ground. These pins are tied together to the low-impedance circuit board ground. |
| 45, 59, 67, 73 | VDDD | supply | Digital IO power. These pin are tied to low-impdance point on the circuit board. |
| 46, 56, 63, 71, 81 | GNDD | supply | Digital IO ground. These pins are tied together to the low-impedance circuit board ground. |

## FUNCTIONAL DESCRIPTIONS

### *1. GENERAL DESCRIPTION*

The VT6304 provides three-port physical layer function in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

Data bits to be transmitted through the cable ports are received from the Link on 2/4/8 data lines (D[0:7]), and are latched internally in the VT6304 in synchronization with the 49.152-MHZ system clock. These bits are combined serially, encoded, and transmitted at 98.304 , 196.608 or 393.216 Mbits/S as the outbound data-strobe information stream. During transmission, the encoded data transmitted differential on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two or four parallel transmitted (repeated) out of the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The output of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the VT6304 on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect a debounce delay is incorporated. There is no delay on a cable disconnect.

### *2. NETWORK INTERFACE*

# VT6304 REGISTERS

Definitions and usage for each of the registers listed below are provided on this and the following pages:

### *3. PHY REGISTER MAP FOR THE CABLE ENVIRONMENT*

| address | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 0000b | Physical_ID | | | | | | R | PS |
| 0001b | RHB | IBR | Gap_count | | | | | |
| 0010b | Extended(7) | | | reserved | Total_ports | | | |
| 0011b | Max_speed | | | reserved | Delay | | | |
| 0100b | Link_active | Contender | Jitter | | | Pwr_class | | |
| 0101b | Resume_int | ISBR | Loop | Pwr_fail | Timeout | Port_event | Enab_accel | Enab_multi |
| 0110b | Reserved | | | | | | | |
| 0111b | Page_select | | | reserve | Port_select | | | |
| 1000b | Register0(page_select) | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| 1111b | Register7(page_select) | | | | | | | |

### *3.1. PHY REGISTER FIELDS FOR THE CABLE ENVIRONMENT*

| | size | type | default | description |
|---|---|---|---|---|
| Physical_ID | 6 | r | - | The address of this node determined during self-identification. A value of 63 indicates a malconfigured bus; the link shall not transmit any packets. |
| R | 1 | r | - | When set to one, indicate that this node is the root. |
| PS | 1 | r | - | Cable Power status. |
| RHB | 1 | rw | 0 | Root hold-off bit. When set to one, instructs the PHY to attempt to become the root during the next tree identify process. |
| IBR | 1 | rw | 0 | Initiate bus reset. When set to one, instructs the PHY to initiate a bus reset immediately (without arbitration). This bit causes assertion of the reset state for 166 us and is self-clearing. |
| Gap_count | 6 | rw | 3F | Used to configure the arbitration timer setting in order to optimize gap times according to the topology of the bus. IEEE 1394-1995 4.3.6 |
| Extended | 3 | r | 7 | constant value of seven |
| Total_ports | 5 | r | 3 | the number of ports implemented by this PHY |
| Max_speed | 3 | r | 010 | Indicates the maximum speed this PHY supports;<br>000 - 98.304 Mbit/s<br>001 - 98.304 and 196.608 Mbit/s<br>010 - ... and 393.216 Mbit/s<br>011 - ... and 786.43 Mbit/s<br>100 - nd 1,572.864 Mbit/s<br>101 - nd 3,145.728 Mbit/s<br>all other values are reserved for future definition |

| | | | | |
|---|---|---|---|---|
| Delay | 4 | R | 0 | Worse case repeater delay, expressed as 144+(delay*20)ns. |
| Link_active | 1 | rw | 1 | Link enabled. Default value of one subsequent to a power reset. Otherwise cleared or set by software to control the value of the L bit transmitted in the self-ID packet. The transmitted L bit shall be the logical AND of this bit and the LPS signal. |
| Contender | 1 | rw | Pin C/LKON | Contender. Cleared or set by software to control the value of the C bit transmitted in the self-ID packet. |
| Pwr_class | 3 | rw | Pin PC0-PC2 | Power class. Controls the value of the pwr field transmitted in the self-ID packet.<br>000 - Node does not need power and does not repeat power<br>001 - Node is self-powered and provides a minimum of 15 W to the bus<br>010 - Node is self-powered and provides a minimum of 30 W to the bus.<br>011 - Node is self-powered and provides a minimum of 45 W to the bus<br>100 - Node may be powered from the bus and is using up to 1 W.<br>101 - Node is powered from the bus and is using up to 1 W. An additional 2 W is needed to enable the link and higher layers.<br>110 - Node is powered form the bus and is using up to 1 W. An additional 5 W is needed to enable the link and higher layers.<br>111 - Node is powered from the bus and is using up to 1 W. An additional 9 W is needed to enable the link and higher layers. |
| Jitter | 3 | R | 0 | The difference between the fastest and slowest repeater data delay, expressed as (jitter+1)*20ns |
| Resume_int | 1 | Rw | 0 | Resume interrupt enable. When set to one, the PHY shall set port_event to one if resume operations commence for any port. |
| ISBR | 1 | rw | 0 | Initiate short (arbitrated) bus reset. A write of one to this bit instructs the PHY to arbitrate and issue a short bus reset. This bit is self-clearing. |
| Loop | 1 | rw | 0 | Loop detect. A write of one to this bit clears it to zero. |
| Pwr_fail | 1 | rw | 0 | Cable power failure detect. Set to one when the PS bit changes from one to zero. A write of one to this bit clears it to zero. |
| Timeout | 1 | rw | 0 | Arbitration state machine timeout. A write of one to this bit clears it to zero. |
| Port_event | 1 | rw | 0 | Port event detect. The PHY sets this bit to one if any of connected, Bias, Disabled or Fault change for a port whose Int_enable bit is one. The PHY also sets this bit to one if resume operations commence for any port and Resume_int is one. A write of one to this bit clears it to zero. |
| Enab_accel | 1 | rw | 0 | Enable arbitration acceleration. When set to one, the PHY shall use the enhancements specification in P1394A. |
| Enab_multi | 1 | rw | 0 | Enable multi-speed packet concatenation. When set to one, the Link shall signal the speed of all packets to the PHY. |
| Page_select | 3 | rw | 000 | Selects which of eight possible PHY register pages are accessible through the window at PHY register address 1000b through 1111b, inclusive. |
| Port_select | 4 | rw | 0000 | If the page selected by Page_select presents per port information, this field selects which port's registers are accessible through the window at PHY |

| | | | | |
|---|---|---|---|---|
| | | | | register addressed 1000b through 1111b, inclusive. |

### *3.2. PHY REGISTER PAGE0: PORT STATUS PAGE*

The port Status page is used to access configuration and status information for each of the PHY's port. The port is selected by writing zero to Page_select and the desired port number to Port_select in the PHY register at address 0111.

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 1000b | AStat | | BStat | | Child | connected | Bias | Disabled |
| 1001b | Negotiated_speed | | | Int_enable | Fault | | | |
| 1010b | | | | | | | | |
| 1011b | | | | | | | | |
| 1100b | | | | | | | | |
| 1101b | | | | | | | | |
| 1110b | | | | | | | | |
| 1111b | | | | | | | | |

### *3.3. PHY REGISTER PORT STATUS PAGE FIELDS*

| | Size | Type | default | Description |
|---|---|---|---|---|
| Astat | 2 | r | - | TPA line State for the port<br>00 = invalid<br>01 =1<br>10 =0<br>11 =z |
| Bstat | 2 | r | - | (same encoding as Astat) |
| Child | 1 | r | - | If equal to one, the port is a child, else a parent. The meaning of this bit is undefined from the time a bus reset is detected until the PHY transitions to state T1:Child Handshake during the tree identify process(see 4.4.2.2 in IEEE Std 1394-1995) |
| Conncted | 1 | r | 0 | If equal to one, the port is connected, else disconnected. The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed. |
| Bias | 1 | r | - | If equal to one, bias voltage is detected( possible connection). The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed. |
| Disabled | 1 | rw | 0 | When set to one, the port shall be disabled. The value of this bit subsequent to a power reset is implementation-dependent, but should be a strappable option. |
| Negotiated_speed | 3 | r | - | Indicated the maximum speed negotiated between this PHY port and its immediately connected port; the encoding is<br>000 – 98.304Mbit/s<br>001 - and 196.608 Mbit/s |

| | | | | |
|---|---|---|---|---|
| | | | | 010 - and 393.216 Mbit/s |
| Int_Enable | 1 | rw | 0 | Enable port event interrupts. When set to one, the PHY shall set Port_event to one if any of Connected, Bias, Disabled or Fault (for this port) change state. |
| Fault | 1 | Rw | 0 | Set to one if an error is detected during a suspend or resume operation. A write of one to this bit clears it to zero. |

### *3.4. PHY REGISTER PAGE 1: VENDOR IDENTIFICATION PAGE*

The Vendor Identification page is used to identify the PHY's vendor and compliance level. The page is selected by writing one to Page_select in the PHY register at address 0111.

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 1000b | Compliance_level | | | | | | | |
| 1001b | Reserved | | | | | | | |
| 1010b | Vendor_ID | | | | | | | |
| 1011b | | | | | | | | |
| 1100b | | | | | | | | |
| 1101b | Product_ID | | | | | | | |
| 1110b | | | | | | | | |
| 1111b | | | | | | | | |

### *3.5. PHY REGISTER VENDOR IDENTIFICATION PAGE FIELDS*

| | Size | Type | Description |
|---|---|---|---|
| Compliance_level | 8 | R | Standard to which the PHY implementation complies:<br>0 = not specified<br>1 = IEEE P1394a<br>All other values reserved for future standardization. The default is "1". |
| Vendor_ID | 24 | R | The company ID or Organizationally Unique Identifier (OUI) of the manufacturer of the PHY. The most significant byte of Vendor_ID appears at PHY register location 1010 and the least significant at 1100. The default value is "00 40 63". |
| Product_ID | 24 | R | The meaning of this number is determined by the company or organization that has been granted Vendor_ID. The most significant byte of Product_ID appears at PHY register location 1101 and the least significant at 1111. The default value is "30 60 00". |

### *3.6. PHY REGISTER PAGE 7: VENDOR-DEPENDENT PAGE*

The vendor-dependent page provides registers set aside for use by the PHY's vendor. The page is selected by writing seven to Page_select in the PHY register at address 0111. **Don't access the registers "used for test"**.

| address | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 1000b | used for test | | | | | | | |

| | | |
|---|---|---|
| 1001b | used for test | |
| 1010b | used for test | |
| 1011b | used for test | |
| 1100b | used for test | |
| 1101b | used for test | |
| 1110b | Link_Speed | Reserved |
| 1111b | used for test | |

### *3.7. PHY REGISTER VENDOR DEPENDENT PAGE FIELDS*

| | Size | Type | Description |
|---|---|---|---|
| Link_Speed | 2 | RW | Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows :<br><br>This field has the effect on the self-ID packets as well as the PHY speed capability which is exchanged between peer PHY during self-ID state. This field is set to 10b (S400) by hardware reset and is unchanged by bus-reset. |
| Vendor_ID | 24 | R | The company ID or Organizationally Unique Identifier (OUI) of the manufacturer of the PHY. The most significant byte of Vendor_ID appears at PHY register location 1010 and the least significant at 1100. The default value is “00 e0 4c”. |
| Product_ID | 24 | R | The meaning of this number is determined by the company or organization that has been granted Vendor_ID. The most significant byte of Product_ID appears at PHY register location 1101 and the least significant at 1111. The default value is “88 01 00”. |

# 4 ELECTRICAL CHARACTERISTICS

## 4.1 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage (OVDD) | -0.3 V to +3.6 V |
| Supply Voltage (OVDD_AUX) | -0.3 V to +3.6 V |
| DC Output Voltage (VOUT) | -0.3 V to VDD+0.3V |
| Storage Temperature Range ($T_{STG)}$ | -40°C to 125°C |
| Ambient Temperature (TA) | 0 to 70°C |
| Lead Temp. (TL) (Soldering, 10 sec) | 250°C |
| ESD Rating ($R_{ZAP = 1.5k, CZAP = 120 pF)}$ | 2.0 KV |
| Input Latchup Current | +/- 25mA |
| Package Power Dissipation | 3.0Watt@$25^0$C |

## 4.2 RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply voltage $V_{DD}$ | | 3.3 Volts ± 5% |
| Supply voltage $V_{DD}$ | | 3.3 Volts ± 5% |
| Supply Current ($I_{DD}$) | D0 State | |
| Supply Current ($I_{DD\_AUX}$) | D0 State | |
| Supply Current ($I_{DD\_AUX}$) | D3cold and PME Enable State | |
| Supply Current ($I_{DD\_AUX}$) | D3cold and PME Disable State | |
| Supply Current ($I_{DD}$) | Low Power Mode | |
| Supply Current ($I_{DD\_AUX}$) | Low Power Mode | |

## 5.3 DC Electrical characteristics

### 4.3.1 Link PHY Interface DC Specification

Unless otherwise noted, all test conditions ate as follows:

Table 1. DC Characteristics

Functional Operating Range ($V_{REF}$ = 5V ± 5%, $V_{CC}$ = 3.3V ± 0.3V, $T_{CASE}$ = 0 to +85 )

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{IL1}$ | Input Low Voltage | | 0.9 | V | 1 |
| $V_{IH1}$ | Input High Voltage | 2.4 | | V | 1 |
| $V_{IL2}$ | Input Low Voltage | | 1.1 | V | 1 |
| $V_{IH2}$ | Input High Voltage | 2.2 | | V | 1 |
| $V_{IL3}$ | Input Low Voltage | | 1.1 | V | 1 |
| $V_{IH3}$ | Input High Voltage | 2.2 | | V | 1 |
| $V_{IL4}$ | Input Low Voltage | | 0.9 | V | 1 |
| $V_{IH4}$ | Input High Voltage | 2.1 | | V | 1 |
| $V_{OL1}$ | Output Low Voltage | | 0.1Vcc | V | 1 |
| $V_{OH1}$ | Output High Voltage | 0.9Vcc | | V | 1 |
| $V_{OL2}$ | Output Low Voltage | | 0.1Vcc | V | 1 |
| $V_{OH2}$ | Output High Voltage | 0.9Vcc | | V | 1 |
| $I_{OL1}$ | Output Low Current | 9.0 | 18.7 | mA | 1, @ $V_{OL1}$ |
| $I_{OH1}$ | Output High Current | 8.2 | 16.2 | mA | 1, @ $V_{OH1}$ |
| $I_{OL2}$ | Output Low Current | 8.5 | 17.8 | mA | 1, @ $V_{OL2}$ |
| $I_{OH2}$ | Output High Current | 7.7 | 15.4 | mA | 1, @ $V_{OH2}$ |
| $I_{LI1}$ | Input Leakage Current | | 50 | A | |
| $I_{LI2}$ | Hi-Z State Data Line Leakage | | 50 | A | (0V < $V_{IN}$ < 3.3 V) |
| $C_{IN}$ | Input Capacitance | | 12 | pF | $F_C$ = 1MHz |
| $C_{OUT}$ | Output Capacitance | | 12 | pF | $F_C$ = 1MHz |
| $C_{I/O}$ | I/O Capacitance | | 12 | pF | $F_C$ = 1MHz |

NOTES:

1. Refer to table 2 for the signals associated with this specification.

Table 2. DC Characteristic Signal Association (Sheet 1 of 2)

| Symbol | Associated Signals |
|---|---|
| $V_{IL1}$ / $V_{IH1}$ | **** Input Type 1 (1394) ****<br>CNA, CTL[0:1], D[0:7], LINKON, LREQ, SCLK |
| $V_{IL2}$ / $V_{IH2}$ | **** Input Type 2 ****<br>CMC, ISO_, ONCT, PC[0:2], TSI, TSO |
| $V_{IL3}$ / $V_{IH3}$ | **** Input Type 3 ****<br>LPS, PD |
| $V_{IL4}$ / $V_{IH4}$ | **** Input Type 4 ****<br>RESET_ |
| $V_{OL1}$ / $V_{OH1}$ | **** Output Type 1 ****<br>CNA, CTL[0:1], D[0:7], LINKON, LREQ, SCLK |
| $V_{OL2}$ / $V_{OH2}$ | **** Output Type 2 ****<br>CMC, ISO_, ONCT, PC[0:2], TSI, TSO |
| $I_{OL1}$ / $I_{OH1}$ | **** Output Type 1 ****<br>CNA, CTL[0:1], D[0:7], LINKON, LREQ, SCLK |
| $I_{OL2}$ / $I_{OH2}$ | **** Output Type 2 ****<br>CMC, ISO_, ONCT, PC[0:2], TSI, TSO |

Table 3. DC Current Characteristic

Functional Operating Range ($V_{REF}$ = 5V ± 5%, $V_{CC}$ = 3.3V ± 0.3V, $T_{CASE}$ = 0 to +85 )

| Symbol | Parameter | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| $I_{CC}$(3v) | $V_{CC}$ Supply Current | 110 | 155 | mA | |
| $I_{CC}$(SUS) ON | Suspend Well Supply Current – Full On | 3 | 5 | mA | |
| $I_{CC}$(SUS) POS/STR | Suspend Well Supply Current – Power On Suspend or Suspend to RAM | 30 | 150 | A | |
| $I_{CC}$(SUS) STD/Soff | Suspend Well Supply Current – Suspend to Disk or Soft Off | 9 | 150 | A | |

### 4.3.3 Analog Signals DC Specification

Unless otherwise noted, all test conditions ate as follows:

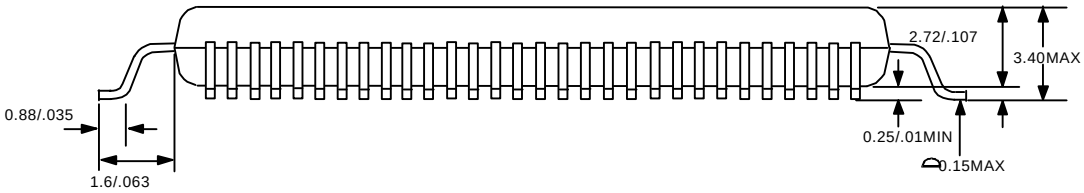
1. $T_A$ = 0 to +70$^0$C
2. $V_{CC}$ = 3.3V +/- 10%
3. 24.576 Mhz +/- 0.01%
4. REXT = 6.2 K +/- 1%, no load

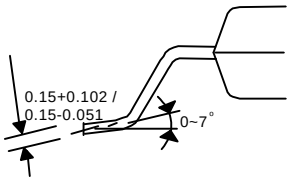
| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | OSCIN | | | 1.5 | Volt |
| $V_{IH}$ | Input High Voltage | OSCIN | 3.5 | | | Volt |
| $I_{IL}$ | Input Low Current | $V_{IN}$=GND. OSCIN | | | -150 | µA |
| $I_{IH}$ | Input High Current | $V_{IN}$=VCC. OSCIN | | | 150 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$= -4 mA TPO± | | | 0.4 | Volt |
| | | $I_{OL}$= -20 mA, PLED[3:0]# | | | 1 | Volt |
| $V_{OH}$ | Output High Voltage | $I_{OH}$= 4 mA TPO± | $V_{CC}$-1.0 | | | Volt |
| | | $I_{OH}$= 4 µA PLED[3:2]# | $V_{CC}$-1.0 | | | Volt |
| | | $I_{OH}$= 6 µA PLED[1:0]# | 2.4 | | | Volt |
| $C_{IN}$ | Input Capacitance | | | 5 | | pF |
| $I_{CC}$ | $V_{CC}$ Supply Current | Transmitting, 100Mbps, 4 portss | | | 170 | mA |
| | | Transmitting, 200Mbps, 4 ports | | | 220 | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Transmitting, 400 Mbps, 4 ports | | | 280 | mA |
| | | Powerdown Mode | | | 0.1 | mA |

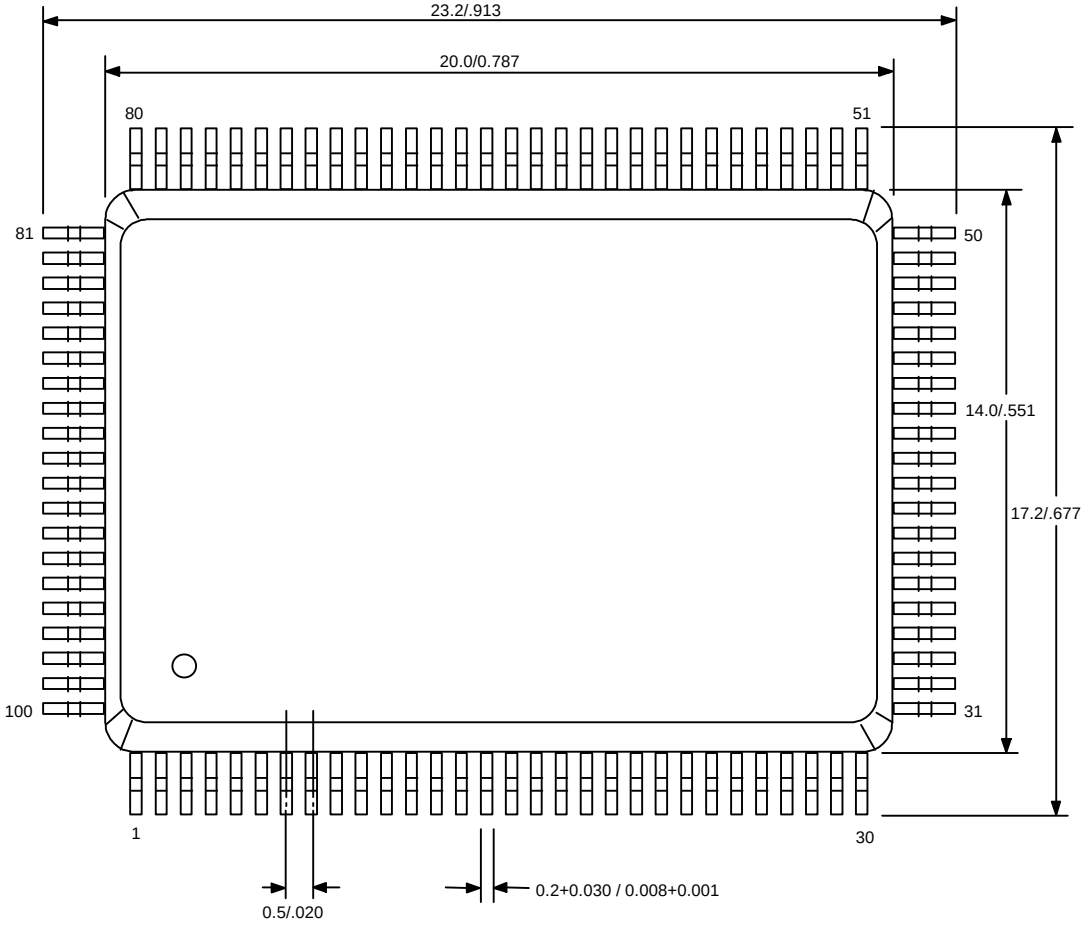
## Package Diminsion

Unit Millimeter/Inch




Unit Millimeter/Inch



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