

**RICOH**

RICOH CORP/ ELECTRONIC

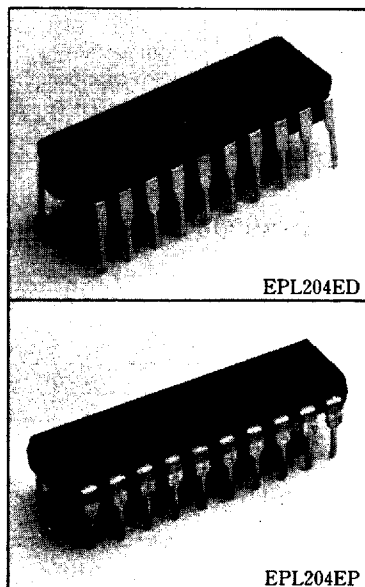
EK-025-8902

**CMOS ELECTRICALLY  
PROGRAMMABLE LOGIC****EPL204ED/EP****■ OUTLINE**

The EPL204 is a field programmable logic array manufactured by using CMOS EPROM processes. It is a programmable "and" fixed "or" array with registered outputs in the 26P8 configuration.

Programming is possible with popular PAL<sup>®</sup> programmers such as Data I/O or Ricoh's IBM P.C. Writer. Programming is similar to all EPROM Devices. Development of CMOS Gate Arrays using one or more of those devices to support larger I/O's is simple and immediate using off the shelf plastic OTP (One Time Programmable) devices.

Input/Output configurations are flexible using 8 programmable macro cells. Feedback, combinatorial or registered outputs and polarity are user definable. Register clocks can be from the internal array or on the conventional external Pin 1 clock terminal.



EPL204ED

EPL204EP

**■ FEATURES**

- Low power consumption and high reliability characteristics of the CMOS-EPROM process
- 20 Pin DIP Plastic OTP (EPL 204EP 300 mil) 20 Pin Window DIP with window (EPL 204ED 300 mil)
- Ultra Violet Reprogramming with window packages – 1000 reprogram cycles
- Data copy protection
- Input/Output propagation delay 25ns maximum
- Flexible I/O capability using I/O macro cells
  - A. Selection of combinational or registered outputs
  - B. Selection of output enable (External  $\overline{OE}$ , Internal OE)
  - C. Polarity of outputs
  - D. Clock selection (external or internal)
  - E. Asynchronous resets (AR1, AR2)
  - F. Synchronous presets (SP1, SP2)

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## ■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Rating	Unit
V <sub>cc</sub>	V <sub>cc</sub> Supply Voltage	with respect to GND	-0.3 ~ 7.0	V
V <sub>pp</sub>	V <sub>pp</sub> Supply Voltage		-0.3 ~ 14.5	V
V <sub>i</sub>	Input Voltage		-0.3 ~ V <sub>cc</sub> + 0.3	V
V <sub>o</sub>	Output Voltage		-0.3 ~ V <sub>cc</sub> + 0.3	V
P <sub>d</sub>	Maximum Power Consumption	T <sub>a</sub> = 25°C	0.8	W
T <sub>opr</sub>	Operating Ambient Temperature		-20 ~ 85	°C
T <sub>stg</sub>	Storage Temperature		-40 ~ 125	°C

## ■ RECOMMENDED OPERATING CONDITION (T<sub>a</sub> = 0 ~ 70°C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V <sub>cc</sub>	Supply Voltage	4.75	5.0	5.25	V
V <sub>IH</sub>	"H" Input Voltage	2.0		V <sub>cc</sub> + 0.3	V
V <sub>IL</sub>	"L" Input Voltage	-0.3		0.8	V

## ■ CAPACITANCE

Symbol	Parameter	Condition	Specified Value			Unit
			Min.	Typ.	Max.	
	Input Pin	f = 1 MHz, V <sub>cc</sub> = 0V		5		pF
	I/O Pin			8		
	V <sub>pp</sub> Pin			10		

## ■ D.C. CHARACTERISTICS (T<sub>a</sub> = -20 ~ 85°C V<sub>cc</sub> = 5V ± 5%)

Symbol	Parameter	Condition	Specified Value			Unit
			Min.	Typ.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>in</sub> = 0V ~ V <sub>cc</sub>	-20		20	μA
I <sub>LO</sub>	Output Leakage Current for OFF State	V <sub>o</sub> = 0V ~ V <sub>cc</sub>	-20		20	μA
V <sub>IL</sub>	"L" Input Voltage		-0.3		0.8	V
V <sub>IH</sub>	"H" Input Voltage		2.0		V <sub>cc</sub> + 0.3	V
V <sub>OL</sub>	"L" Output Voltage	V <sub>cc</sub> = MIN I <sub>oL</sub> = 8 mA			0.5	V
V <sub>OH</sub>	"H" Output Voltage	V <sub>cc</sub> = MIN I <sub>oH</sub> = -3.2mA	2.4			V
I <sub>cc1</sub>	Power Supply Current (Standby)	V <sub>cc</sub> = MAX f = 0 MHz V <sub>in</sub> = GND or V <sub>cc</sub>			60	mA
I <sub>cc2</sub>	Power Supply Current (Operation)	V <sub>cc</sub> = MAX f = 10 MHz V <sub>in</sub> = GND or V <sub>cc</sub>			70	mA

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## ■ AC CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 5V ± 5%)

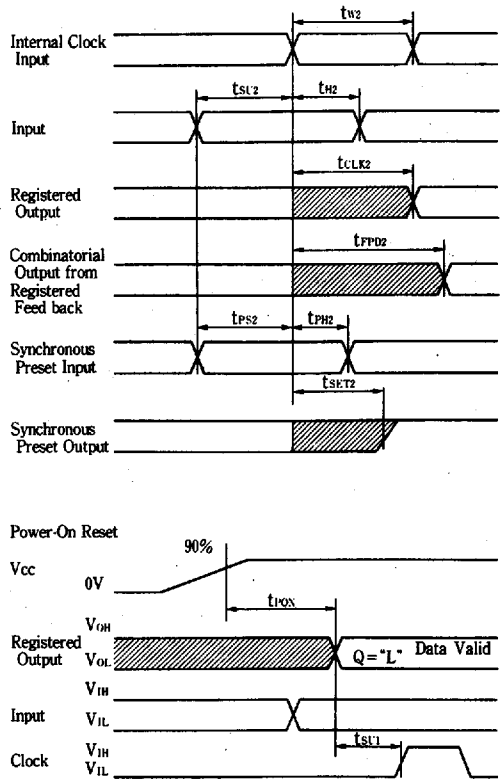
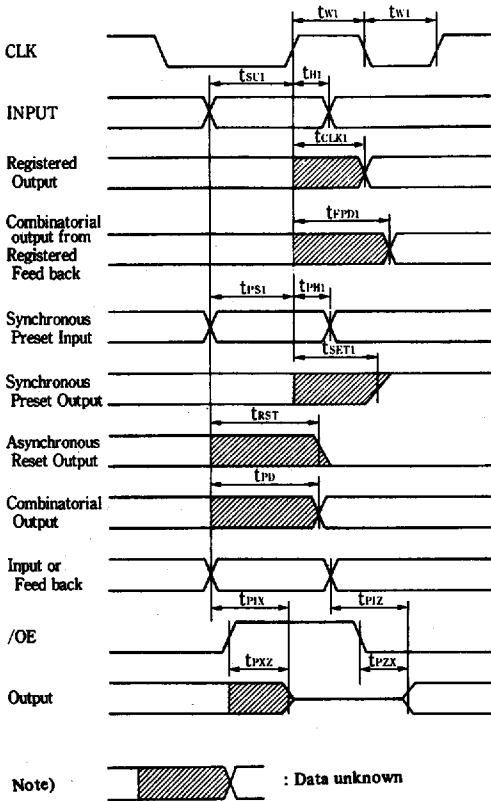
Symbol	項 Parameter 目		Condition	Specified Value			Unit
	Clock	Parameters		Min	Typ	Max	
t <sub>PD</sub>	External Clock	Input or I/O input to non-registered output	CL=50pF R1=560Ω R2=1.1KΩ			25	nS
t <sub>PIX</sub>		Input or I/O input to output disable				25	nS
t <sub>PIZ</sub>		Input or I/O input to output enable				25	nS
t <sub>PXZ</sub>		/OE (pin 11) to output disable				20	nS
t <sub>PZK</sub>		/OE (pin 11) to output enable				20	nS
t <sub>SU1</sub>		Input or I/O input setup time			18		nS
t <sub>H1</sub>		Input or I/O input hold time			0		nS
t <sub>CLK1</sub>		Clock to output delay				15	nS
t <sub>F<sub>PD1</sub></sub>		Clock to non-registered output from registered feed back				35	nS
t <sub>W1</sub>		External clock width			15		nS
t <sub>PS1</sub>		CLK (1pin) Synchronous preset input setup time			18		nS
t <sub>SET1</sub>		Clock to register preset				15	nS
t <sub>RST</sub>		Input or I/O input to asynchronous reset				25	nS
t <sub>P1</sub>		Minimum clock period (t <sub>SU1</sub> + t <sub>CLK1</sub> )				33	nS
f <sub>1</sub>		Maximum frequency (1/t <sub>P1</sub> )			30		MHz
t <sub>PH1</sub>	Synchronous preset input hold time		0		nS		
t <sub>SU2</sub>	Internal Clock	Input or I/O input setup time	CL=50pF R1=560Ω R2=1.1KΩ	5		nS	
t <sub>H2</sub>		Input or I/O input hold time		10		nS	
t <sub>CLK2</sub>		Clock P.T. input to output delay				30	nS
t <sub>F<sub>PD2</sub></sub>		Clock P.T. input to non-registered output from registered feed back				50	nS
t <sub>W2</sub>		Clock P.T. input width			15		nS
t <sub>PS2</sub>		Synchronous preset input set up time			5		nS
t <sub>SET2</sub>		Clock P.T. input to register preset				30	nS
t <sub>P2</sub>		Minimum Clock period (t <sub>SU2</sub> + t <sub>CLK2</sub> )				35	nS
t <sub>PH2</sub>		Synchronous preset input hold time			10		nS
f <sub>2</sub>		Maximum frequency (1/t <sub>P2</sub> )			28.6		MHz
t <sub>PON</sub>		Power on reset time		45		μS	

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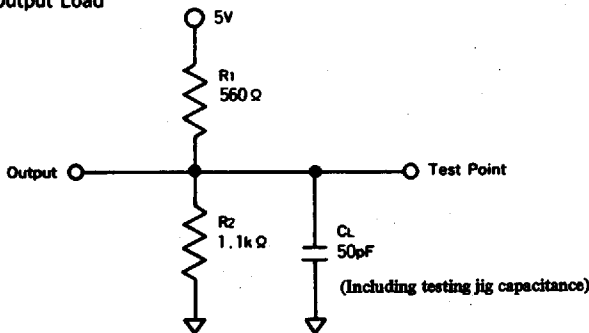
■ TIMING CHART

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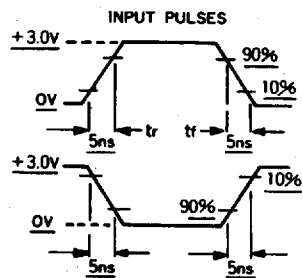


Note) : Data unknown

Output Load



Input Waveform



NOTE : This is the A.C. characteristic measurement with a voltage of 1.5V on both the input and output.

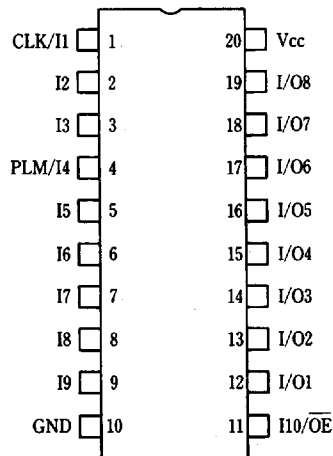
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## ■ PIN DESCRIPTION

PIN No.	PIN Name		Function	
	Logic Mode	Program Mode	Logic Mode	Program Mode
1	CLK/I1	Vpp	Input	Clock
2	I2	CA4		Programming Power Supply
3	I3	CA3		
4	PLM/I4	CA2		
5	I5	CA1		
6	I6	CA0		Row Address Input
7	I7	RA5		
8	I8	RA4		
9	I9	NC		NC
10	GND	GND		GND
11	I10/OE	PGM/OE	Input/Output Enable	Programming Control/Output Enable
12	I/O1	D0	Input/Output	DATA Input/Output
13	I/O2	D1		
14	I/O3	D2		
15	I/O4	D3		
16	I/O5	RA3		Row Address Input
17	I/O6	RA2		
18	I/O7	RA1		
19	I/O8	RA0		
20	Vcc	Vcc	Vcc	Vcc

## ■ PIN CONFIGURATION

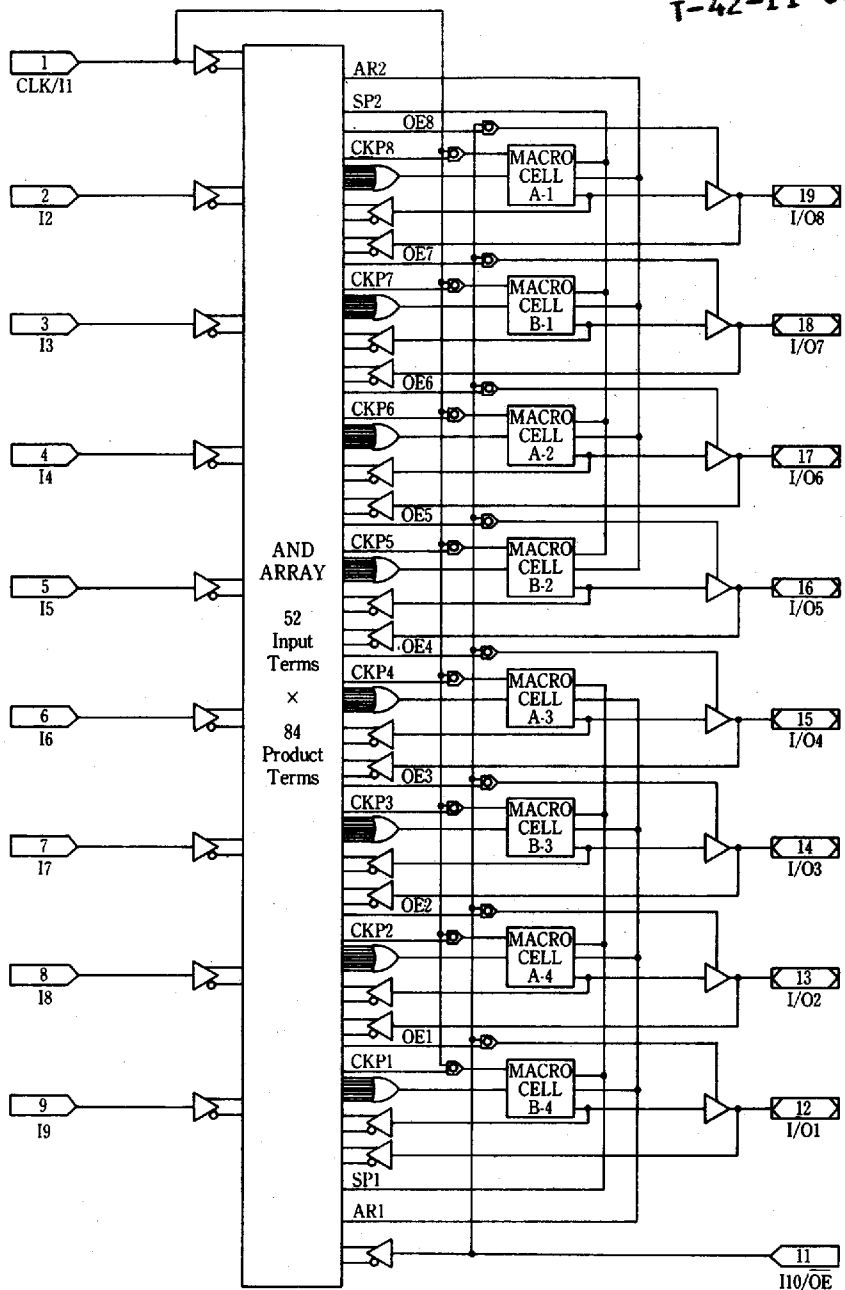


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■ BLOCK DIAGRAM

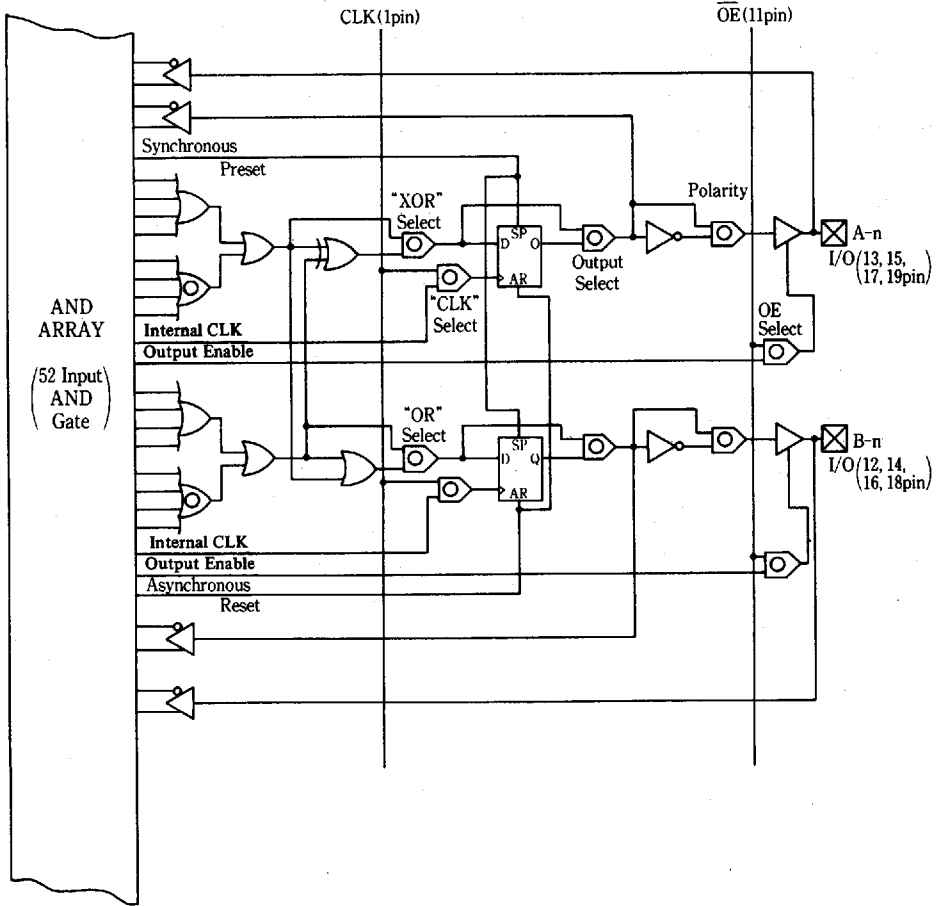
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■ MACRO I/O CELL

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## ■ FUNCTIONS AND OPERATIONS

The EPL204 is an electrically reprogrammable logic array. The configuration of the EPL204 is 52 input terms (18 external inputs and 8 feedbacks).

All inputs are TTL levels. Control of all registers for asynchronous and synchronous operation and output polarity is user definable.

All product terms and input terms to the "AND" array have ultra violet EPROM cells connections. In the unprogrammed state all intersections are connected.

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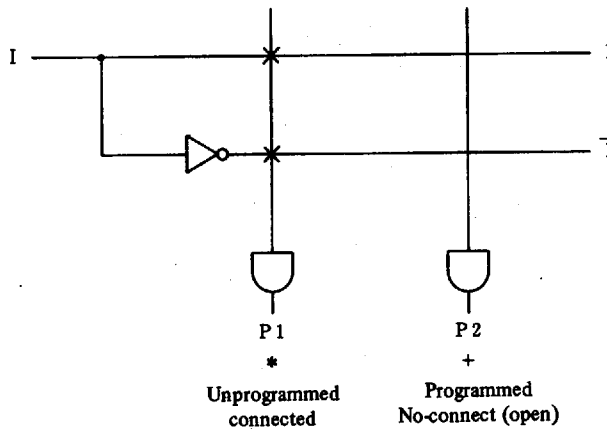


Fig. 1

All macro I/O cells have "XOR" or "OR" selections and output polarity selections.

## (1) "OR"/"XOR" select

Eight product terms are ORed or XORed or fed straight through to each output.



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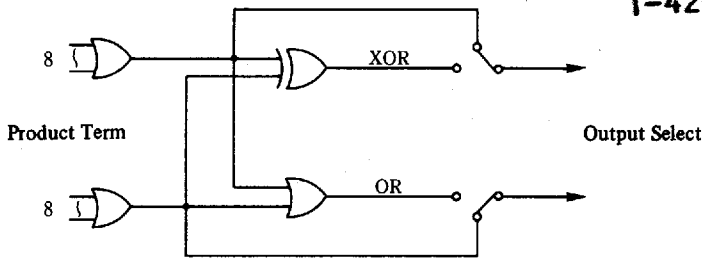


Fig. 2 "OR" "XOR" Select

**(2) OE select**

Each macro cell can be selected via pin 11 or from the internal product term.

**(3) Output select, CLK select**

CLK select of each macro cell register can be clocked from the conventional CLK (pin 1) or from an internal clock out of the array. Each register has a synchronous preset and an asynchronous reset.

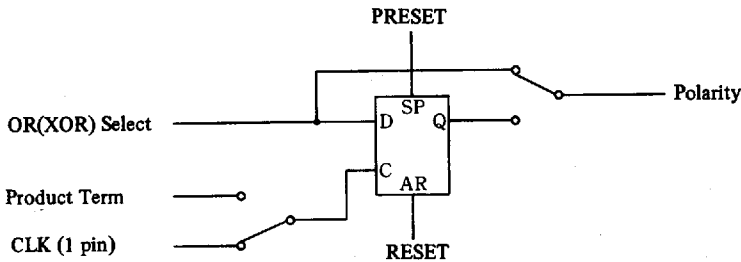


Fig. 3 Output Select, CLK Select

**(4) Polarity**

You can select the polarity of the output signal.

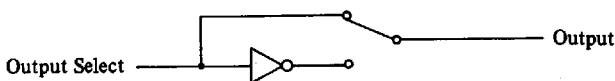


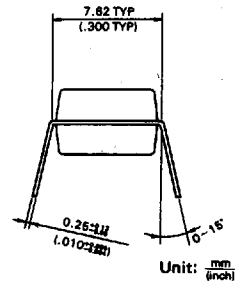
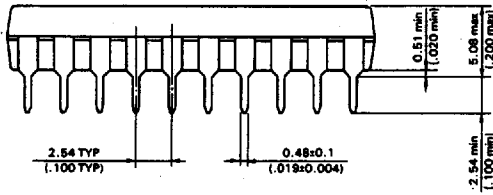
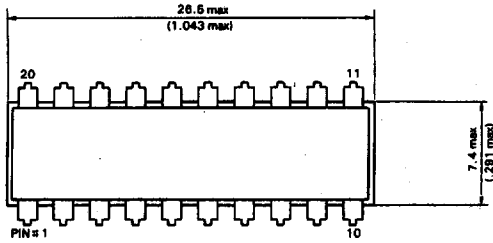
Fig. 4 Polarity

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■ PACKAGE DIMENSION

- Mold DIP Package (DIP-20-P1)

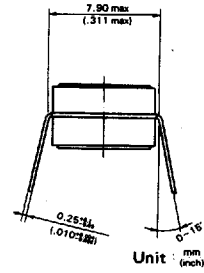
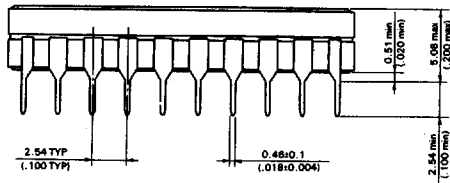
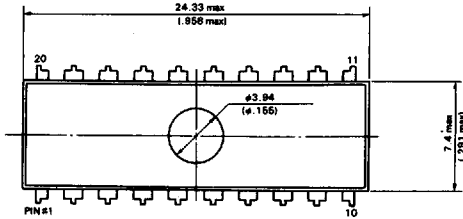
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● CER DIP Package  
(DIP-20-G1)

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