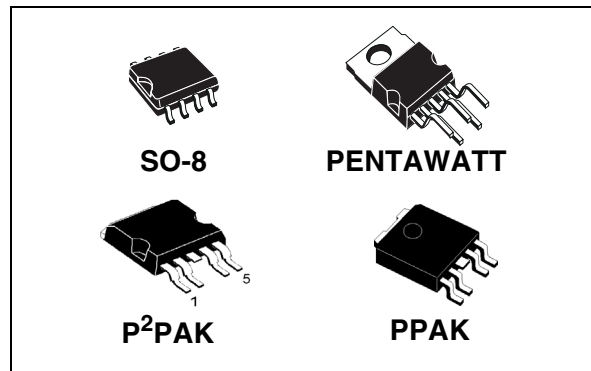


Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN750 VN750S VN750PT VN750-B5	60 m Ω	6 A	36 V

- CMOS compatible input
- On state open load detection
- Off state open load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low stand-by current
- Reverse battery protection (see [Application schematic](#))


Description

The VN750 is a monolithic device designed in STMicroelectronic's VIPower M0-3 Technology. The VN750 is intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects the open load condition in both the on and off state. In the off state the device detects if the output is shorted to V_{CC} . The device automatically turns off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PENTAWATT	VN750	-
SO-8	VN750S	VN750S13TR
P ² PAK	VN750-B5	VN750-B513TR
PPAK	VN750PT	VN750PT13TR

Contents

- 1 Block diagram and pin description 6**

- 2 Electrical specifications 7**
 - 2.1 Absolute maximum ratings 7
 - 2.2 Thermal data 8
 - 2.3 Electrical characteristics 9
 - 2.4 Electrical characteristics curves 15
 - 2.5 GND protection network against reverse battery 18
 - 2.5.1 Solution 1: resistor in the ground line (RGND only) 18
 - 2.5.2 Solution 2: diode (DGND) in the ground line 19
 - 2.6 Load dump protection 19
 - 2.7 MCU I/Os protection 19
 - 2.8 Open load detection in Off state 19
 - 2.9 SO-8 maximum demagnetization energy (VCC = 13.5V) 21
 - 2.10 PPAK/P²PAK maximum demagnetization energy (VCC=13.5V) 22

- 3 Package and PCB thermal data 23**
 - 3.1 SO-8 thermal data 23
 - 3.2 P²PAK thermal data 25
 - 3.3 PPAK thermal data 28

- 4 Package and packing information 31**
 - 4.1 ECOPACK[®] packages 31
 - 4.2 SO-8 package information 31
 - 4.3 PENTAWATT mechanical data 33
 - 4.4 P²PAK mechanical data 35
 - 4.5 PPAK mechanical data 37
 - 4.6 SO-8 packing information 39
 - 4.7 PENTAWATT packing information 40
 - 4.8 P²PAK packing information 40
 - 4.9 PPAK packing information 41

- 5 Revision history 43**

List of tables

Table 1.	Device summary	1
Table 2.	Suggested connections for unused and not connected pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data	8
Table 5.	Power	9
Table 6.	Switching ($V_{CC}=13V$)	9
Table 7.	Input pin	10
Table 8.	V_{CC} output diode.	10
Table 9.	Status pin	10
Table 10.	Protections	10
Table 11.	Open load detection	11
Table 12.	Truth table.	12
Table 13.	Electrical transient requirements on V_{CC} pin	13
Table 14.	Thermal parameter	25
Table 15.	Thermal parameter	27
Table 16.	Thermal parameter	30
Table 17.	SO-8 mechanical data	32
Table 18.	PENTAWATT mechanical data	33
Table 19.	P ² PAK mechanical data	36
Table 20.	PPAK mechanical data	37
Table 21.	Document revision history	43

List of figures

Figure 1.	Block diagram	6
Figure 2.	Configuration diagram (top view)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	Status timings	11
Figure 5.	Switching time waveforms	11
Figure 6.	Waveforms	14
Figure 7.	Off state output current	15
Figure 8.	High level input current	15
Figure 9.	Input clamp voltage	15
Figure 10.	Status leakage current	15
Figure 11.	Status low output voltage	15
Figure 12.	Status clamp voltage	15
Figure 13.	On state resistance Vs T_{case}	16
Figure 14.	On state resistance Vs V_{CC}	16
Figure 15.	Open load On state detection threshold	16
Figure 16.	Input high level	16
Figure 17.	Input low level	16
Figure 18.	Input hysteresis voltage	16
Figure 19.	Overvoltage shutdown	17
Figure 20.	Openload Off state voltage detection threshold	17
Figure 21.	Turn-on voltage slope	17
Figure 22.	Turn-off voltage slope	17
Figure 23.	I_{lim} Vs T_{case}	17
Figure 24.	Application schematic	18
Figure 25.	Open load detection in Off state	20
Figure 26.	SO-8 maximum turn-off current versus inductance	21
Figure 27.	PPAK /P ² PAK maximum turn-off current versus inductance	22
Figure 28.	PC board	23
Figure 29.	Rthj-amb Vs. PCB copper area in open box free air condition	23
Figure 30.	SO-8 thermal impedance junction ambient single pulse	24
Figure 31.	Thermal fitting model of a single channel	24
Figure 32.	PC board	25
Figure 33.	Rthj-amb Vs. PCB copper area in open box free air condition	26
Figure 34.	P ² PAK thermal impedance junction ambient single pulse	26
Figure 35.	Thermal fitting model of a single channel	27
Figure 36.	PC board	28
Figure 37.	Rthj-amb Vs. PCB copper area in open box free air condition	28
Figure 38.	PPAK thermal impedance junction ambient single pulse	29
Figure 39.	Thermal fitting model of a single channel	29
Figure 40.	SO-8 package dimensions	31
Figure 41.	PENTAWATT package dimensions	33
Figure 42.	P ² PAK package dimensions	35
Figure 43.	PPAK package dimensions	37
Figure 44.	SO-8 tube shipment (no suffix)	39
Figure 45.	SO-8 tape and reel shipment (suffix "TR")	39
Figure 46.	PENTAWATT tube shipment (no suffix)	40
Figure 47.	P2PAK tube shipment (no suffix)	40
Figure 48.	P ² PAK tape and reel (suffix "13TR")	41

Figure 49. PPAK suggested pad layout	41
Figure 50. PPAK tube shipment (no suffix)	42
Figure 51. PPAK tape and reel (suffix "13TR")	42

1 Block diagram and pin description

Figure 1. Block diagram

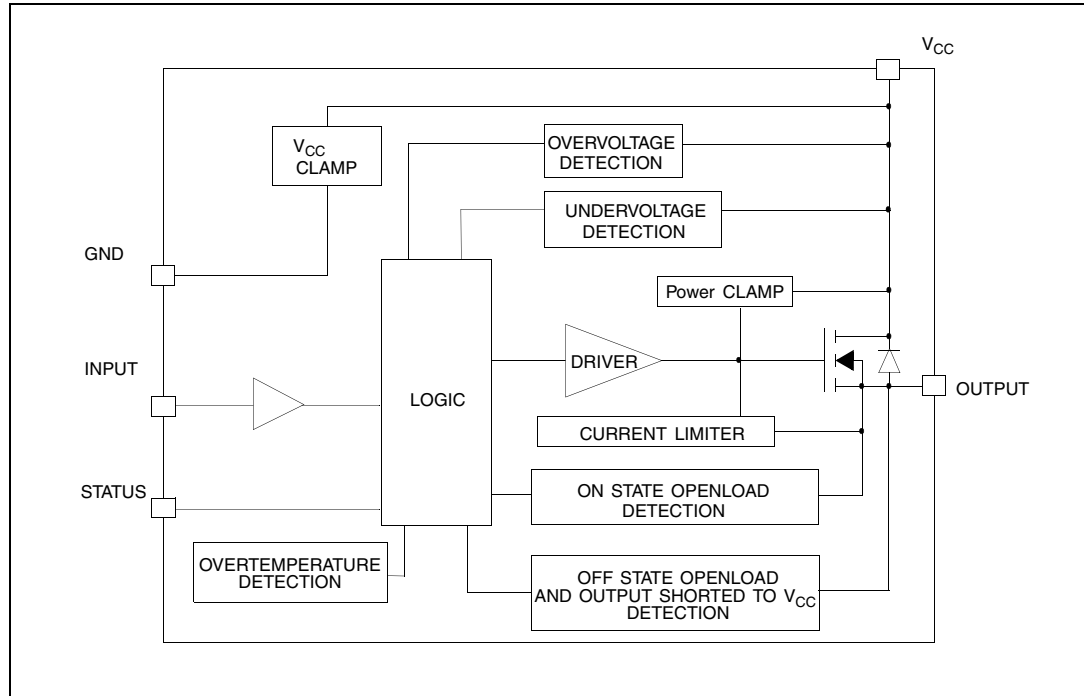


Figure 2. Configuration diagram (top view)

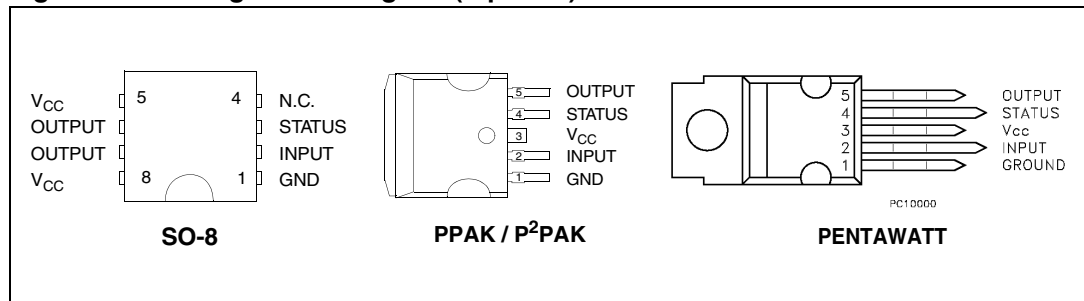
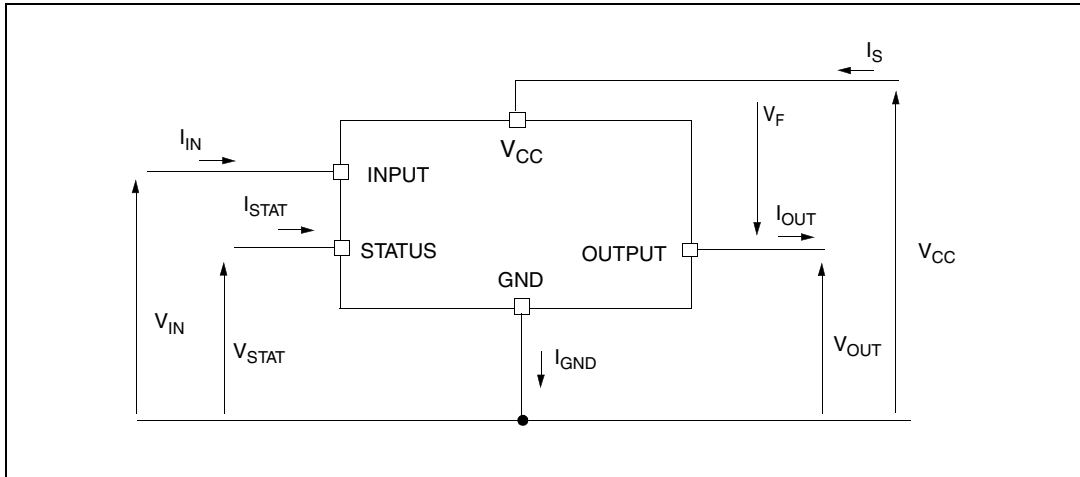


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		SO-8	PENTAWATT	P ² PAK	PPAK	
V _{CC}	DC supply voltage	41				V
- V _{CC}	Reverse DC supply voltage	- 0.3				V
- I _{gnd}	DC reverse ground pin current	- 200				mA
I _{OUT}	DC output current	Internally limited				A
- I _{OUT}	Reverse DC output current	- 6				A
I _{IN}	DC input current	+/- 10				mA
I _{STAT}	DC Status current	+/- 10				mA
V _{ESD}	Electrostatic discharge (human body model: R=1.5KΩ; C=100pF)					
	- INPUT	4000				V
	- STATUS	4000				V
	- OUTPUT	5000				V
	- V _{CC}	5000				V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value				Unit
		SO-8	PENTAWATT	P ² PAK	PPAK	
E _{MAX}	Maximum switching energy (L=1.8mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =9A)	100				mJ
E _{MAX}	Maximum switching energy (L=2.46mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =9A)			138	138	mJ
P _{tot}	Power dissipation T _C =25°C	4.2	60	60	60	W
T _j	Junction operating temperature	Internally limited				°C
T _C	Case operating temperature	- 40 to 150				°C
T _{stg}	Storage temperature	- 55 to 150				°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value				Unit
		SO-8	PENTAWATT	P ² PAK	PPAK	
R _{thj-case}	Thermal resistance junction-case	-	2.1	2.1	2.1	°C/W
R _{thj-lead}	Thermal resistance junction-lead	30	-	-	-	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	93 ⁽¹⁾	62.1	52.1 ⁽²⁾	77.1 ⁽²⁾	°C/W
		82 ⁽³⁾	62.1	37 ⁽⁴⁾	44 ⁽⁴⁾	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.
3. When mounted on a standard single-sided FR-4 board with 2cm² of Cu (at least 35μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
4. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick). Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On state resistance	$I_{OUT} = 2A$; $T_j = 25^{\circ}C$; $V_{CC} > 8V$ $I_{OUT} = 2A$; $V_{CC} > 8V$			60 120	m Ω m Ω
I_S	Supply current	Off State; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$		10	25	μA
		Off State; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$; $T_j = 25^{\circ}C$		10	20	μA
		On State; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$		2	3.5	mA
$I_{L(off1)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off state output current	$V_{IN} = 0V$; $V_{OUT} = 3.5V$	-75		0	μA
$I_{L(off3)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$			5	μA
$I_{L(off4)}$	Off state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$			3	μA

Table 6. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3V$		40		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7V$		30		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 1.3V$ to $V_{OUT}=10.4V$	See Figure 21 .			V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 11.7V$ to $V_{OUT}=1.3V$	See Figure 22 .			V/ μs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25V$	1			μA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	$V_{IN} = 3.25V$			10	μA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 - 0.7	8	V V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT} = 1.3A; T_j = 150^\circ C$			0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6mA$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5V$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5V$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6	6.8 - 0.7	8	V V

Table 10. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^\circ C$
T_R	Reset temperature		135			$^\circ C$
T_{hyst}	Thermal hysteresis		7	15		$^\circ C$
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
I_{lim}	Current limitation	$9V < V_{CC} < 36V$ $5V < V_{CC} < 36V$	6	9	15 15	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 2 A; V_{IN} = 0V;$ $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Open load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Openload ON state detection threshold	$V_{IN} = 5V$	50		200	mA
$t_{DOL(on)}$	Openload ON state detection delay	$I_{OUT} = 0A$			200	μs
V_{OL}	Openload OFF state voltage detection threshold	$V_{IN} = 0V$	1.5		3.5	V
$t_{DOL(off)}$	Openload detection delay at turn-off				1000	μs

Figure 4. Status timings

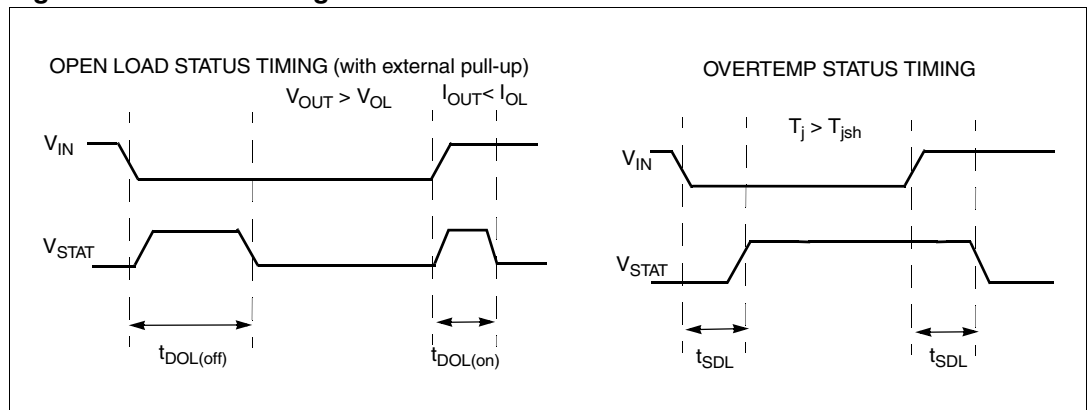


Figure 5. Switching time waveforms

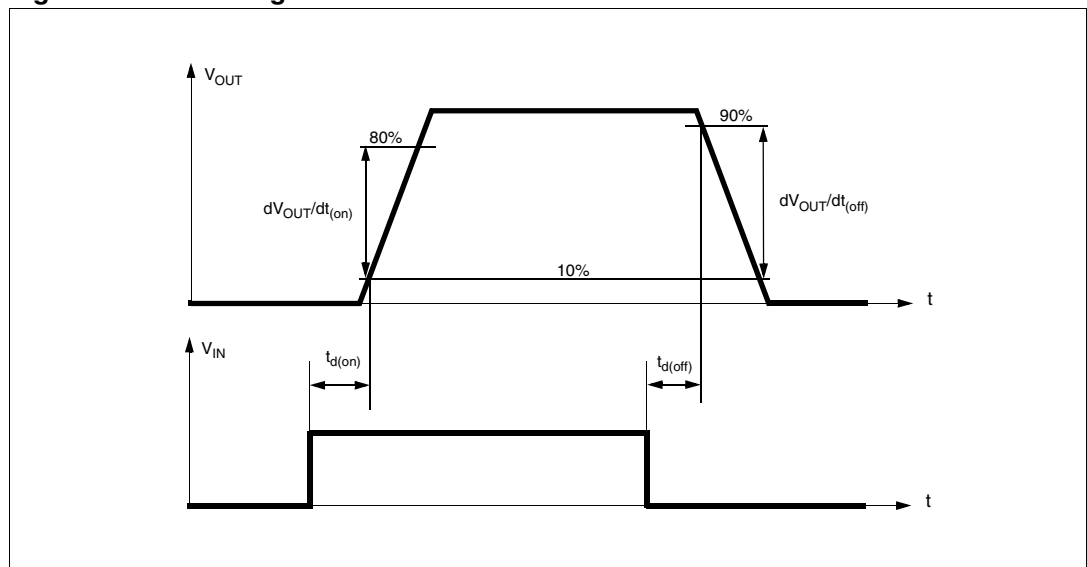


Table 12. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H
	H	X	$(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage $> V_{OL}$	L	H	L
	H	H	H
Output current $< I_{OL}$	L	L	H
	H	H	L

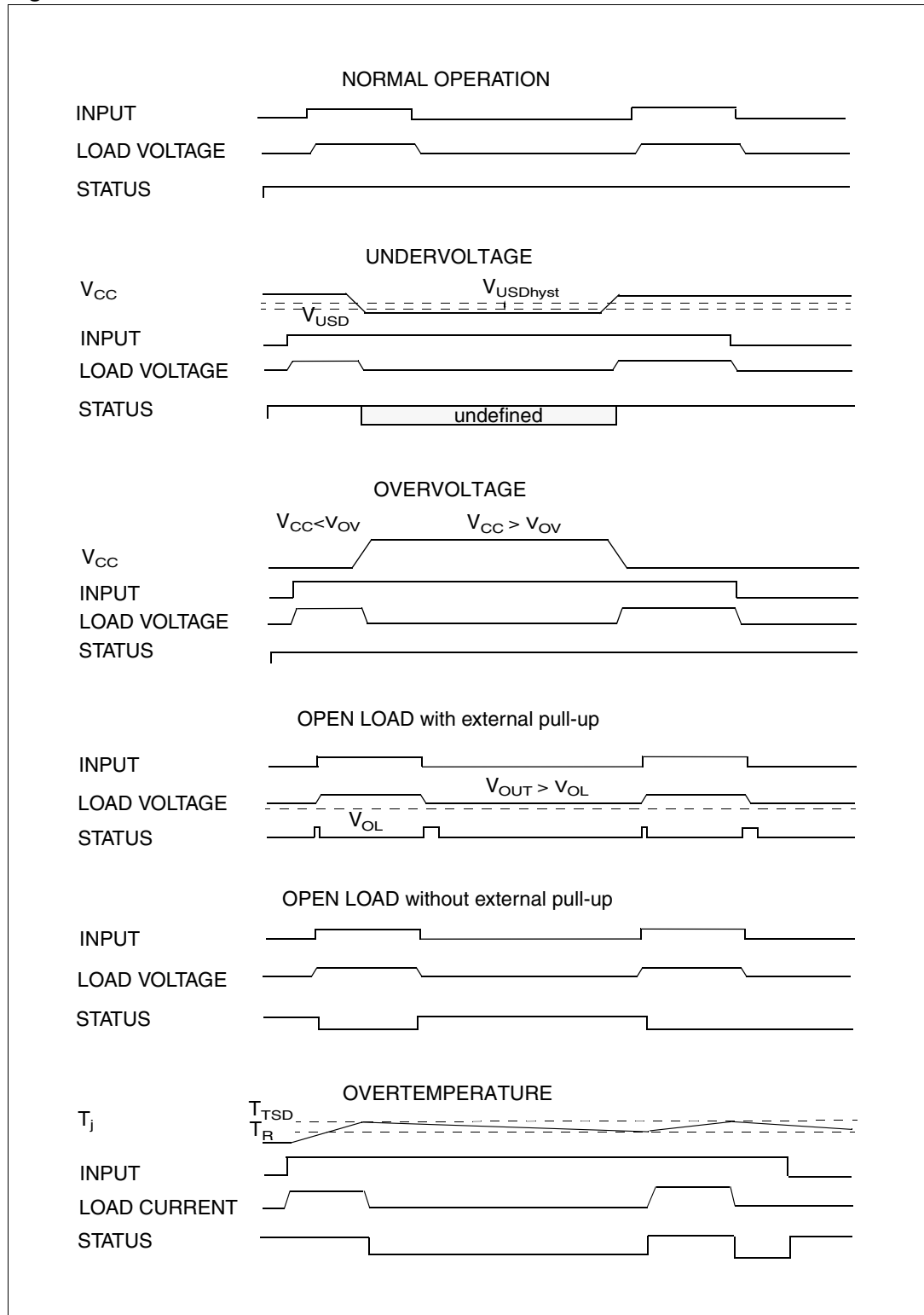
Table 13. Electrical transient requirements on V_{CC} pin

ISO T/R 7637/1 Test pulse	Test levels				Delays and impedance
	I	II	III	IV	
1	- 25 V	- 50 V	- 75 V	- 100 V	2 ms 10 Ω
2	+ 25 V	+ 50 V	+ 75 V	+ 100 V	0.2 ms 10 Ω
3a	- 25 V	- 50 V	- 100 V	- 150 V	0.1 μs 50 Ω
3b	+ 25 V	+ 50 V	+ 75 V	+ 100 V	0.1 μs 50 Ω
4	- 4 V	- 5 V	- 6 V	- 7 V	100 ms, 0.01 Ω
5	+ 26.5 V	+ 46.5 V	+ 66.5 V	+ 86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off state output current

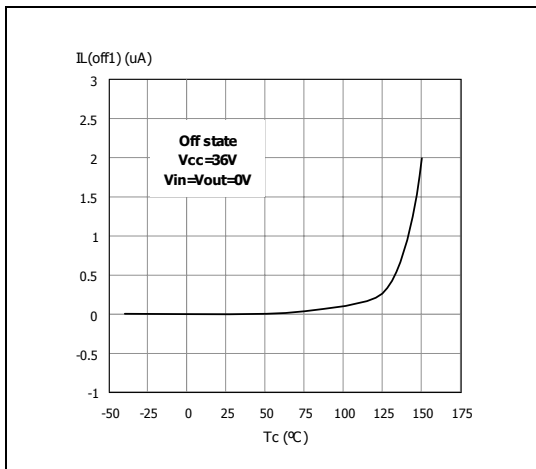


Figure 8. High level input current

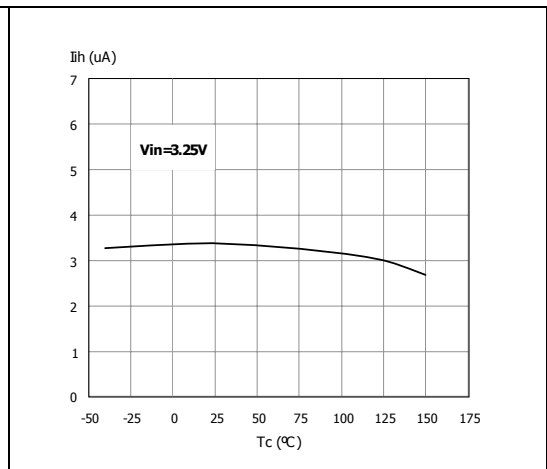


Figure 9. Input clamp voltage

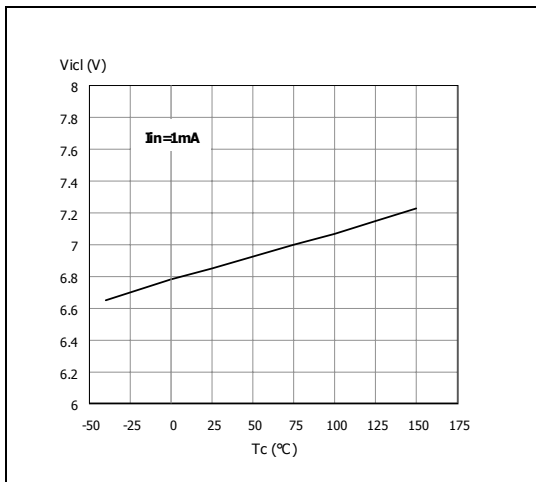


Figure 10. Status leakage current

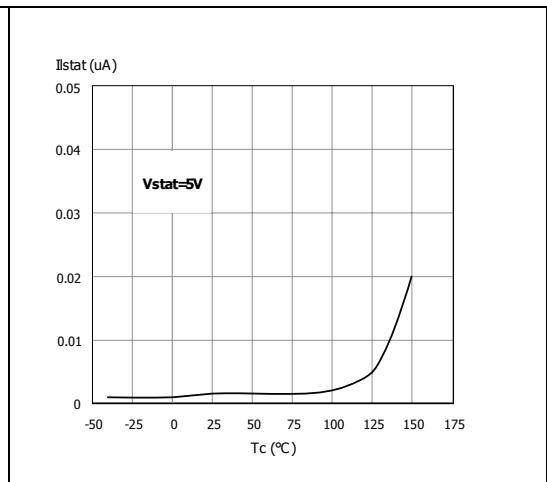


Figure 11. Status low output voltage

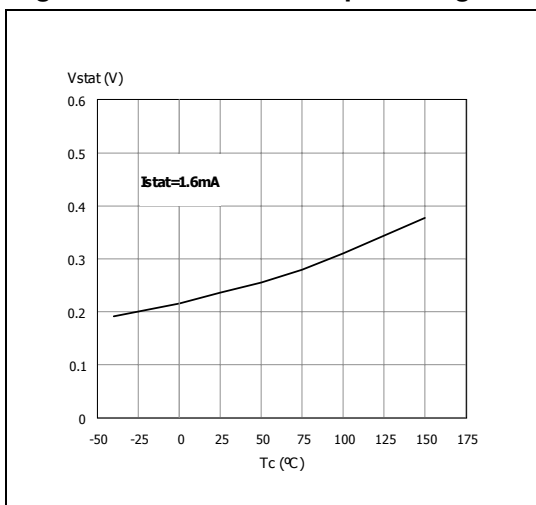


Figure 12. Status clamp voltage

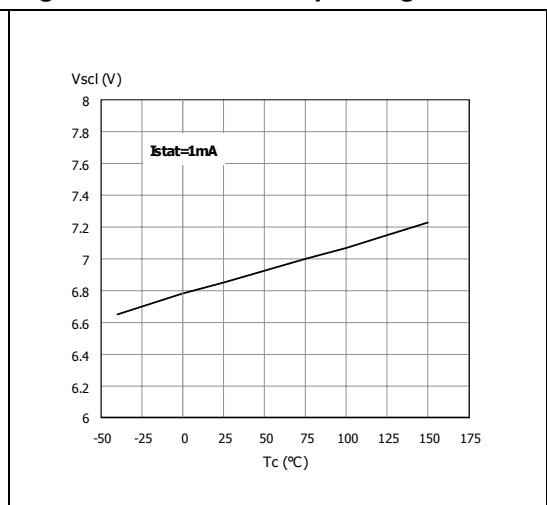


Figure 13. On state resistance Vs T_{case}

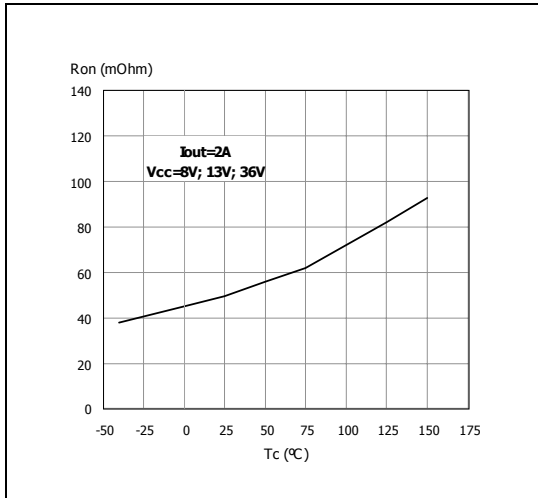


Figure 14. On state resistance Vs V_{CC}

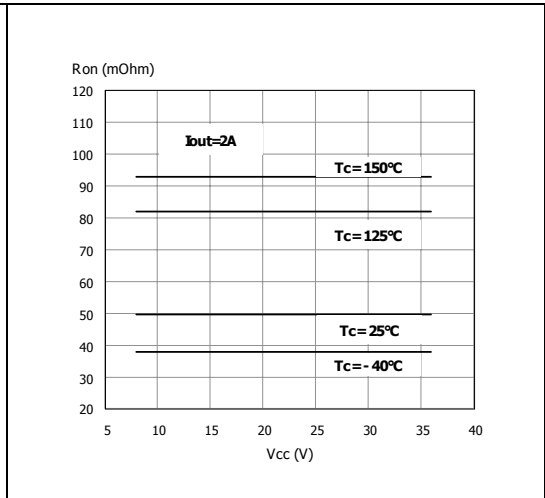


Figure 15. Open load On state detection

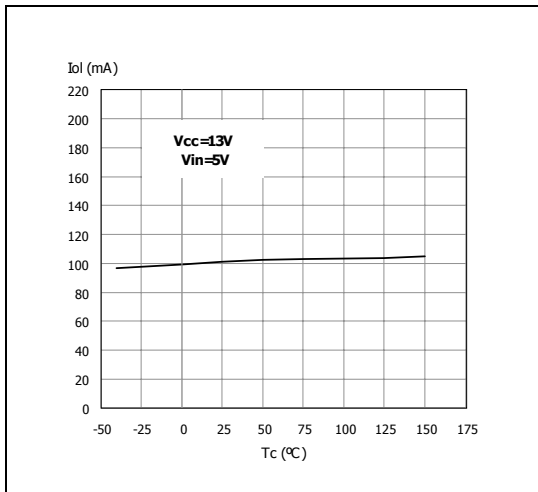


Figure 16. Input high level threshold

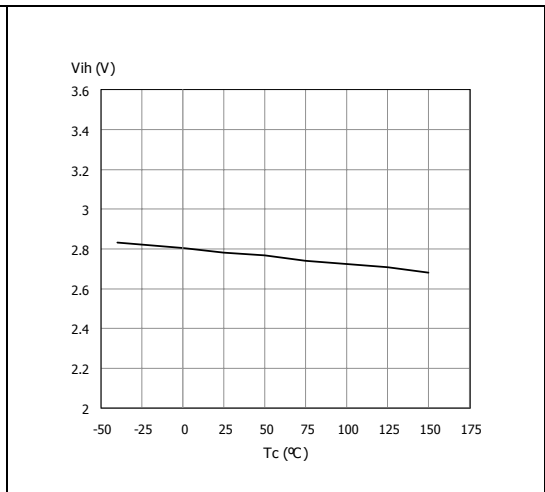


Figure 17. Input low level

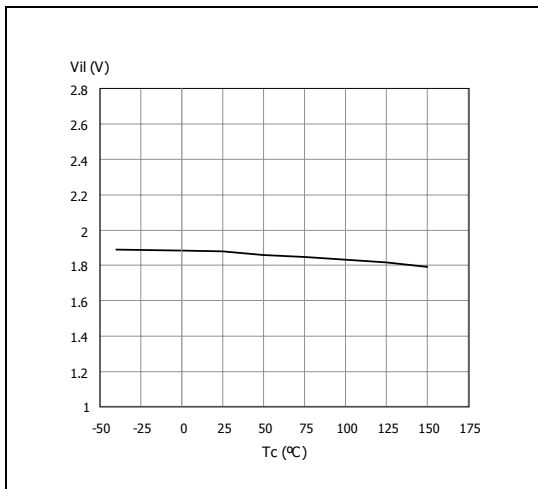


Figure 18. Input hysteresis voltage

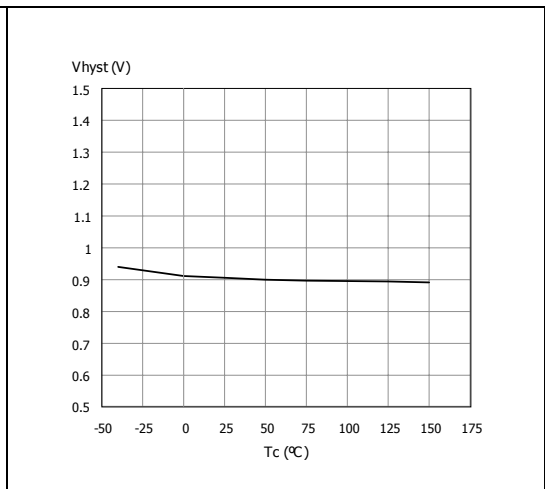


Figure 19. Overtoltage shutdown

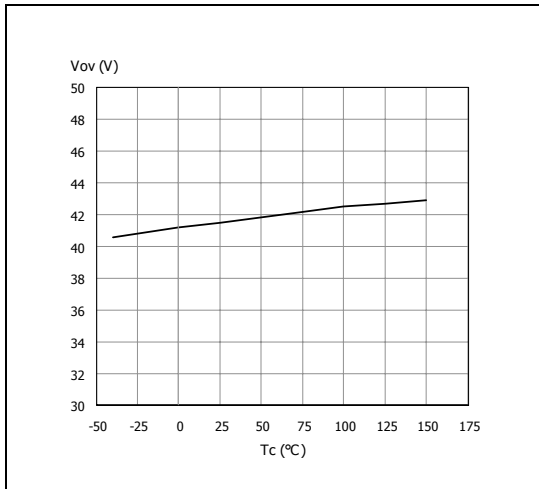


Figure 20. Openload Off state voltage detection threshold

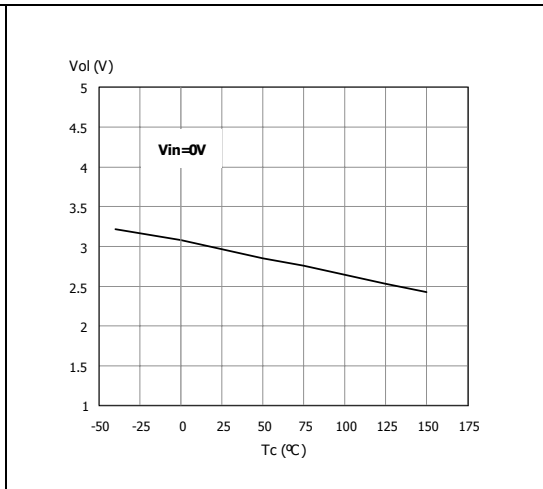


Figure 21. Turn-on voltage slope

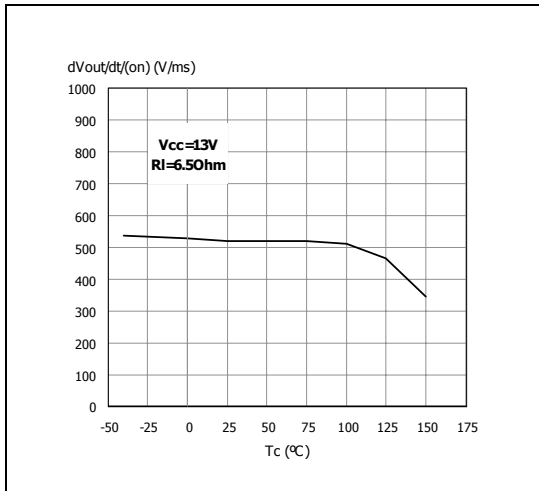


Figure 22. Turn-off voltage slope

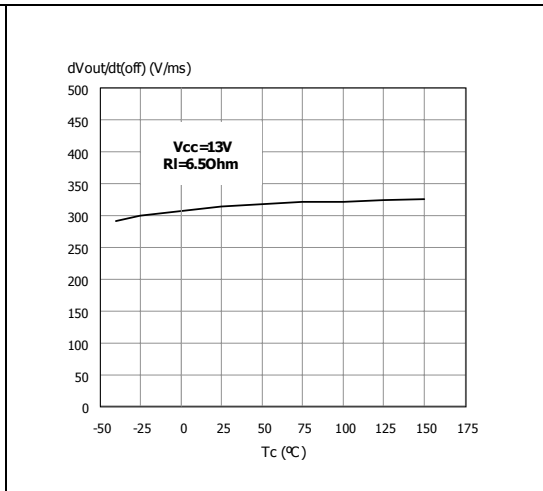


Figure 23. Ilim Vs Tcase

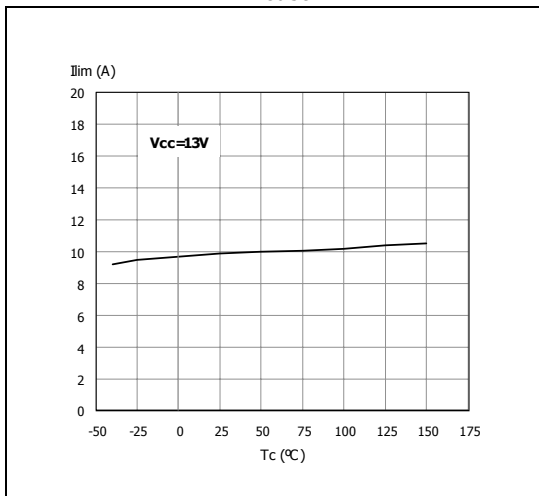
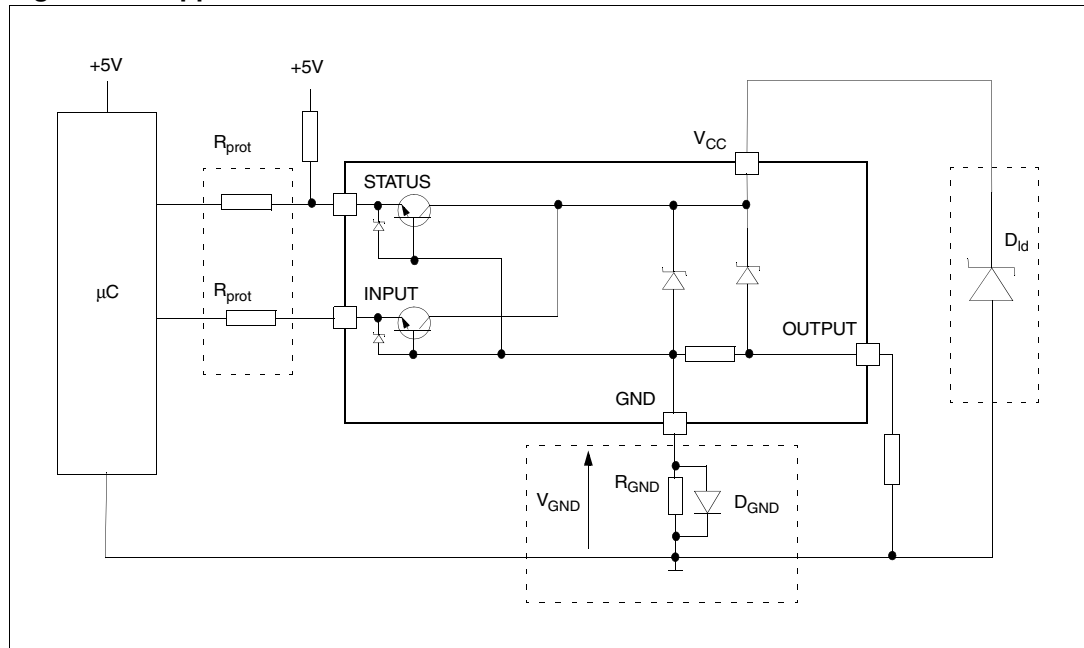


Figure 24. Application schematic



2.5 GND protection network against reverse battery

2.5.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where - I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC} < 0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

2.5.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

2.6 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

2.7 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$.

2.8 Open load detection in Off state

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

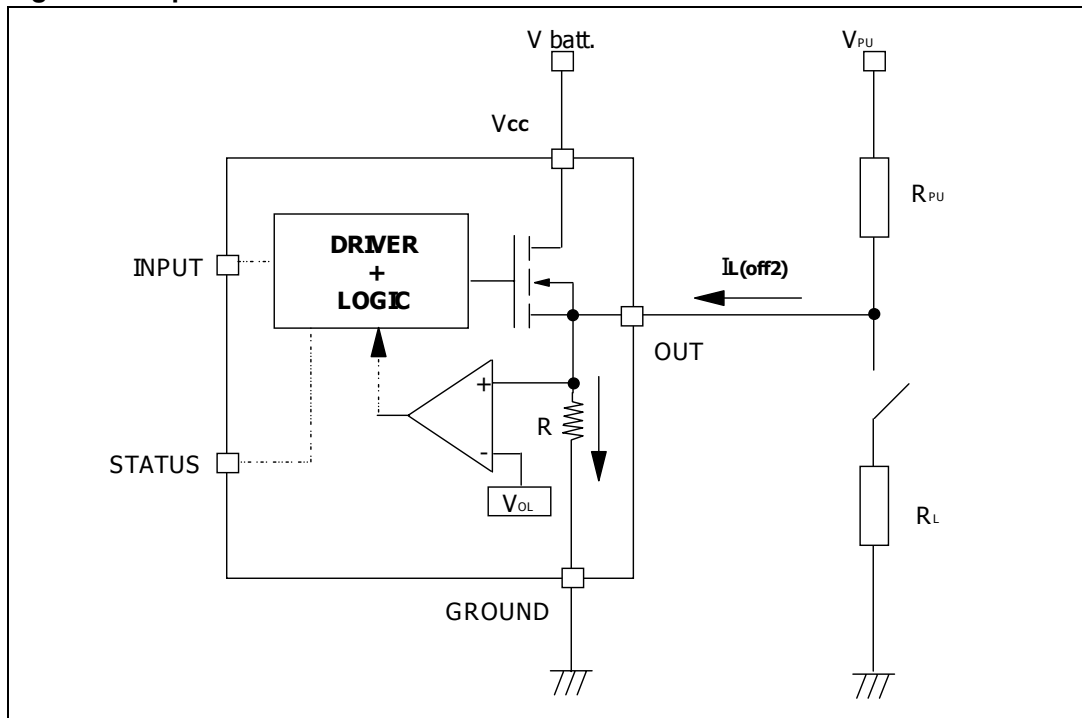
The external resistor has to be selected according to the following requirements:

- no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Omin} ; this results in the following condition $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{Omin}$.
- no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{S(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

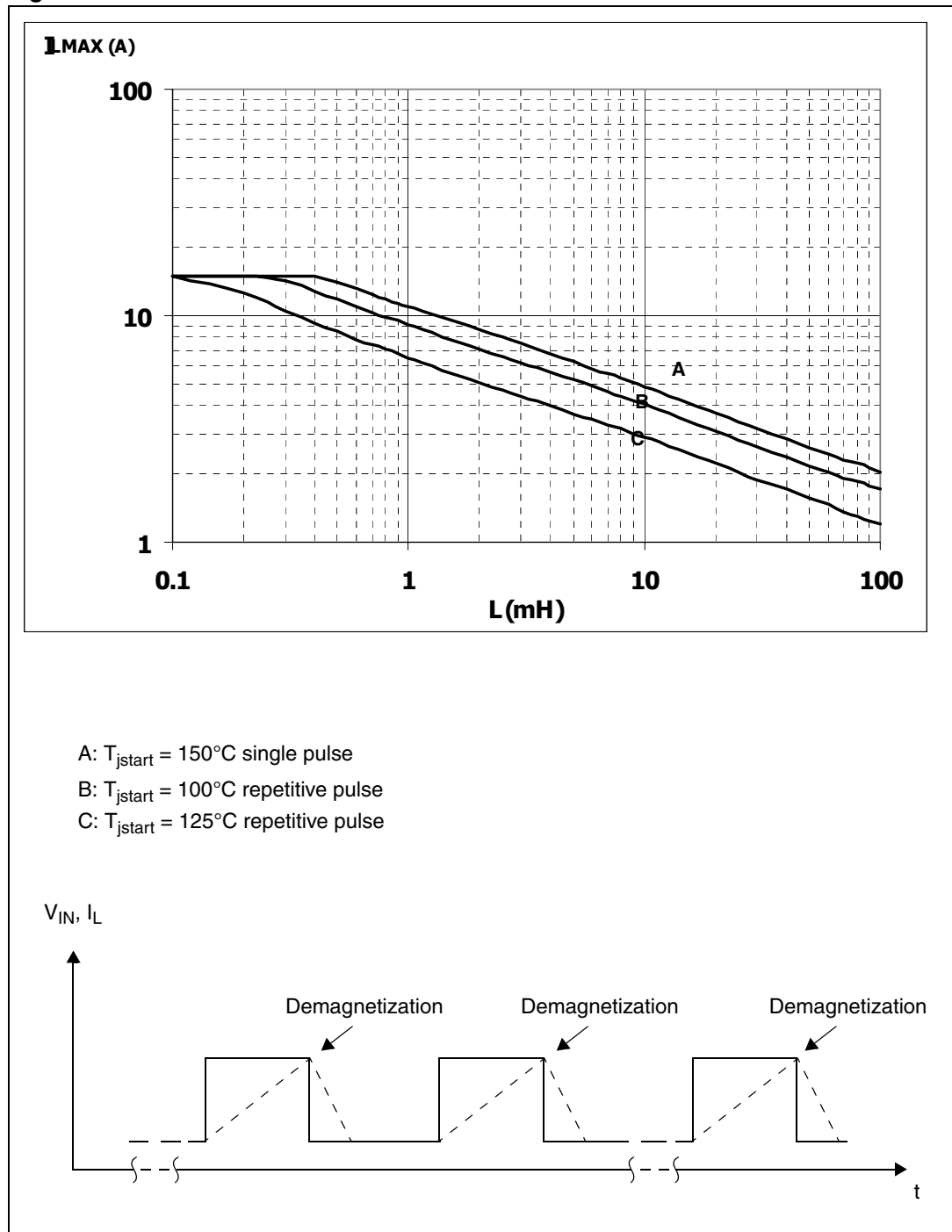
The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 25. Open load detection in Off state



2.9 SO-8 maximum demagnetization energy ($V_{CC} = 13.5V$)

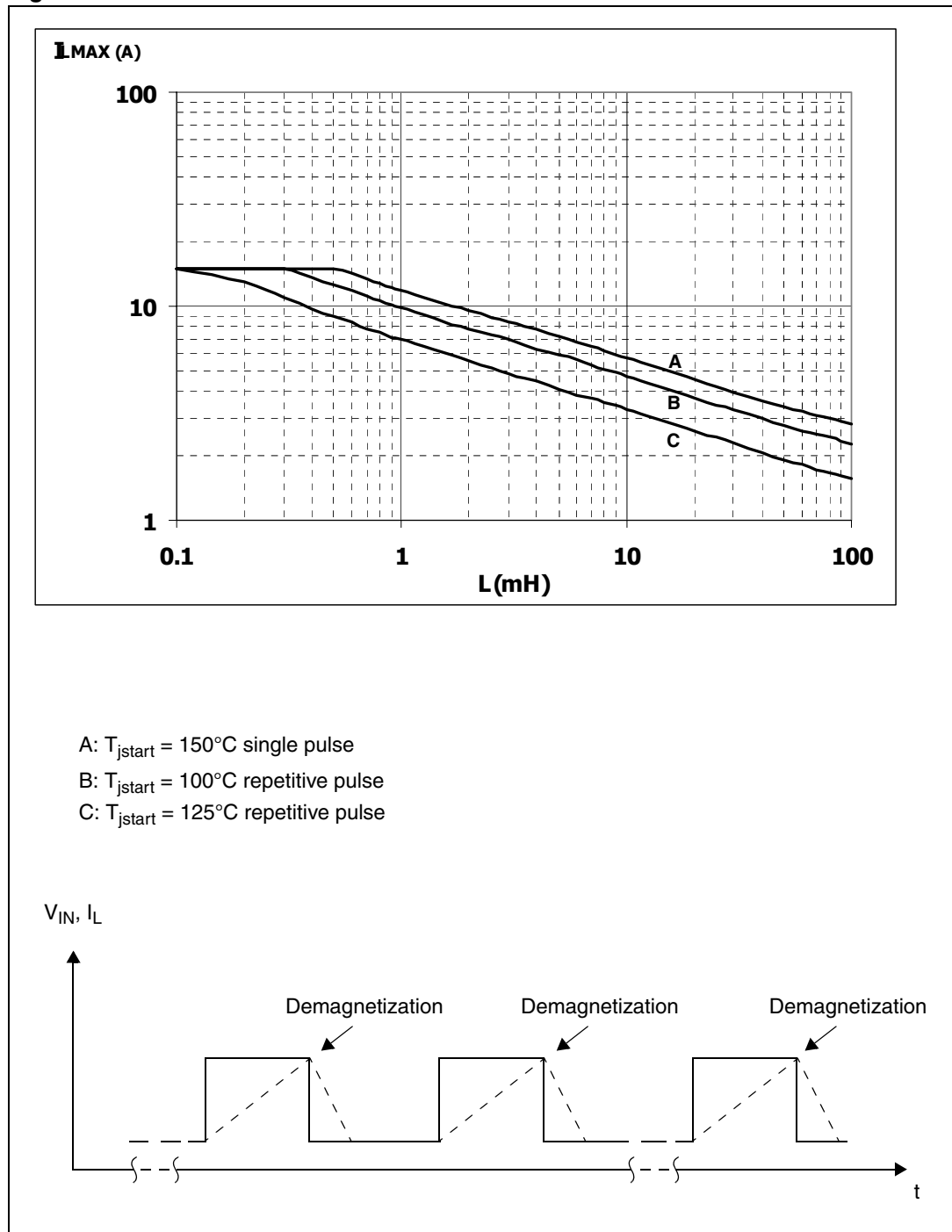
Figure 26. SO-8 maximum turn-off current versus inductance



Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

2.10 PPAK/P²PAK maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 27. PPAK /P²PAK maximum turn-off current versus inductance

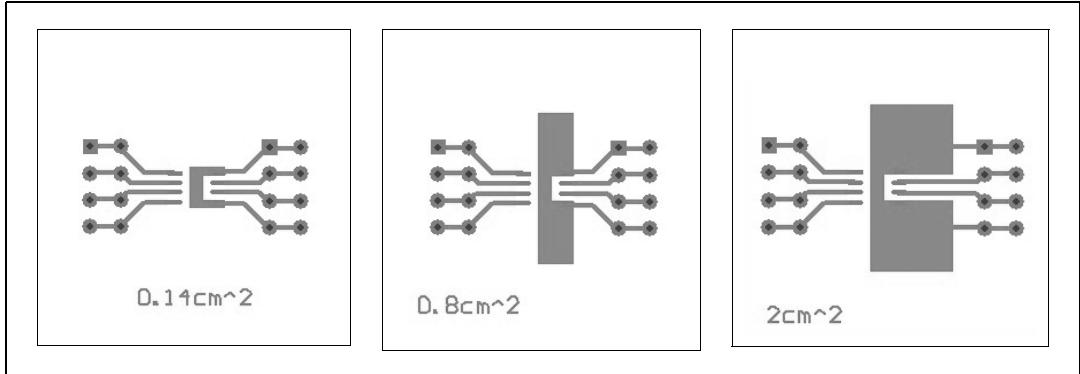


Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3 Package and PCB thermal data

3.1 SO-8 thermal data

Figure 28. PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58 mm, PCB thickness = 2 mm, Cu thickness=35 μ m, Copper areas: 0.14 cm², 0.8 cm², 2 cm²).

Figure 29. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

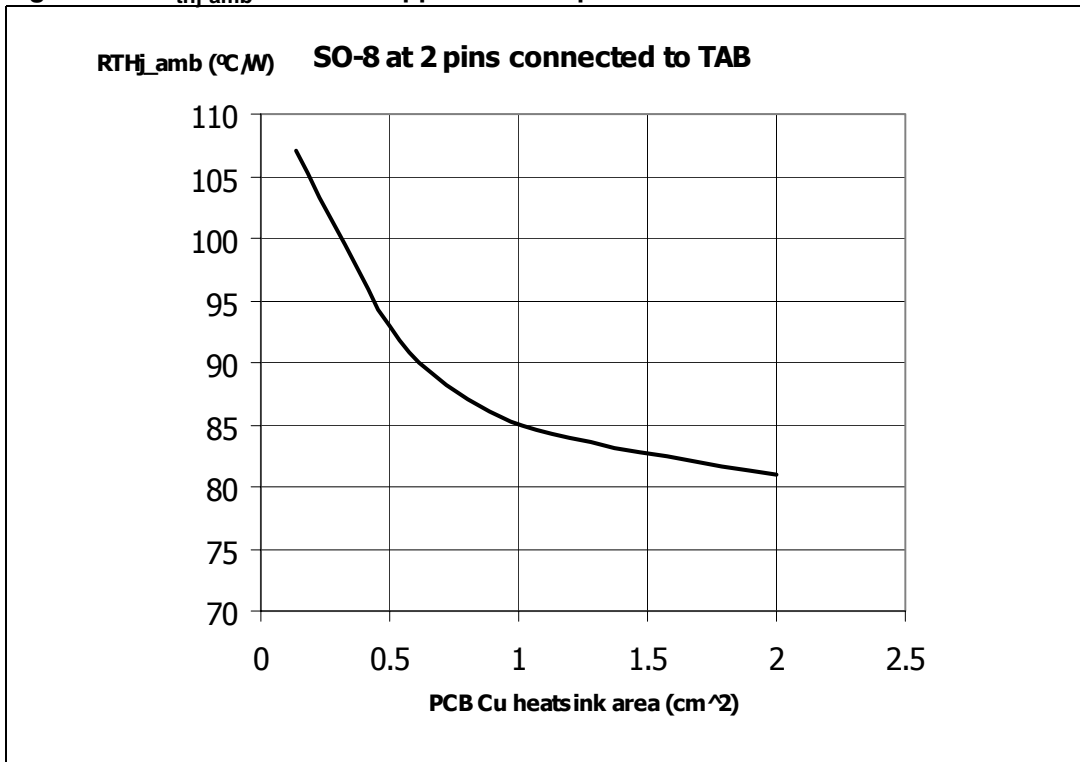
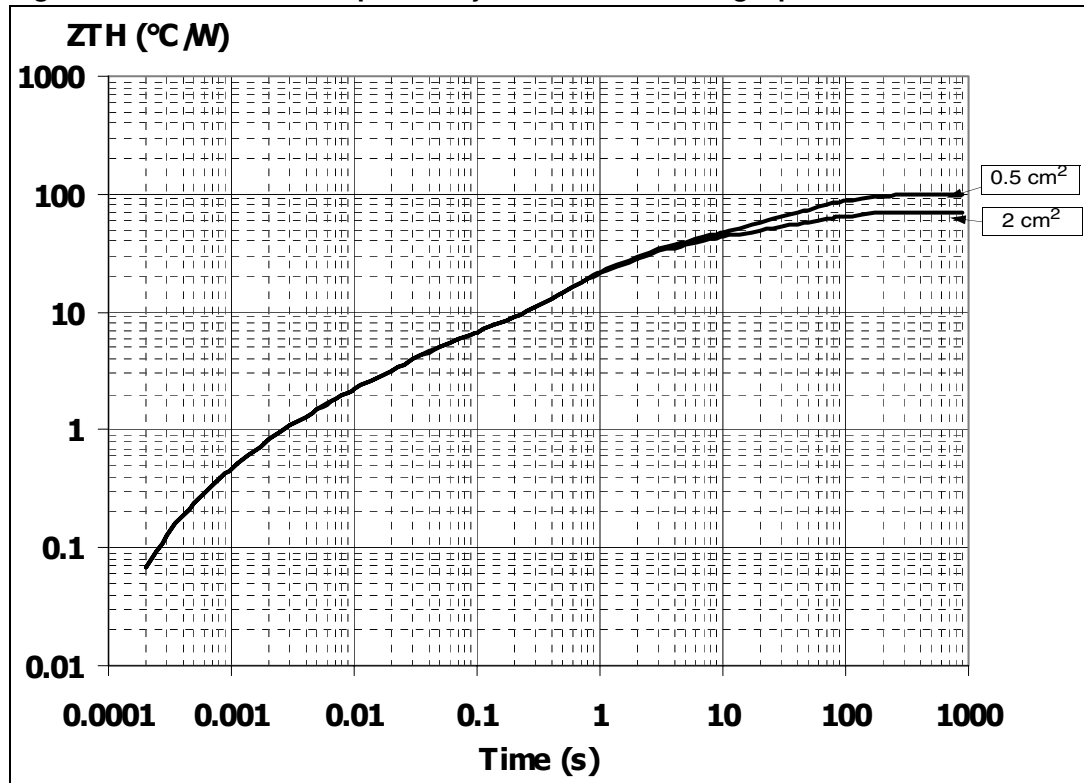


Figure 30. SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31. Thermal fitting model of a single channel

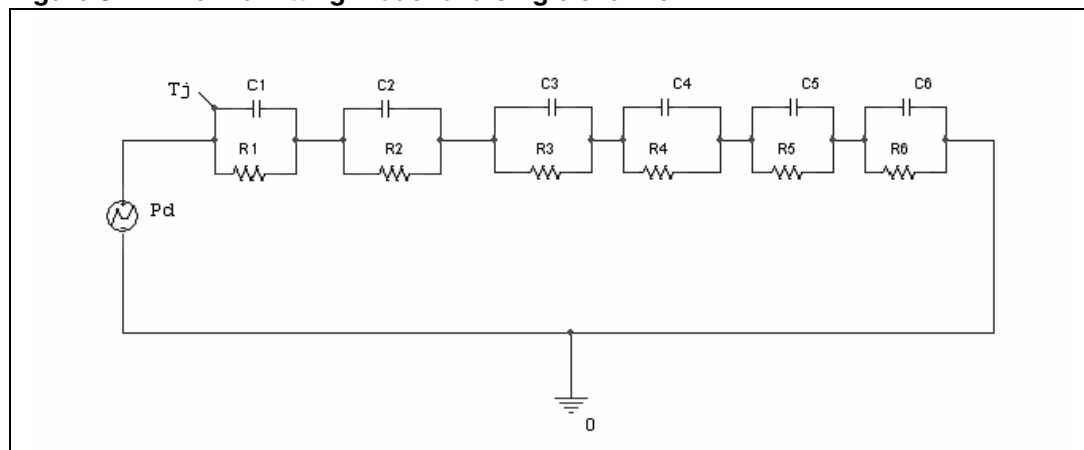
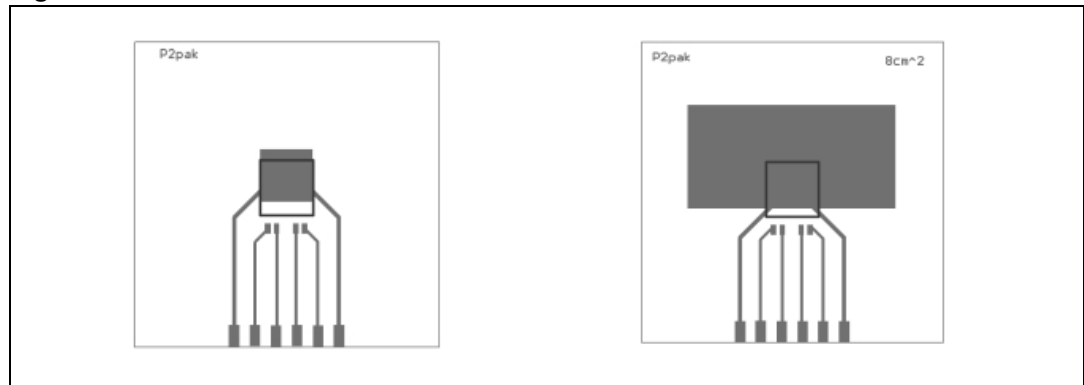


Table 14. Thermal parameter

Area/island (cm ²)	0.5	2
R1 (°C/W)	0.05	
R2 (°C/W)	0.8	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W·s/°C)	0.006	
C2 (W·s/°C)	0.0026	
C3 (W·s/°C)	0.0075	
C4 (W·s/°C)	0.045	
C5 (W·s/°C)	0.35	
C6 (W·s/°C)	1.05	2

3.2 P²PAK thermal data

Figure 32. PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35μm, Copper areas: 0.97cm², 8cm²).

Figure 33. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

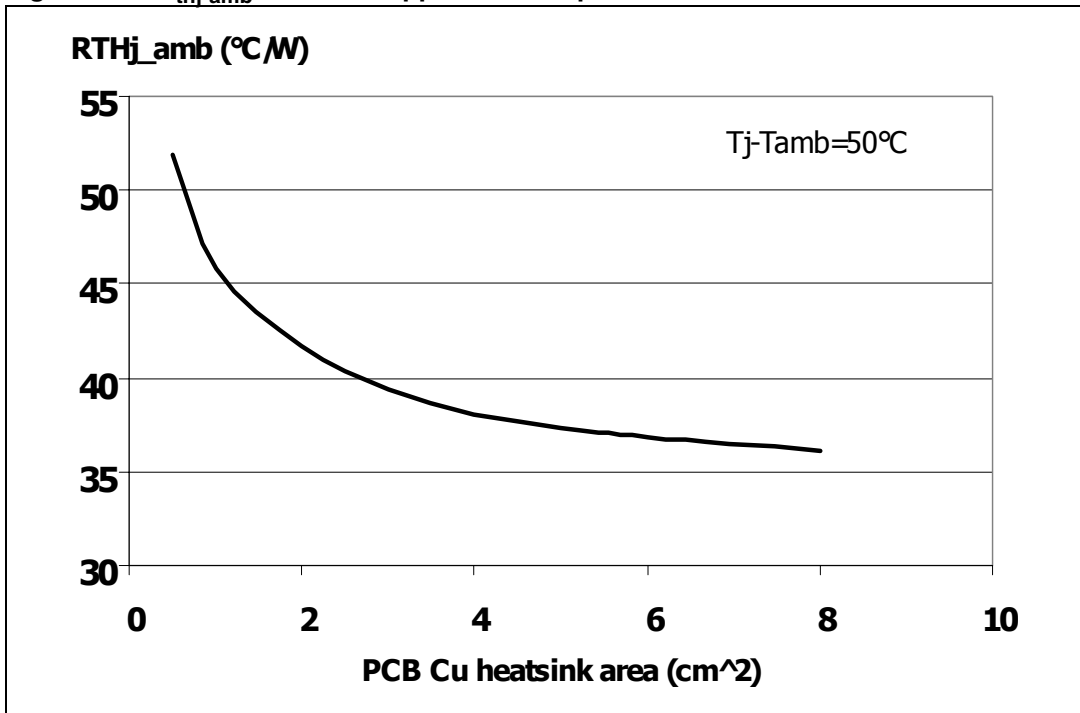
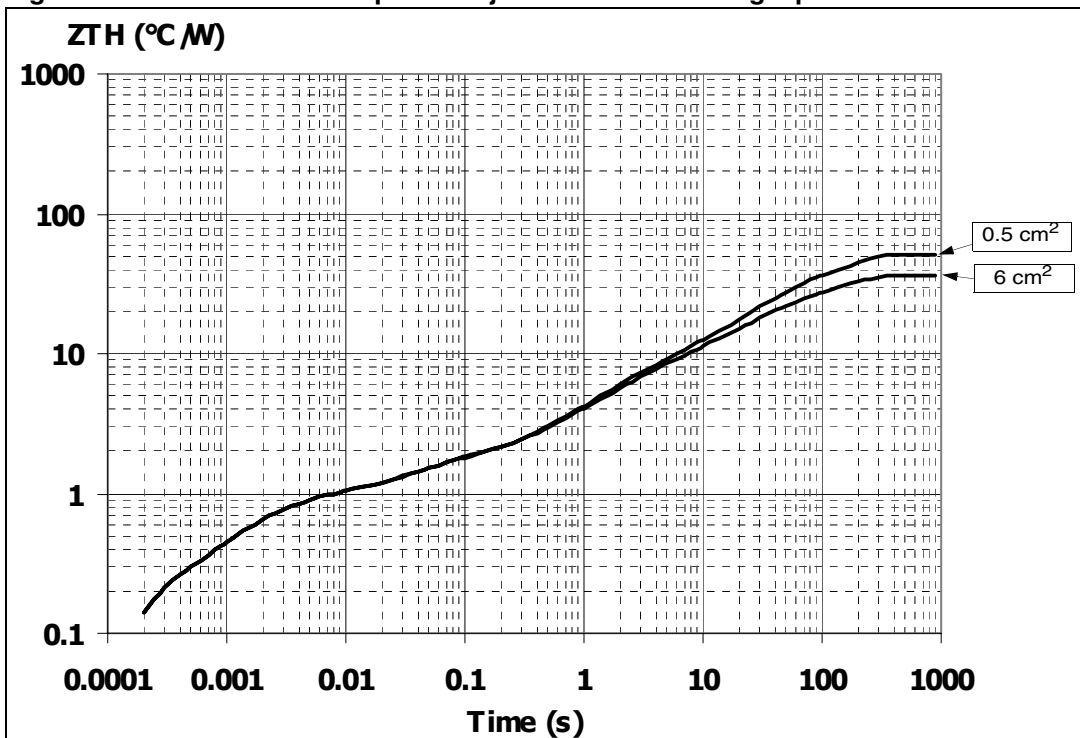


Figure 34. P²PAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. Thermal fitting model of a single channel

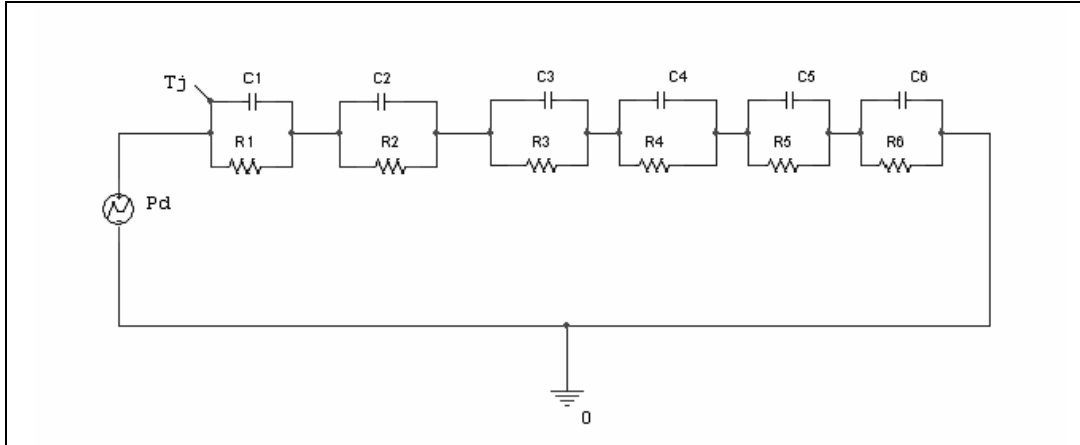
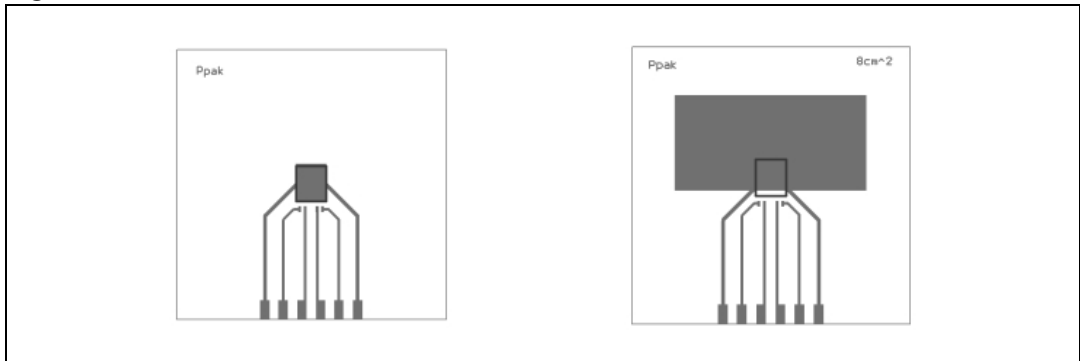


Table 15. Thermal parameter

Area/island (cm ²)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	0.7	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0006	
C2 (W·s/°C)	0.0025	
C3 (W·s/°C)	0.055	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

3.3 PPAK thermal data

Figure 36. PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness=35 μ m , Copper areas: 0.44 cm², 8 cm²).

Figure 37. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

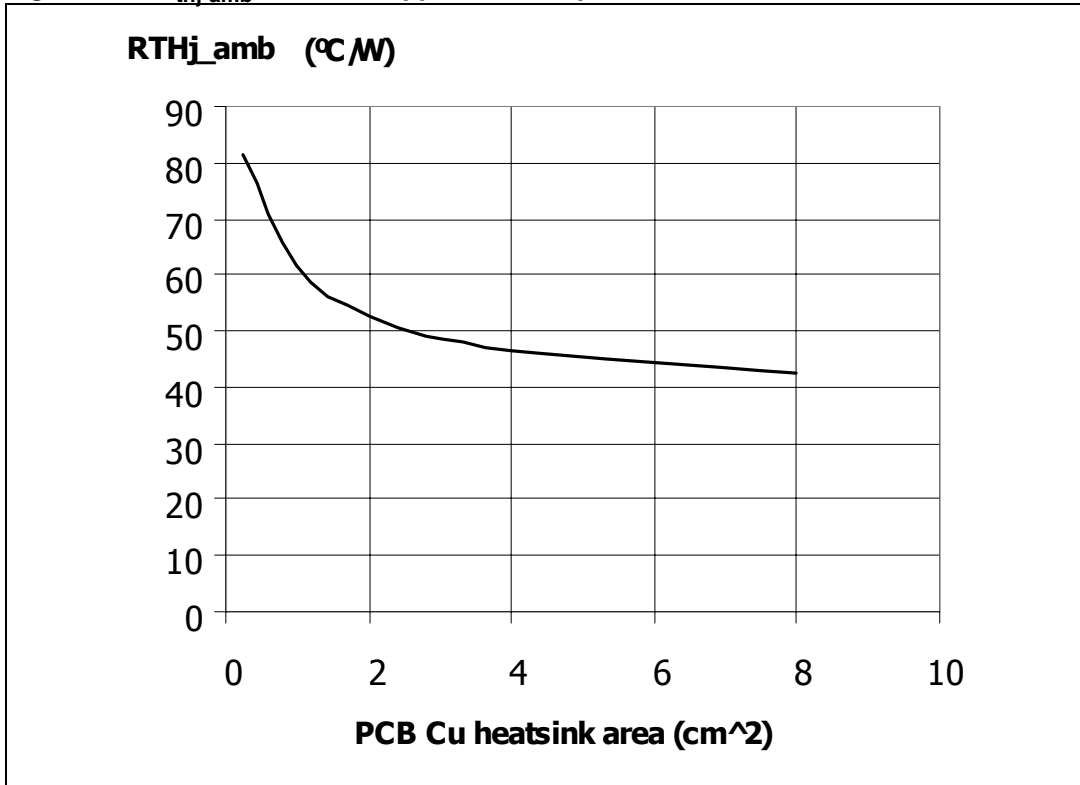
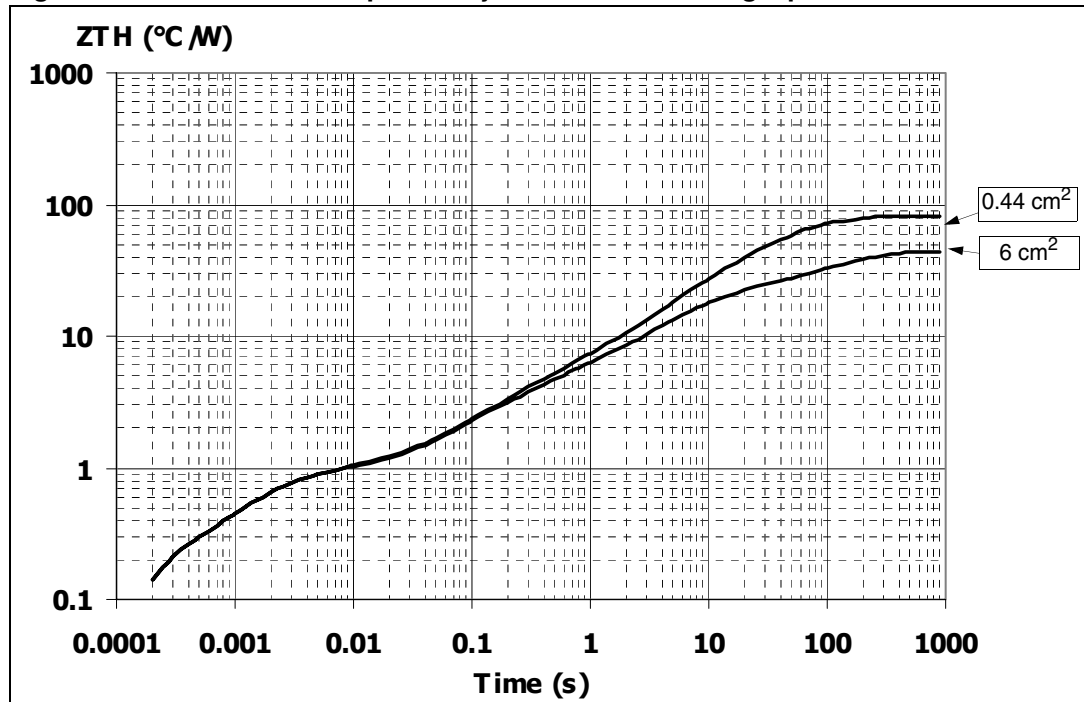


Figure 38. PPAK thermal impedance junction ambient single pulse



Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 39. Thermal fitting model of a single channel

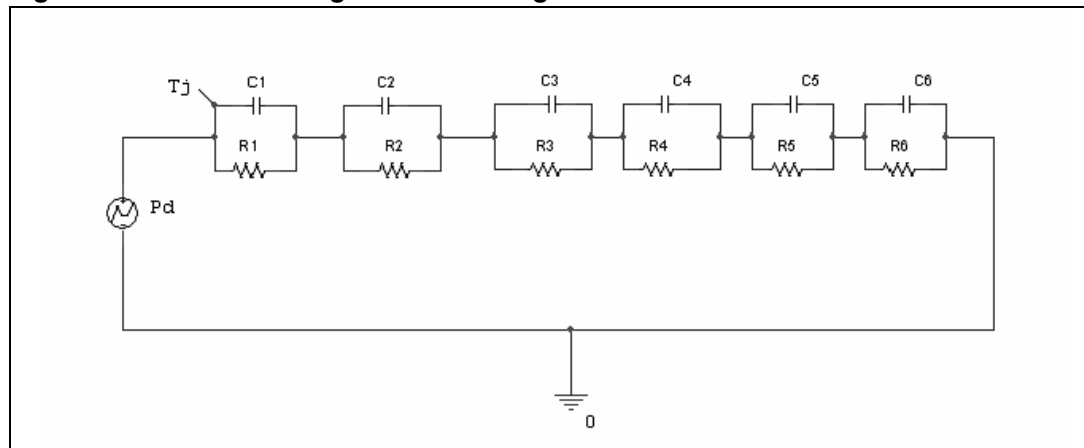


Table 16. Thermal parameter

Area/island (cm ²)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	1.6	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.0006	
C2 (W·s/°C)	0.0025	
C3 (W·s/°C)	0.08	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4.2 SO-8 package information

Figure 40. SO-8 package dimensions

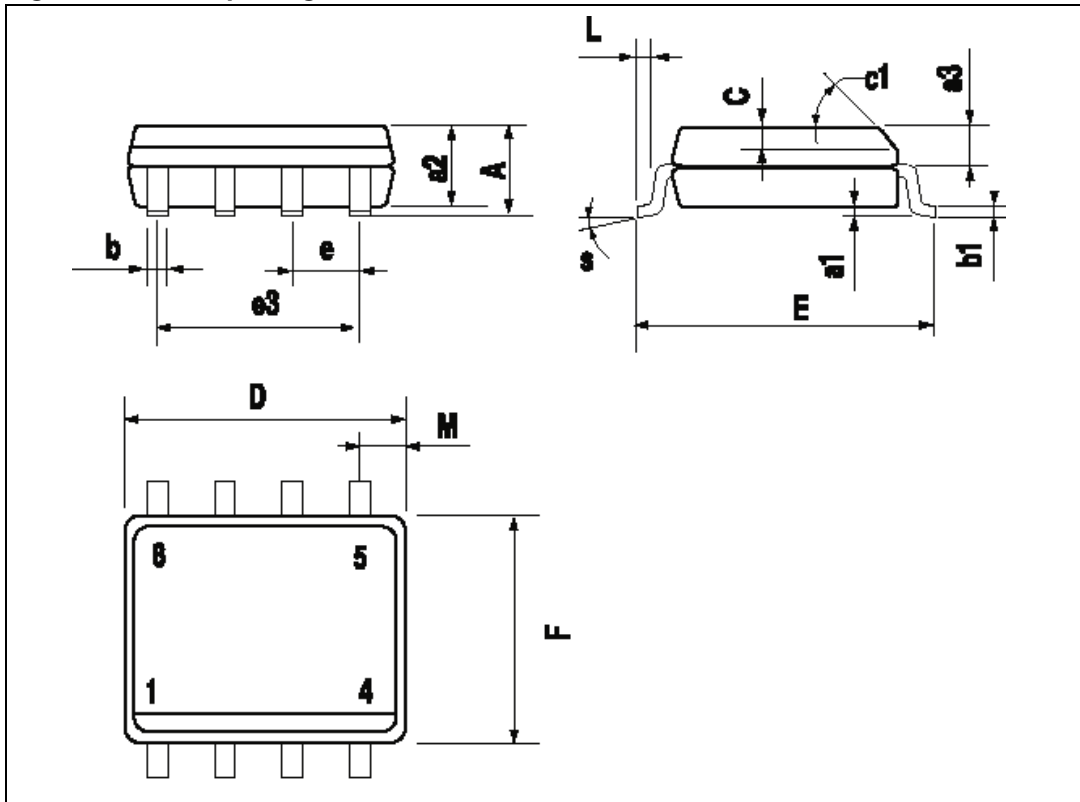


Table 17. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

4.3 PENTAWATT mechanical data

Figure 41. PENTAWATT package dimensions

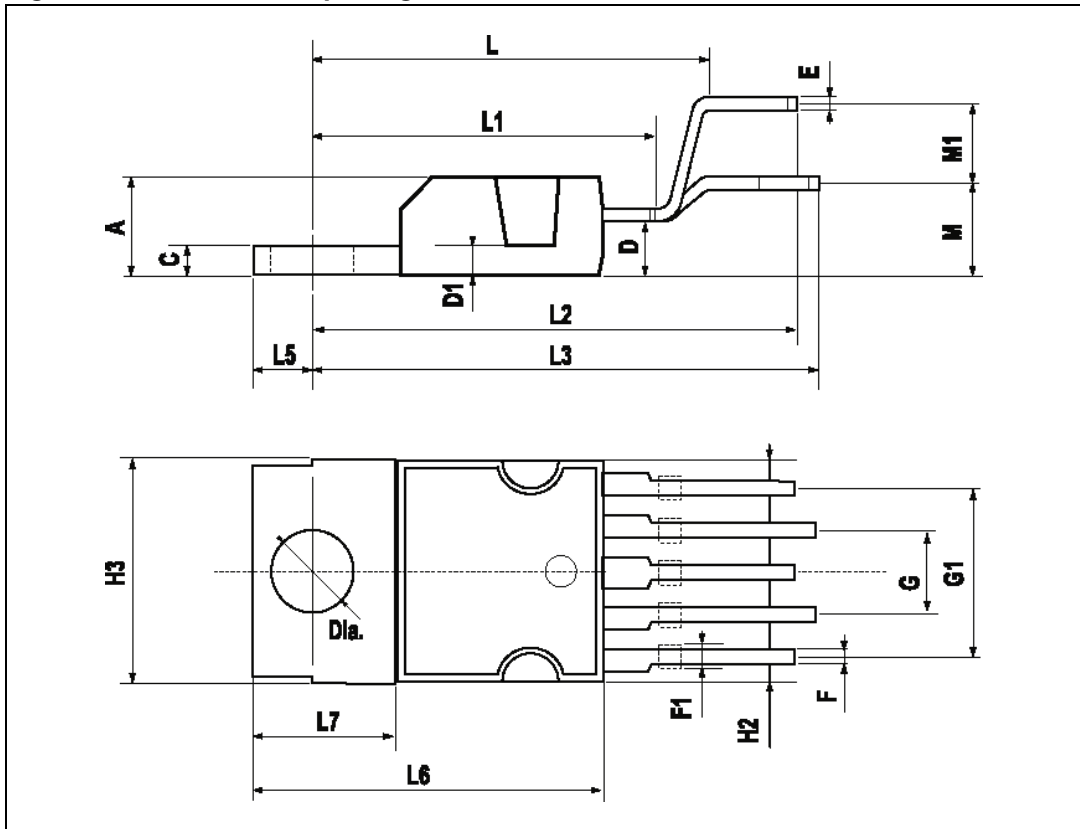


Table 18. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4

Table 18. PENTAWATT mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

4.4 P²PAK mechanical data

Figure 42. P²PAK package dimensions

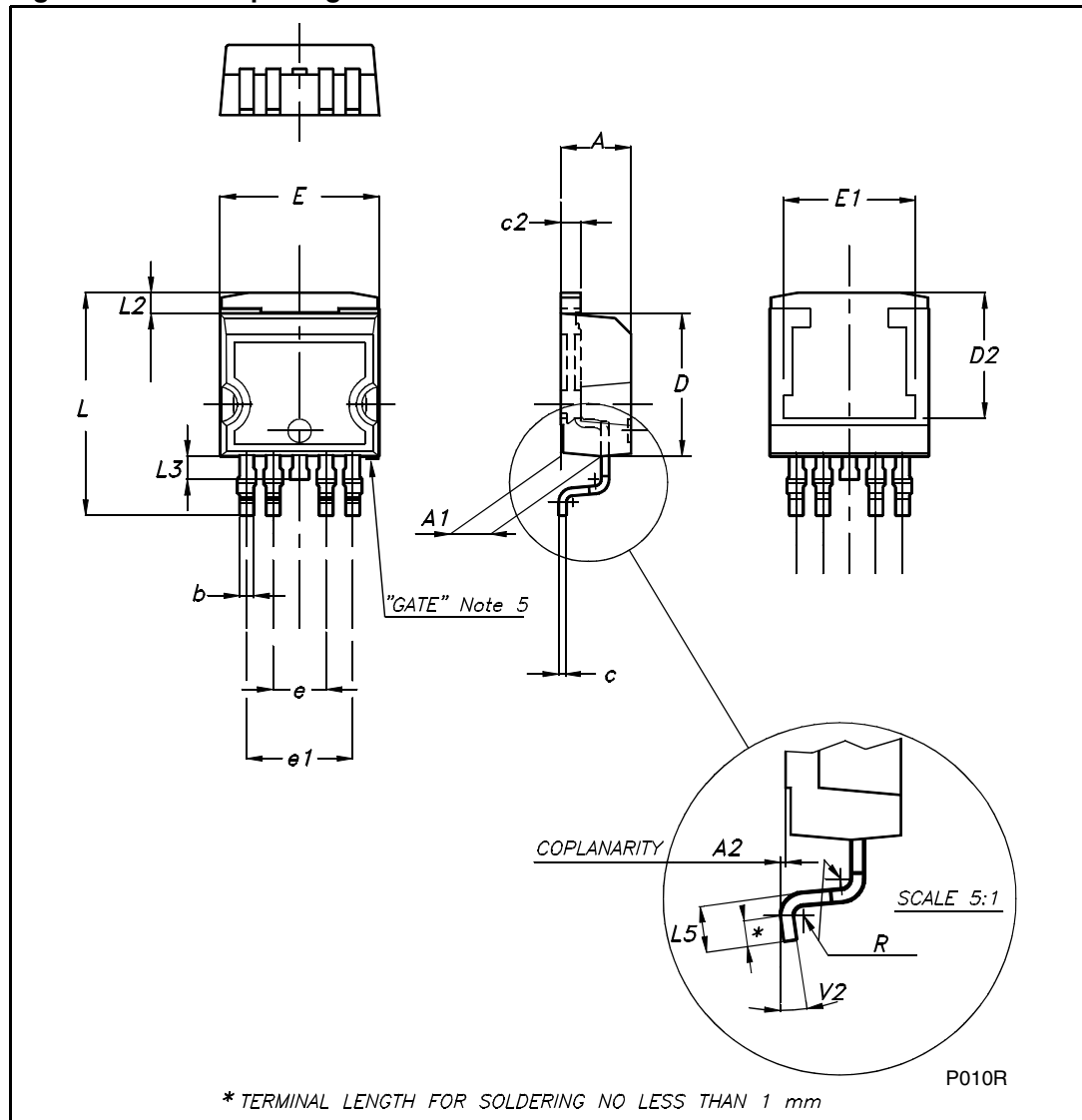


Table 19. P²PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package weight	1.40 Gr (typ)		

4.5 PPAK mechanical data

Figure 43. PPAK package dimensions

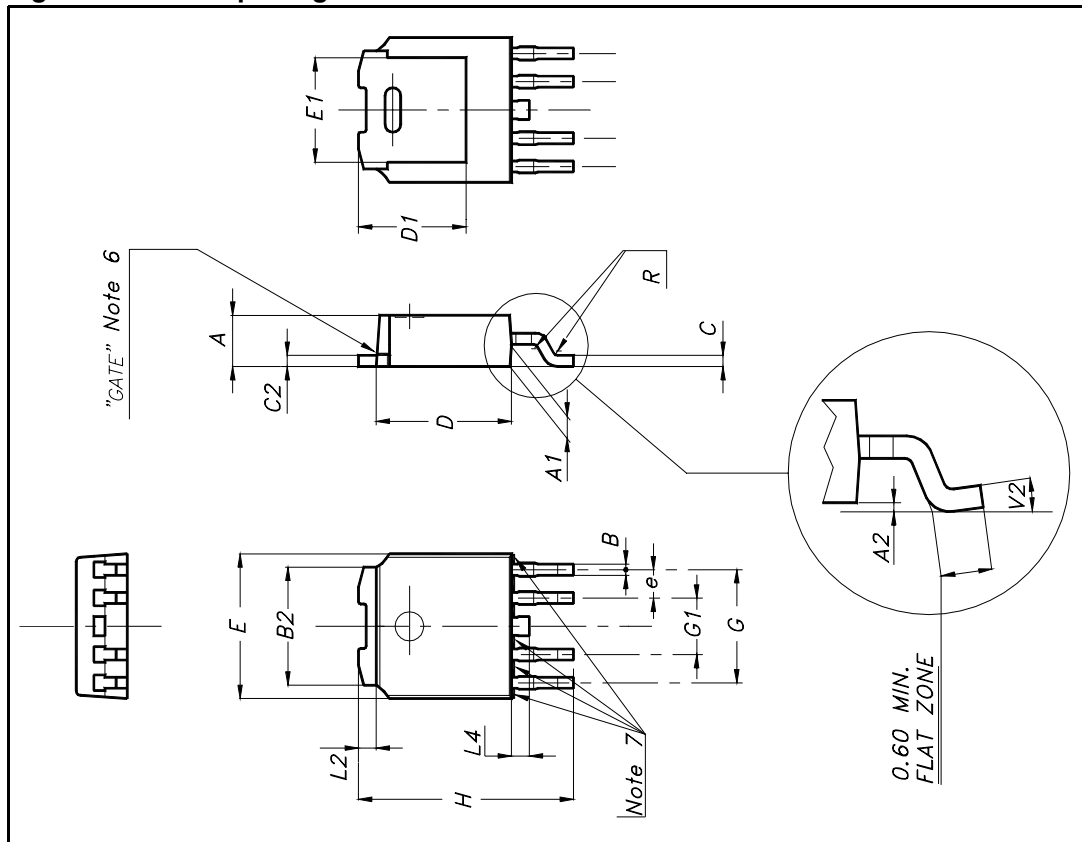


Table 20. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60

Table 20. PPAK mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package weight	Gr. 0.3		

4.6 SO-8 packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 44. SO-8 tube shipment (no suffix)

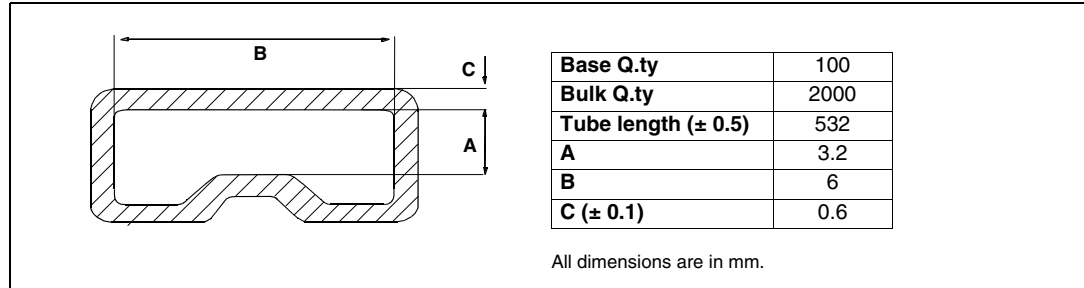
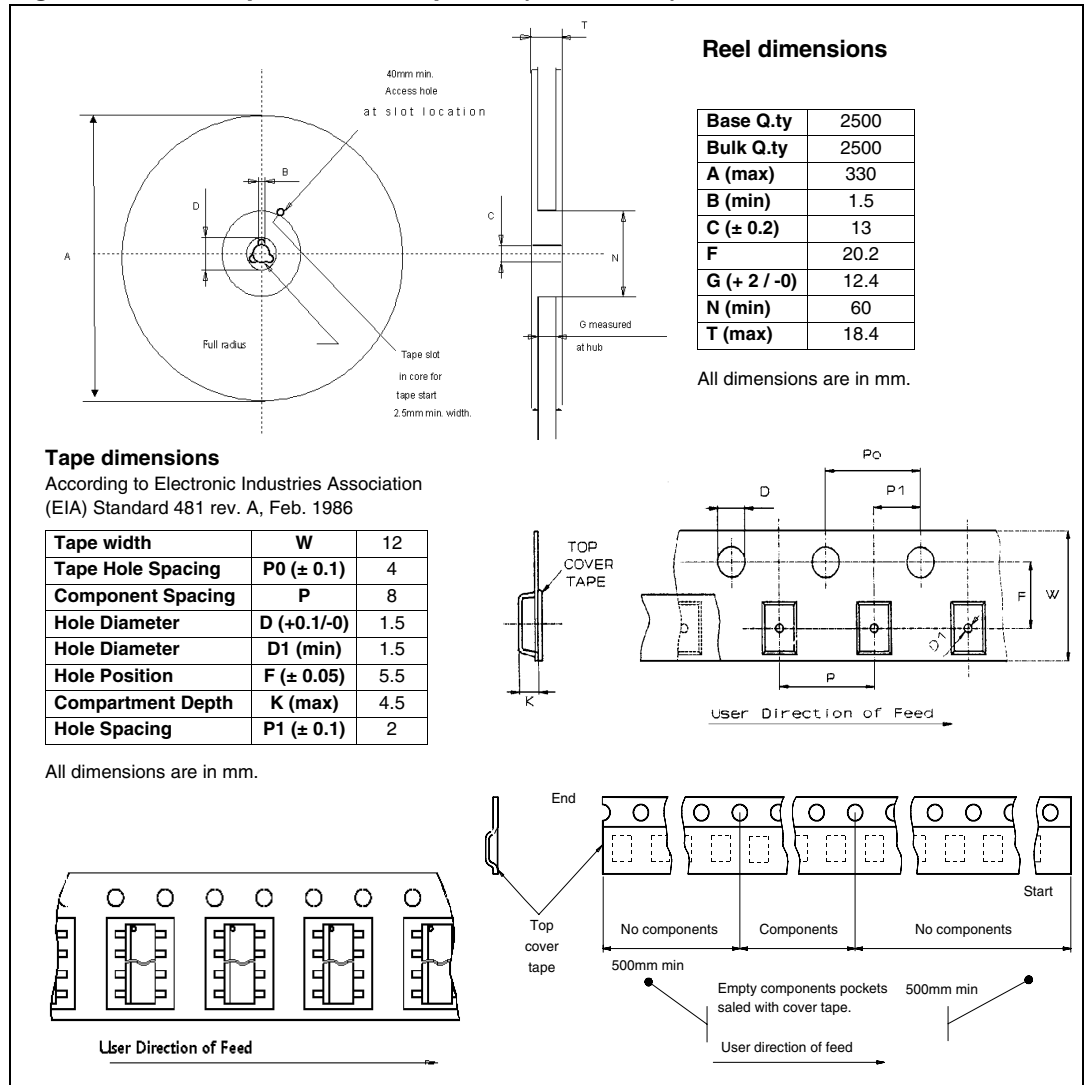


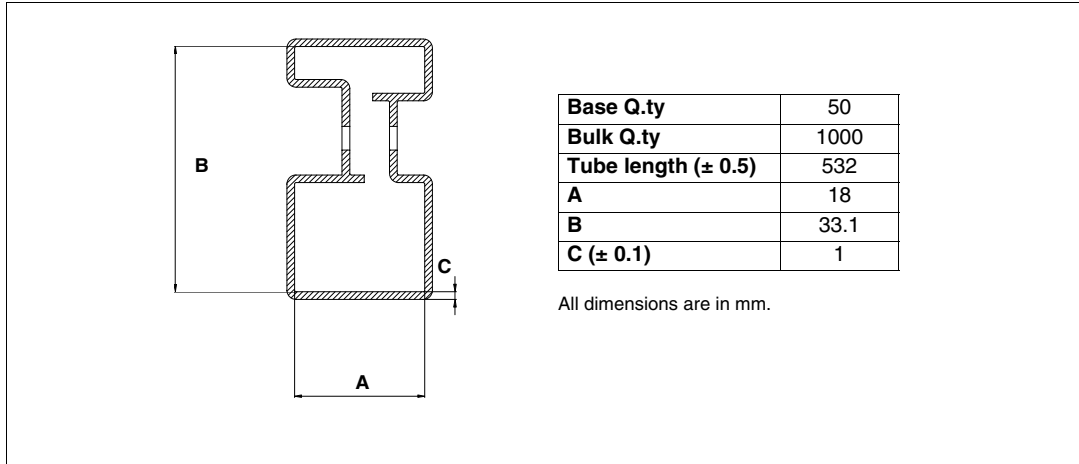
Figure 45. SO-8 tape and reel shipment (suffix “TR”)



4.7 PENTAWATT packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 46. PENTAWATT tube shipment (no suffix)



4.8 P²PAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 47. P²PAK tube shipment (no suffix)

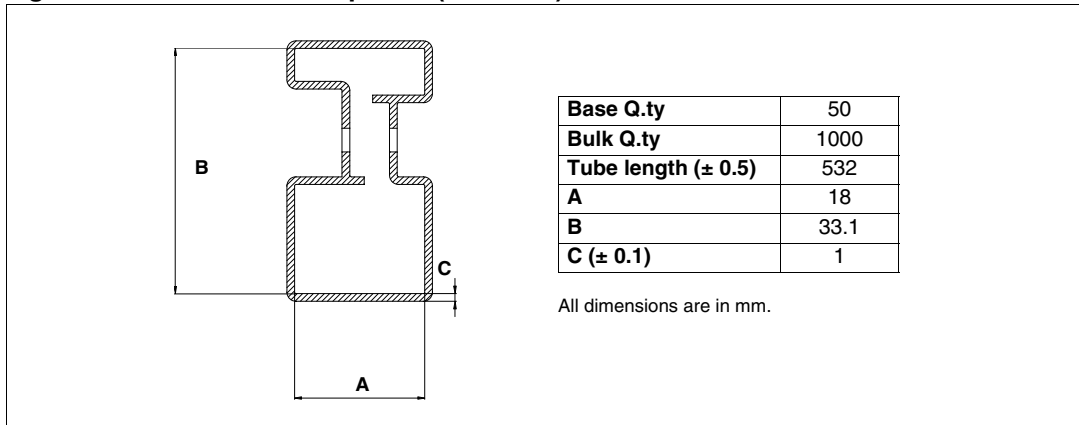
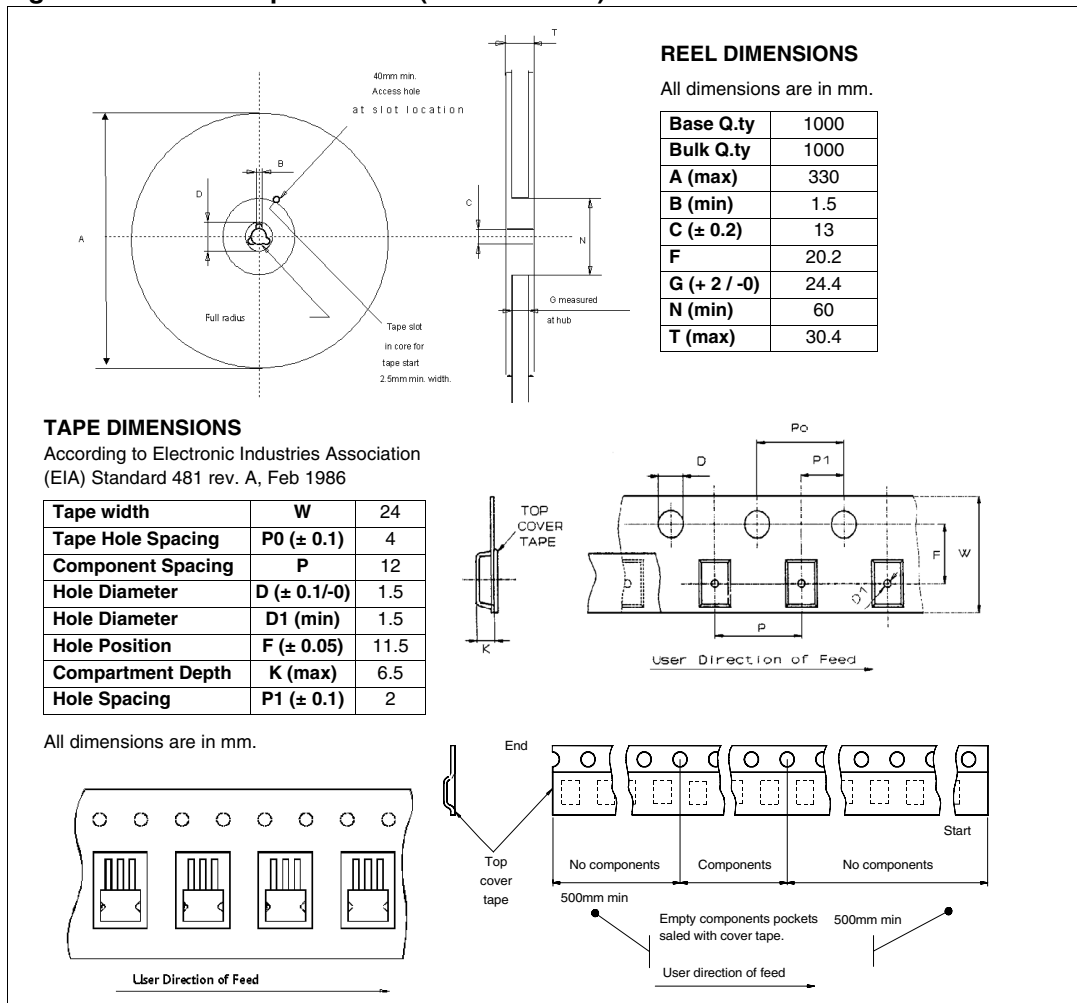


Figure 48. P²PAK tape and reel (suffix “13TR”)



4.9 PPAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 49. PPAK suggested pad layout

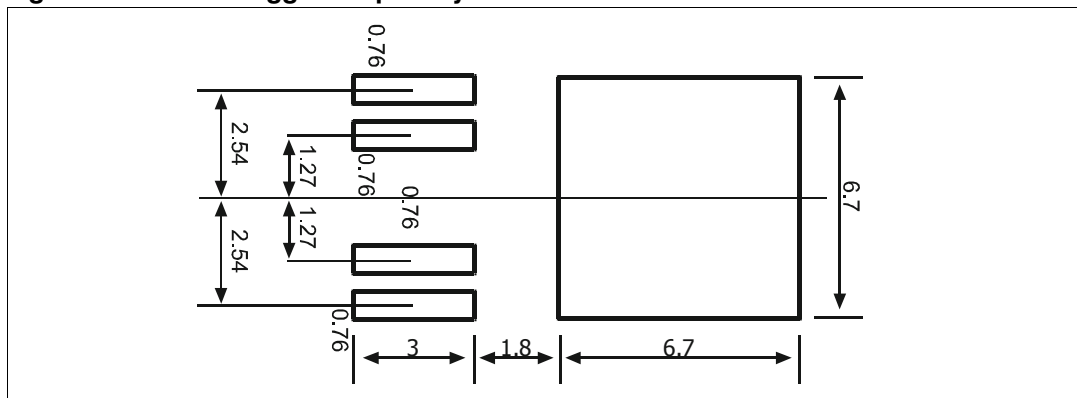


Figure 50. PPAK tube shipment (no suffix)

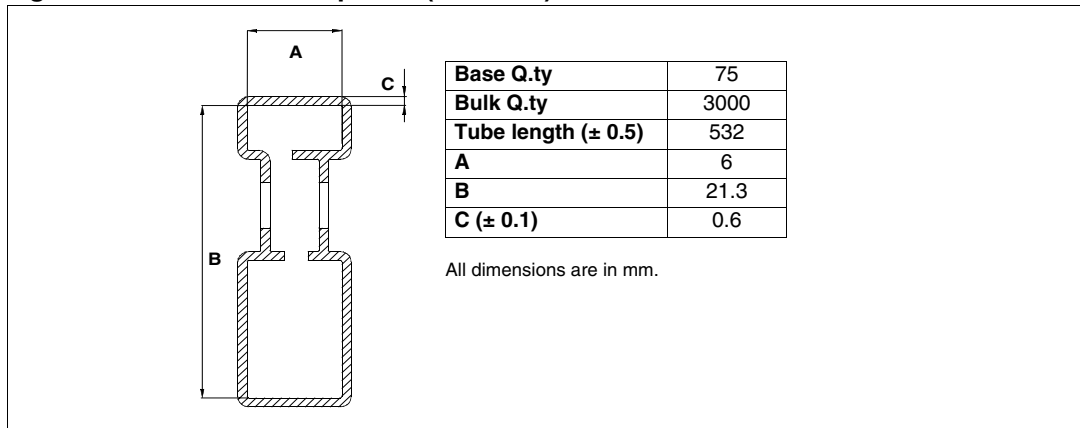
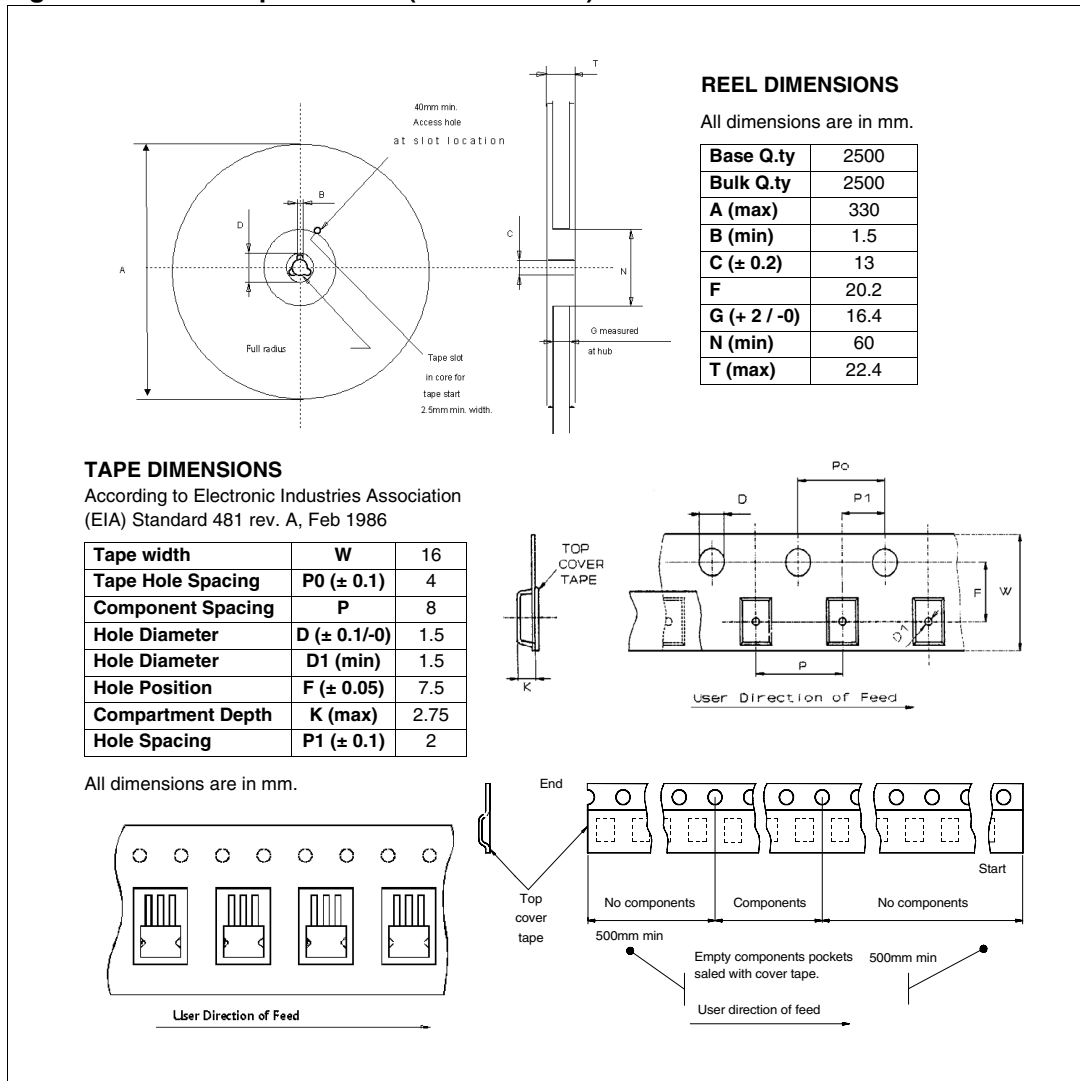


Figure 51. PPAK tape and reel (suffix "13TR")



5 Revision history

Table 21. Document revision history

Date	Revision	Changes
21-Jun-2004	1	Initial release.
03-May-2006	2	Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins: insertion (page 2). 6cm ² Cu condition insertion in thermal data table (page 3). V _{CC} - output diode section update (page 4). Revision history table insertion (page 30). Disclaimers update (page 31).
24-Nov-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK[®] packages</i> information. Updated <i>Figure 48.: P²PAK tape and reel (suffix "13TR")</i> : – changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com