AN1233
APPLICATION NOTE

LDMOS PACKAGES

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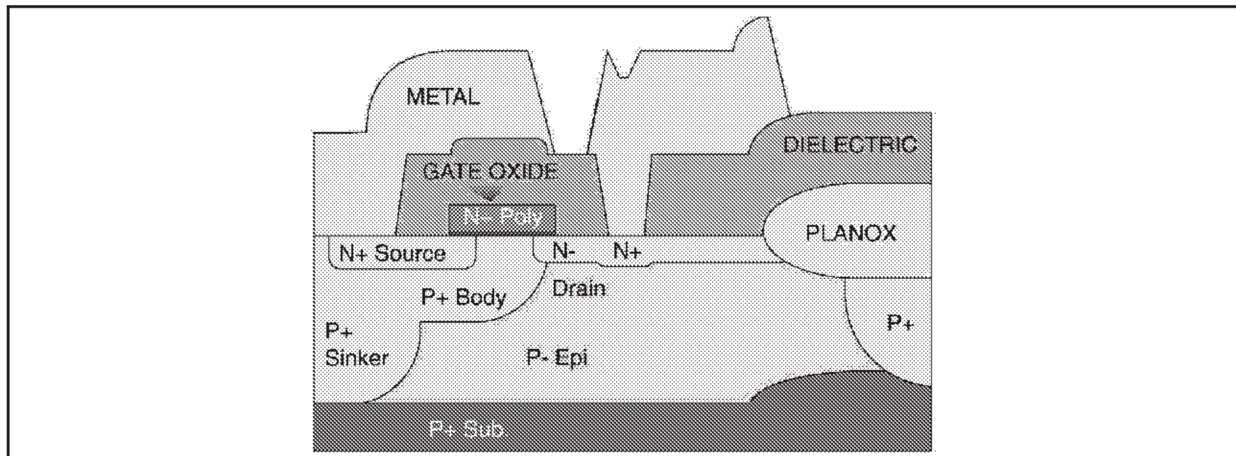
1. ABSTRACT

LDMOS technology recently implemented at ST is an important step forwards, combining technological and environmental progress. In the basic LDMOS structure (figure 1), a p-epitaxial layer is grown on an p-type substrate to form a larger drain region. An important consequence of this structure is that both the n+ source and the drain region are on the die surface, with the laterally diffused low resistance p+ sinker connecting the source region to the p+ substrate and source terminal. Wire-bonded connections which normally connect the source and the external circuitry (DMOS configuration) are no longer required thus greatly reducing the negative feedback due to wires self-capacitance and inductance. This leads to higher gain at high frequencies. A further advantage of this structure is that an electrical insulator required to isolate the drain with DMOS transistors is no longer needed. Hence not only electrical and thermal performances of the package are improved, but it also eliminates beryllium oxide, a toxic compound, from the package. LDMOS package development offers higher dissipated power, cost reduction and lower environmental impact.

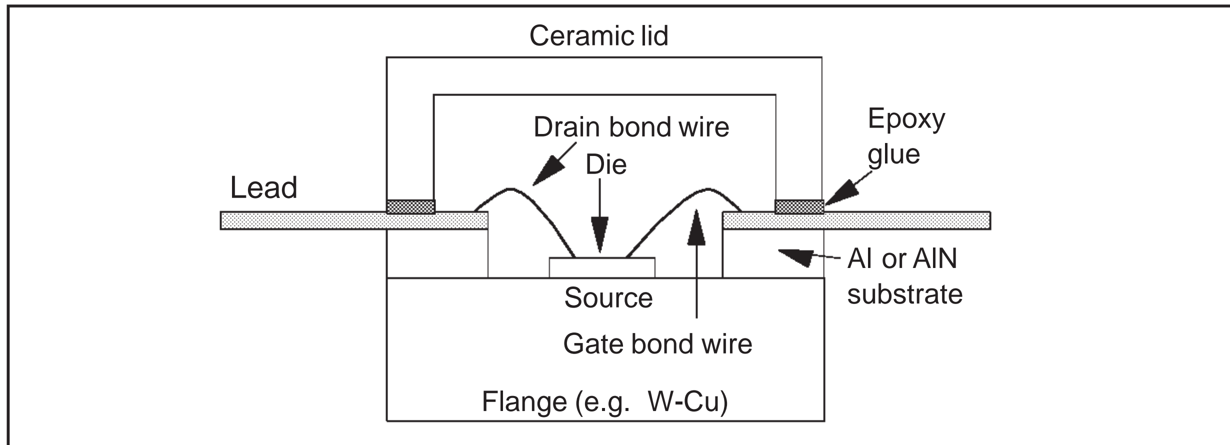
2. LDMOS PACKAGE STRUCTURE.

Figure 1: LDMOS Cross Section



In such a structure there is no need to electrically isolate the die from the flange as for bipolar die, by using a Beryllium Oxide (BeO) interface (figure 1 and 2). LDMOS package development eliminates any substances which could affect and/or deteriorate the environment. Therefore, because BeO is toxic it is no longer used. Moreover, the LDMOS die is soldered directly to the flange (For example, the tungsten-copper alloy flange).This results in better electrical and thermal performances.

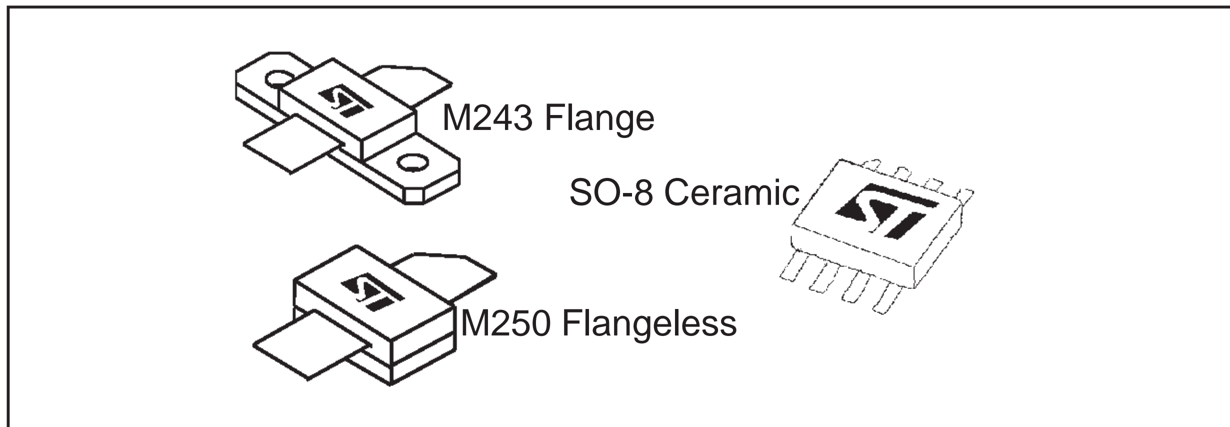
Figure 2: LDMOS Package Structure



3. MOUNTING TECHNIQUES AND CHARACTERISTICS.

Surface mount packages were developed to reduce assembly cost and space allocation on printed circuit board (PCB). Today, ST microelectronics offers three types of packages for its L-DMOS product: Flange, Flangeless and SMD (figure 3). Indeed all three package types have their own mounting techniques and characteristics:

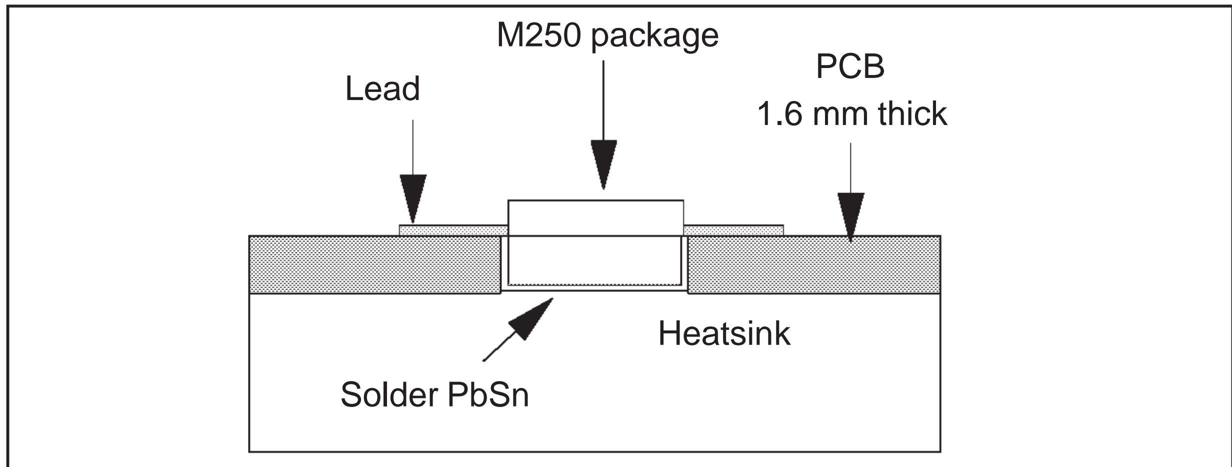
Figure 3: Package Styles



3.1 Flange Package (e.g. M243 package).

Heatsink flatness on the mounting area must be better than 0.02 mm. The mounting area roughness must be less than 0.5 µm. Flux solution is not needed. Because the package is non hermetically sealed, damage could occure. The PCB must be thouroughly washed clear of flux solution before mounting the RF transistor. Then a thin layer of thermal paste must be applied to the flange; however, an excessive thickness of thermal paste will increase the thermal resistance and one must stay cautious. Screws with a flat washer must be used in order to spread the pressure evenly on the joints. Each screw must be slightly tightened (finger tight: 0.05 Nm) and then the screws must be tightened to the specified torque. A typical torque value for M243 package is 0.65 Nm. Reflow soldering is the recommended mounting technique even though clamping can also be used. The backside of the package must be directly soldered to the heatsink. (See figure 4 for the flangeless package).

Figure 4: Flangeless Package Mounting



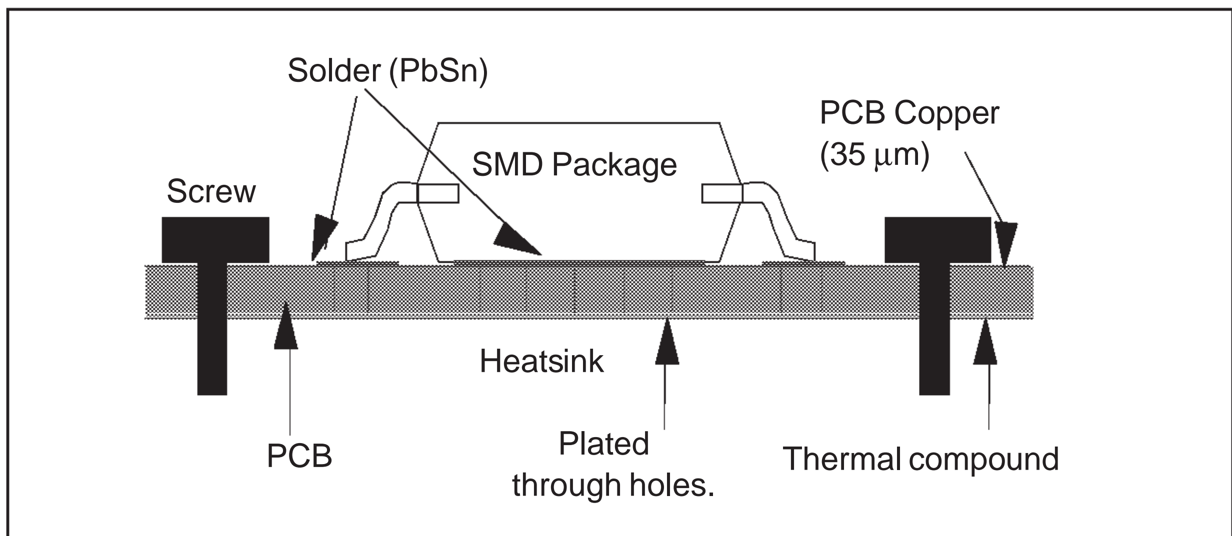
3.2. Flangeless Package (e.g. M250 package).

Reflow soldering is the recommended mounting technique even though the clamping method can also be used. The backside of the package must be directly soldered to the heatsink (see figure 4).

3.3. SMD Package (e.g. SO8 Ceramic).

Reflow soldering is the recommended mounting technique. Clamping can also be used. Dissipated power (heat) is mainly transferred by conduction from the device to the heatsink through the printed circuit board. Thermal resistance from the junction to the ambient must be reduced to a minimum value, hence all interfaces between the package and the ambient must be taken carefully into consideration (see figure 5). Metallized ground plate and leads contribute to the heat flow. So it is recommended to mount the device on a large grounded metallized area on the printed circuit board. Since the PCB is a poor thermal conductor (FR4, Duroid, etc.), it is also recommended to use thermal vias (plated through holes) to improve the heat conduction.

Figure 5: SMD Package Mounting



4. LOWERING THE THERMAL RESISTANCE BETWEEN JUNCTION AND AMBIENT.

In order to decrease the thermal resistance between the junction and the ambient one can consider undertaking the following actions:

1) Increase the number of plated through holes.

2) Increase the holes diameter. However, one must bare in mind that if the diameter is too large solder leaks out and forms solder balls beneath the PCB. This increases the thermal resistance between PCB and heatsink (0.5 mm < Hole diameter < 1.0 mm).

3) Decrease spacing between plated through holes.

4) Decrease thickness of the printed circuit board.

5) Use of a thin layer of thermal paste between PCB and heatsink.

6) Screw the PCB to the heatsink as close as possible to the package. The screws will also help heat flows to the heatsink (see figure 5).

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