KL5KUSB107

USB Combo - Serial & Parallel

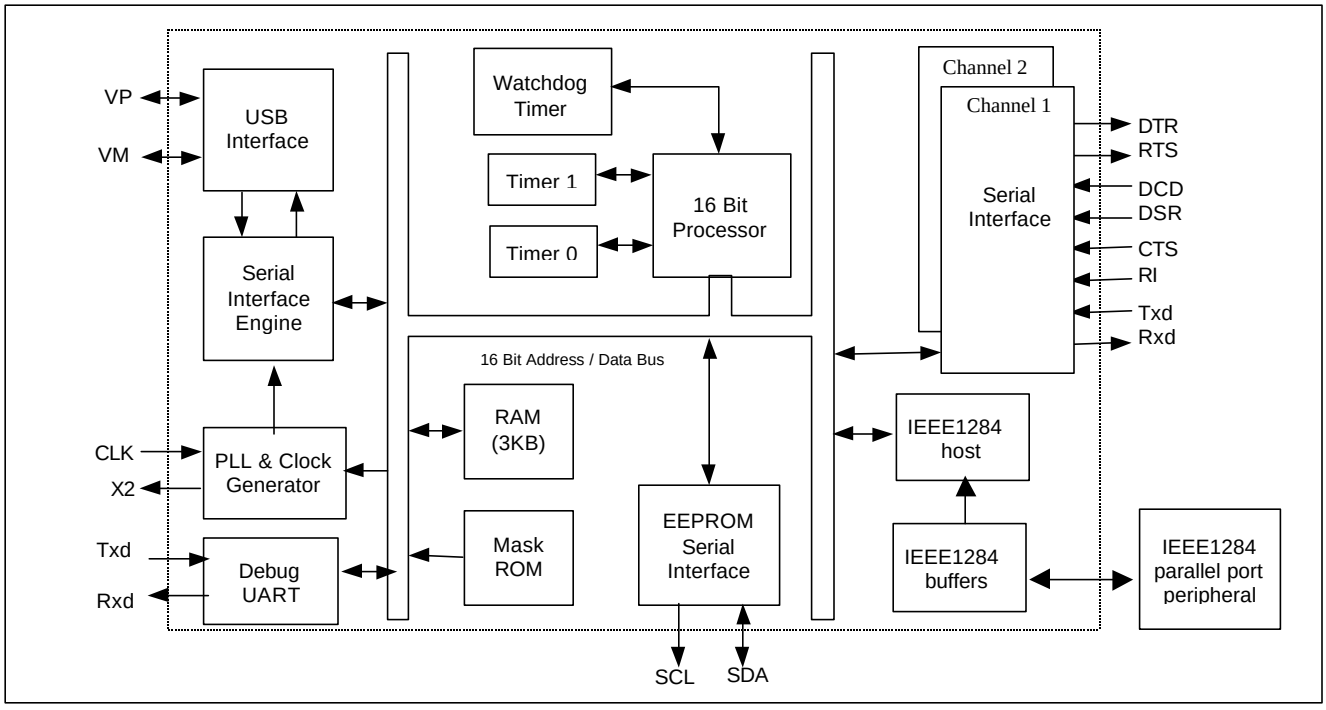
Description

The Kawasaki USB to Parallel / 2Serial enables your system to have the capability to communicate between the USB (Universal Serial Bus) port and parallel port and 2 serial ports. This device meets the USB 1.0/1.1 and IEEE1284 enhanced parallel port and standard serial port specifications. All the advantages of USB are available to peripherals with parallel and serial port interface. With Kawasaki's USB to Serial/Parallel device and software, it is transparent to the peripheral and no firmware changes are required which makes it possible to convert peripherals with serial and parallel interfaces to USB interface with minimum modifications. This device is ideal for Legacy solutions.

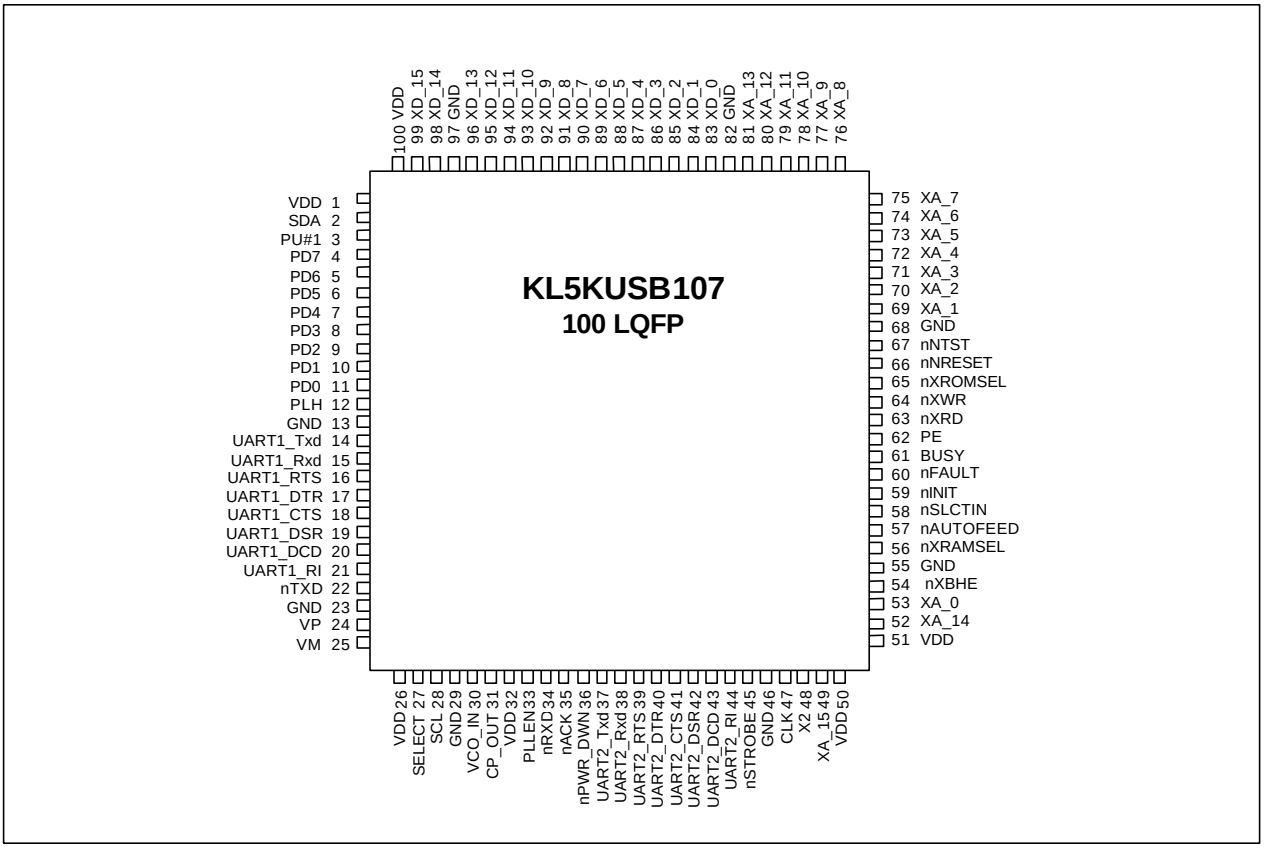
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- Compliant with the USB 1.0/1.1 (Universal Serial Bus)
- Plug and Play compatible
- Compliant with USB printer device class specification
- Utilizes low cost external crystal circuitry
- IEEE1284 compliant including EPP and ECP
- PC parallel port register-based standard operation
- 5V tolerate Centronics inputs pins.
- 2 serial ports
- 230Kbps serial baud rate
- 128 byte FIFO
- Serial EEPROM interface
- Utilizes low cost external crystal circuitry
- 1.5K x 16 internal RAM buffer for fast communications
- Debug UART for debug and code development
- USB host device drivers available
- Multiple logical channels support
- Single-chip solution in a 100 pin LQFP

Block Diagram



Pin Diagram 100LQFP



Pin Description

Pin # LQFP	I/O	Pin Name	Description
1		VDD	VDD
2	IN/OUT	SDA*	Serial EEPROM serial data. Connect to EEPROM/SDA for <=16Kb EEPROM, and EEPROM/SCL for >16Kb EEPROM
3	IN	PU#1*	Pull up to USB +Pin for High Speed
4	IN/OUT	PD7	Parallel port: Data7
5	IN/OUT	PD6	Parallel port: Data6
6	IN/OUT	PD5	Parallel port: Data5
7	IN/OUT	PD4	Parallel port: Data4
8	IN/OUT	PD3	Parallel port: Data3
9	IN/OUT	PD2	Parallel port: Data2
10	IN/OUT	PD1	Parallel port: Data1
11	IN/OUT	PD0	Parallel port: Data0
12	IN	PLH*	Parallel port: Peripheral Logic High
13		GND	GND
14	OUT	UART1_Txd*	UART1: Transmit Data
15	IN	UART1_Rxd*	UART1: Receive Data
16	OUT	UART1_RTS*	UART1: Request To Send
17	OUT	UART1_DTR*	UART1: Data Terminal Ready
18	IN	UART1_CTS*	UART1: Clear To Send
19	IN	UART1_DSR*	UART1: Data Set Ready
20	IN	UART1_DCD*	UART1: Data Carrier Detect
21	IN	UART1_RI*	UART1: Ring Indicate
22	OUT	nTXD	Debug UART Txd
23		GND	USB GND
24	IN/OUT	VP	USB DATA + Pin
25	IN/OUT	VM	USB DATA - Pin
26		VDD	USB VDD
27	IN	SELECT	Parallel port: Printer is selected and online
28	OUT	SCL*	Serial EEPROM clock. Connect to EEPROM/SCL for <=16Kb EEPROM, and EEPROM/SDA for >16Kb EEPROM
29		GND	GND
30	IN	VCO_IN	PLL VCO In
31	OUT	CP_OUT	PLL VCO Out
32		VDD	VDD
33	IN	PLLEN*	PLL Enable
34	IN	nRXD*	Debug UART Rxd
35	IN	nACK	Parallel port: Acknowledge
36	OUT	nPWR_DWN	Power Down
37	OUT	UART2_Txd*	UART2: Transmit Data
38	IN	UART2_Rxd*	UART2: Receive Data
39	OUT	UART2_RTS*	UART2: Request To Send
40	OUT	UART2_DTR*	UART2: Data Terminal Ready
41	IN	UART2_CTS*	UART2: Clear To Send
42	IN	UART2_DSR*	UART2: Data Set Ready
43	IN	UART2_DCD*	UART2: Data Carrier Detect

Pin # LQFP	I/O	Pin Name	Description
44	IN	UART2_RI*	UART2: Ring Indicate
45	IN/OUT	nSTROBE	Parallel port: Strobe
46		GND	GND
47	IN	CLK	12MHz Clock/Crystal Input
48	OUT	X2	12MHz Crystal Output
49	OUT	XA_15	External Memory Address Pin
50		VDD	VDD
51		VDD	VDD
52	OUT	XA_14	External Memory Address Pin
53	OUT	XA_0	External Memory Address Pin
54	OUT	nXBHE	External Memory byte High Enable (Active low)
55		GND	GND
56	OUT	nXRAMSEL	External RAM CS (Active low)
57	OUT	nAUTOFEED	Parallel port: Auto feed
58	OUT	nSLCTIN	Parallel port: Select
59	OUT	nINIT	Parallel port: Initialize
60	IN	nFAULT	Parallel port: Error
61	IN	BUSY	Parallel port: Busy
62	IN	PE	Parallel port: Paper end or error
63	OUT	nXRD	External Memory Read (Active low)
64	OUT	nXWR	External Memory Write (Active low)
65	OUT	nXROMSEL	External ROM CS (Active low)
66	IN	nNRESET	Reset Pin
67	IN	nNTST*	Test Pin, *Disconnect for Normal Operation*
68		GND	GND
69	OUT	XA_1	External Memory Address Pin
70	OUT	XA_2	External Memory Address Pin
71	OUT	XA_3	External Memory Address Pin
72	OUT	XA_4	External Memory Address Pin
73	OUT	XA_5	External Memory Address Pin
74	OUT	XA_6	External Memory Address Pin
75	OUT	XA_7	External Memory Address Pin
76	OUT	XA_8	External Memory Address Pin
77	OUT	XA_9	External Memory Address Pin
78	OUT	XA_10	External Memory Address Pin
79	OUT	XA_11	External Memory Address Pin
80	OUT	XA_12	External Memory Address Pin
81	OUT	XA_13	External Memory Address Pin
82		GND	GND
83	IN/OUT	XD_0*	External Memory Data Pin
84	IN/OUT	XD_1*	External Memory Data Pin
85	IN/OUT	XD_2*	External Memory Data Pin
86	IN/OUT	XD_3*	External Memory Data Pin
87	IN/OUT	XD_4*	External Memory Data Pin
88	IN/OUT	XD_5*	External Memory Data Pin
89	IN/OUT	XD_6*	External Memory Data Pin
90	IN/OUT	XD_7*	External Memory Data Pin
91	IN/OUT	XD_8*	External Memory Data Pin
92	IN/OUT	XD_9*	External Memory Data Pin

Pin # LQFP	I/O	Pin Name	Description
93	IN/OUT	XD_10*	External Memory Data Pin
94	IN/OUT	XD_11*	External Memory Data Pin
95	IN/OUT	XD_12*	External Memory Data Pin
96	IN/OUT	XD_13*	External Memory Data Pin
97		GND	GND
98	IN/OUT	XD_14*	External Memory Data Pin
99	IN/OUT	XD_15*	External Memory Data Pin
100		VDD	VDD

*Pins are 5V tolerant.

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM in the this device or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers

The processor supports prioritized vectored hardware interrupts and has as many as 240 software interrupt vectors.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

The Processor – Divide/Multiply function

The processor's divide/multiply function contains all the instructions of the base processor that additionally includes integer divide and multiply instructions. A signed multiply instructions takes two 16-bit operands and returns a 32-bit result. A signed divide instruction divides a 32-bit operand by a 16-bit operand.

RAM Buffer

The USB controller contains internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal 48MHz clock. This circuitry is designed to allow use of a low cost 12 MHz external crystal which is connected to CLK and X2. If an external 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit and connected directly to the CLK input pin.

USB Interface

The USB controller meets the Universal Serial Bus (USB) specification ver 1.0/1.1. The transceiver is capable of transmitting and receiving serial data at the USB's full speed, 12 Mbits/sec data rate. The driver portion of the transceiver is differential, while the receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally, the transceiver connects to the physical layer of the USB.

Debug UART

An independent UART serial port is provided for debug and code development. The port can be configured for a wide selection of baud rates, 7200 to 115.2K baud. The port provides transmit and receive data support only.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface can support a variety of serial EEPROM formats.

Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_{IN} (Normal)	-0.3 to V_{DD}+0.3	V
	V_{IN} (5V Tolerant)	-0.3 to 6.0	V
Storage Temperature	TSTG	-55 to 125	°C

DC Characteristics and conditions (V_{DD} @ 3.3V±.3V)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0	-	-	V
V_{IL}	Input low voltage		-	-	0.8	V
V+ *	Input high voltage	Schmitt	-	1.8	2.3	V
V- *	Input low voltage	Schmitt	0.5	0.9	-	V
V_H*	Hysteresis voltage	Schmitt	0.4	-	-	V
I_{IH}	Input high current	$V_{IN} = V_{DD}$	-10	-	10	µA
I_{IL}	Input low current	$V_{IN} = V_{ss}$	-10	-	10	µA
V_{OH}	Output high voltage		2.4	-	-	V
V_{OL}	Output low voltage		-	-	0.4	V
I_{OZ}	3-state leakage current	$V_{OH}=V_{SS}$	-10	-	10	µA
		$V_{OL}=V_{DD}$	-10	-	-10	µA

*For reset pin (nNRESET, pin 66)