

FDN359AN N-Channel Logic Level PowerTrench™ MOSFET

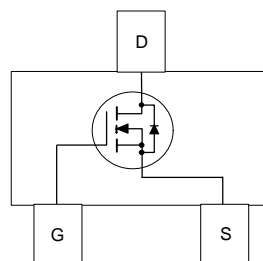
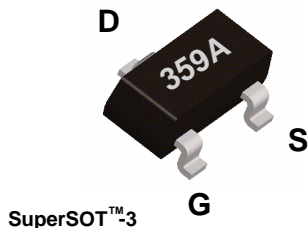
General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 2.7 A, 30 V. $R_{DS(ON)} = 0.046 \Omega @ V_{GS} = 10 V$
 $R_{DS(ON)} = 0.060 \Omega @ V_{GS} = 4.5 V.$
- Very fast switching.
- Low gate charge (5nC typical).
- High power version of industry standard SOT-23 package. Identical pin out to SOT-23 with 30% higher power handling capability.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Maximum Drain Current - Continuous (Note 1a)	2.7	A
	- Pulsed	15	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$		23		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1	μA
					10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.7\text{ A}$ $T_J = 125^\circ\text{C}$		0.037	0.046	Ω
				0.055	0.075	
			$V_{GS} = 4.5\text{ V}, I_D = 2.4\text{ A}$	0.049	0.06	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	15			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.7\text{ A}$		9.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		480		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
SWITCHING CHARACTERISTICS (Note)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 5\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		6	12	ns
t_r	Turn - On Rise Time			13	24	ns
$t_{D(off)}$	Turn - Off Delay Time			15	27	ns
t_f	Turn - Off Fall Time			4	10	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 2.7\text{ A},$ $V_{GS} = 5\text{ V}$		5	7	nC
Q_{gs}	Gate-Source Charge			1.4		nC
Q_{gd}	Gate-Drain Charge			1.6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note)		0.65	1.2	V

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on FR-4 PCB in a still air environment :



a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz Cu.



b. 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

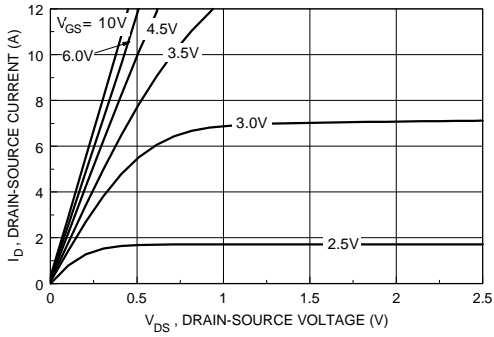


Figure 1. On-Region Characteristics.

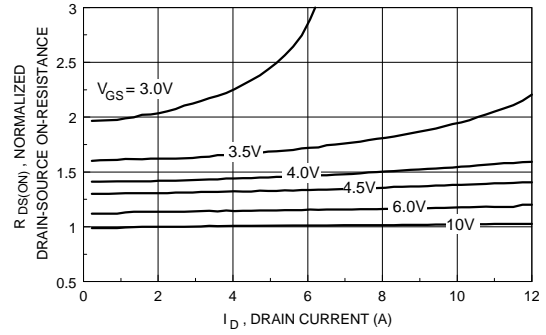


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

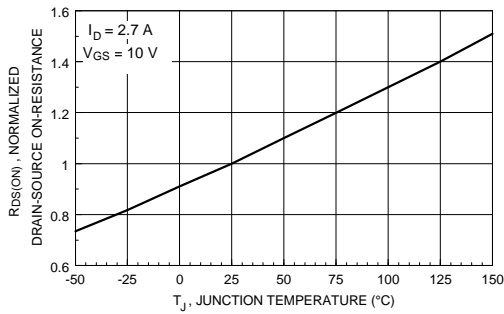


Figure 3. On-Resistance Variation with Temperature.

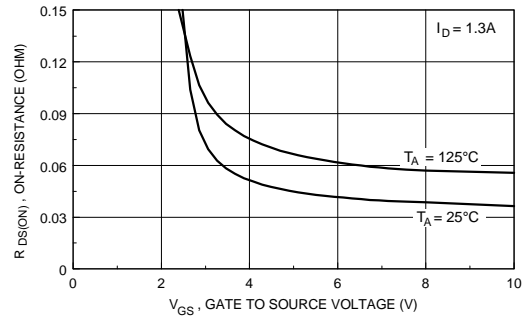


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

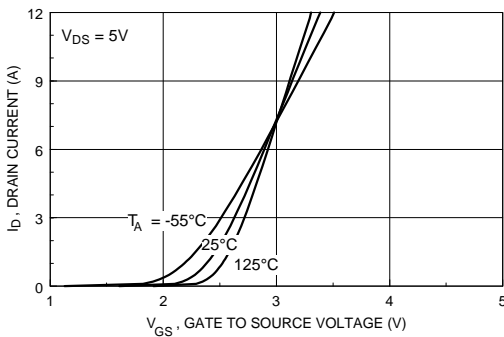


Figure 5. Transfer Characteristics.

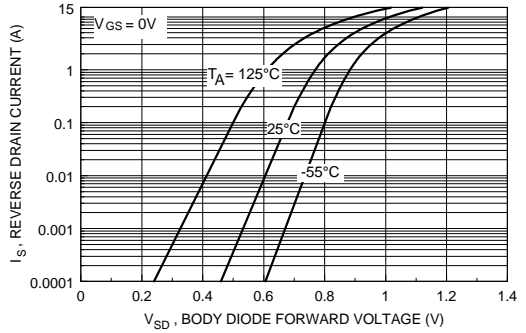


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics

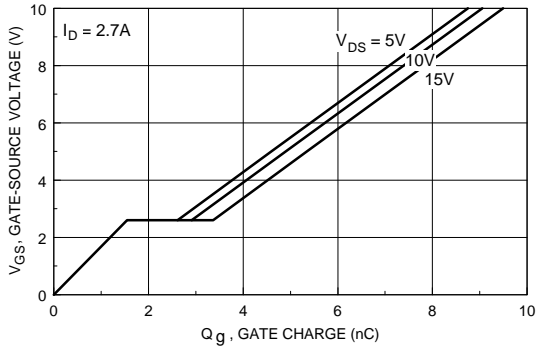


Figure 7. Gate Charge Characteristics.

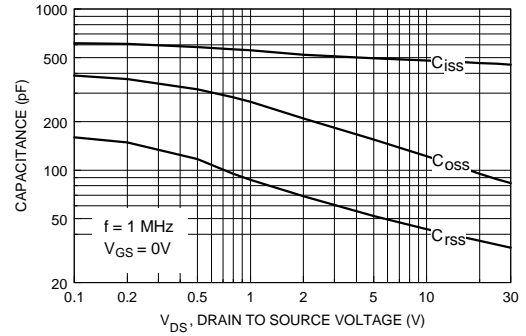


Figure 8. Capacitance Characteristics.

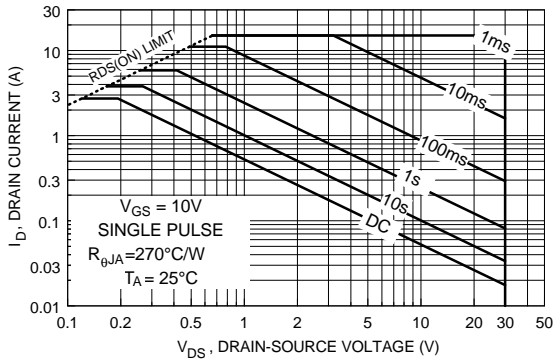


Figure 9. Maximum Safe Operating Area.

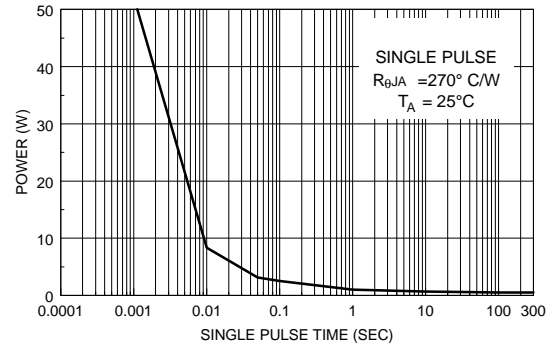


Figure 10. Single Pulse Maximum Power Dissipation.

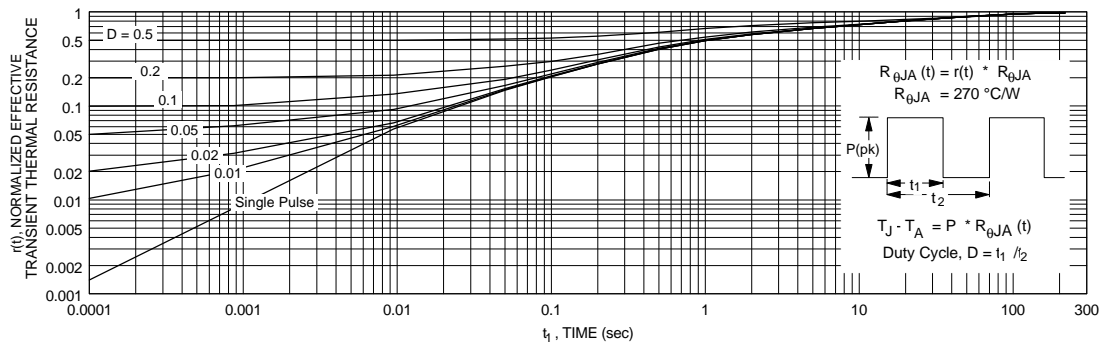
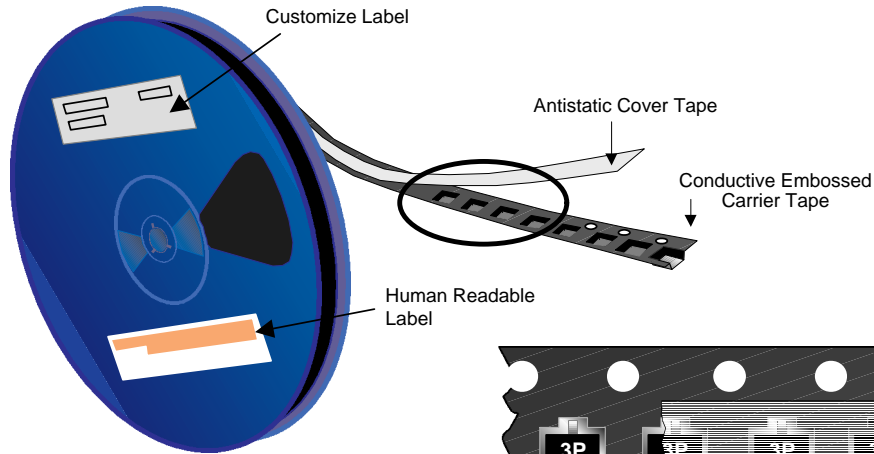


Figure 11. Transient Thermal Response Curve.

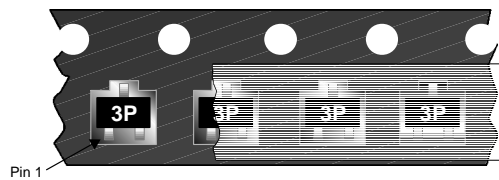
Thermal characterization performed using the conditions described in note 1b.
Transient thermal response will change depending on the circuit board design.

SuperSOT™-3 Tape and Reel Data and Package Dimensions

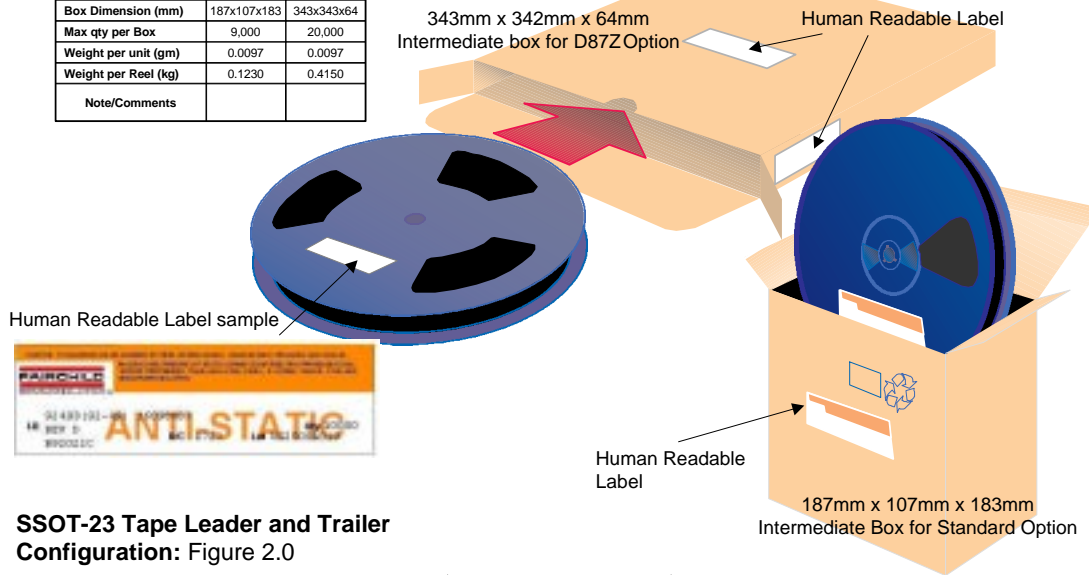
SSOT-3 Packaging Configuration: Figure 1.0



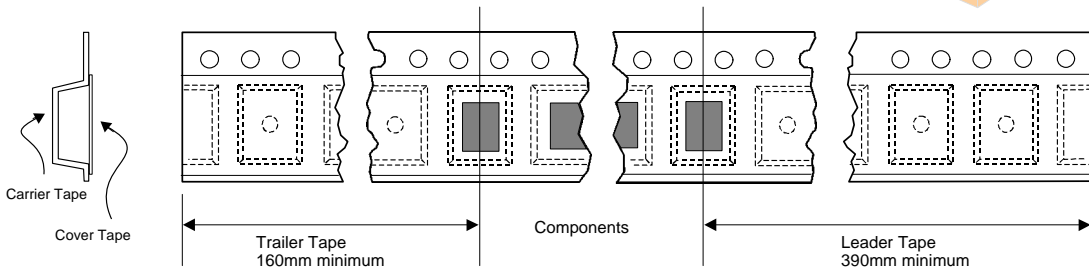
SSOT-3 Std Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	187x107x183	343x343x64
Max qty per Box	9,000	20,000
Weight per unit (gm)	0.0097	0.0097
Weight per Reel (kg)	0.1230	0.4150
Note/Comments		



SSOT-3 Std Unit Orientation

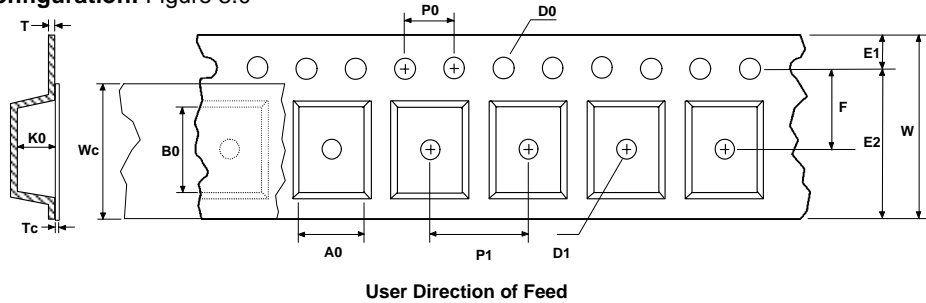


SSOT-23 Tape Leader and Trailer Configuration: Figure 2.0



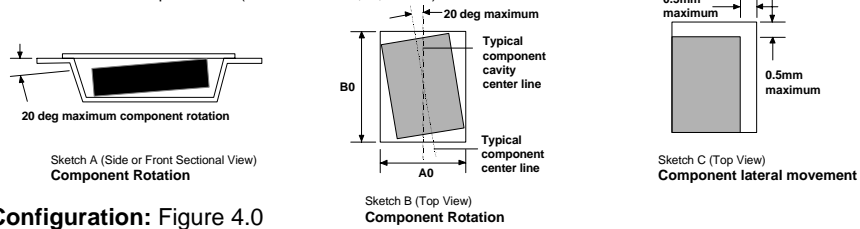
SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

SSOT-3 Embossed Carrier Tape Configuration: Figure 3.0

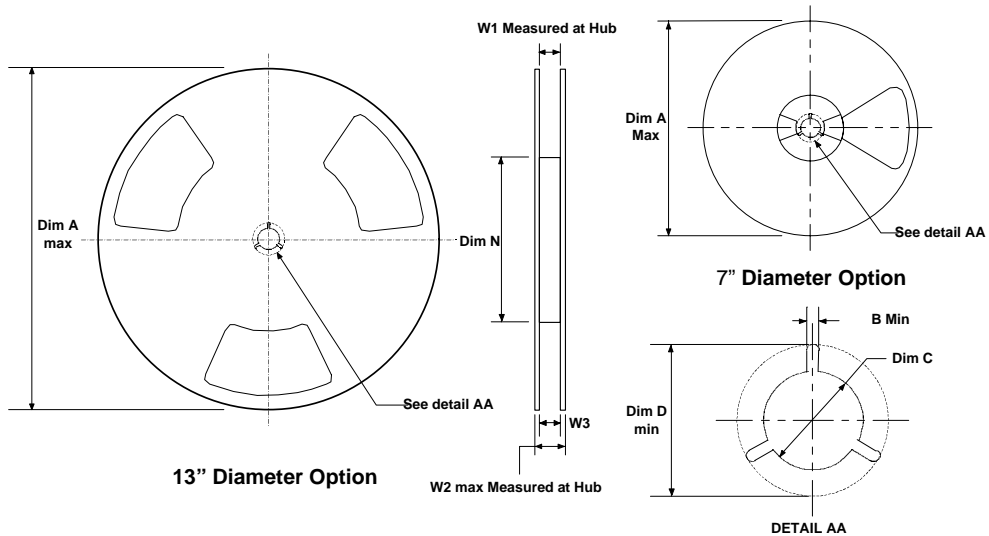


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.00 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



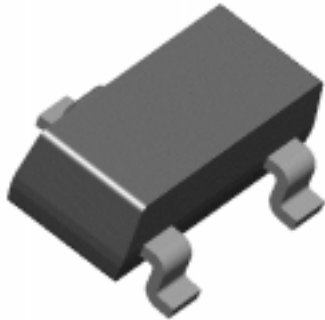
SSOT-3 Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

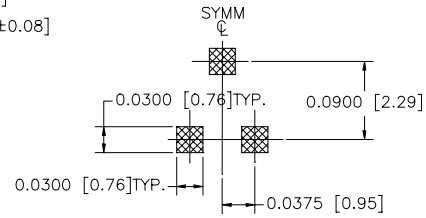
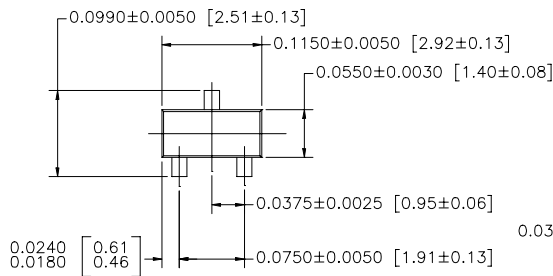
SuperSOT™-3 (FS PKG Code 32)



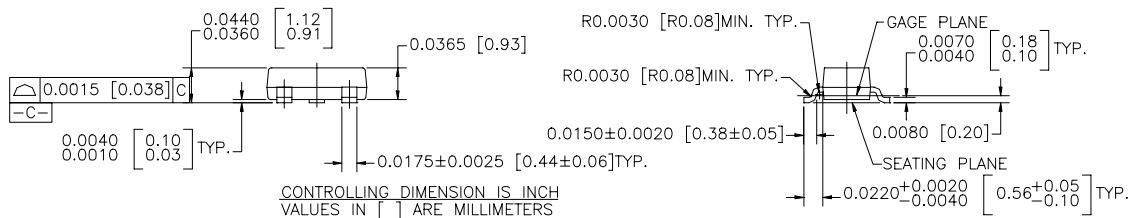
Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097



LAND PATTERN RECOMMENDATION



NOTES : UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

- STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
- NO JEDEC REGISTRATION AS OF DEC. 1995.

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