

MN39471PT

Diagonal 6.9 mm (type-1/3) 1 800 H CCD Area Image Sensor

■ Overview

The MN39471PT is a super high resolution CCD area image sensor which includes 2 310 k pixels in type-1/3 image format size.

Adopting RGB Bayer arrangement in primary color filter array on chip provides excellent color reproduction. As the aspect ratio of image area is 3:2 which is the same as that of 35mm film, pictures can be taken in similar framing manner to use of a usual film camera.

As The MN39471PT has also a skipping readout mode for image monitoring by LCD panel, you can fix the composition in real time.

Part Number	Size	Scanning mode	Color or B/W
MN39471PT	6.9mm (type-1/3)	IS *	Color

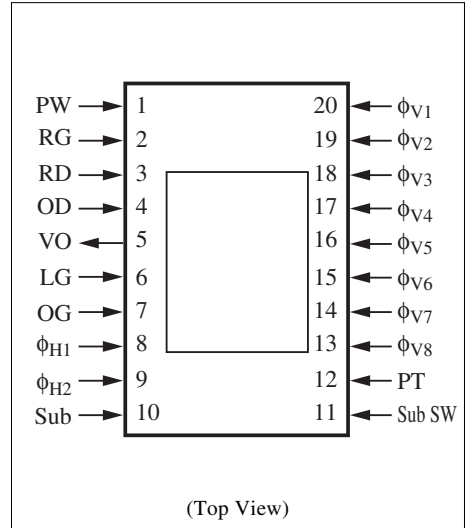
Note) Interlace scan

■ Features

- Photographic grade super high resolution by 2 310 k pixels in type-1/3 format
- Responds to 5 : 1 skipping readout mode for LCD monitoring
- The same aspect ratio of 3 : 2 as a 35 mm film
- Newly developed small plastic package

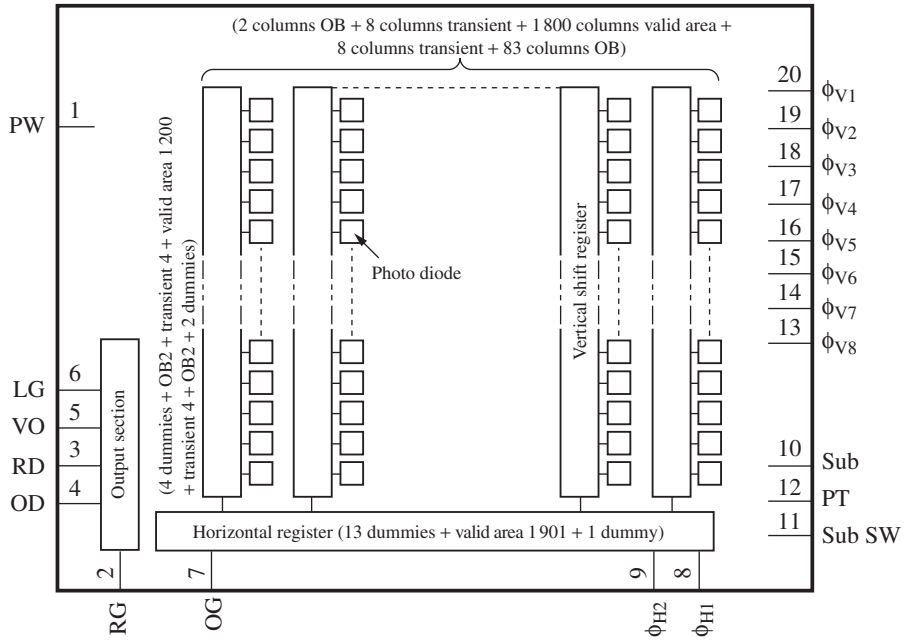
■ Applications

- Digital still camera
- FA, OA cameras

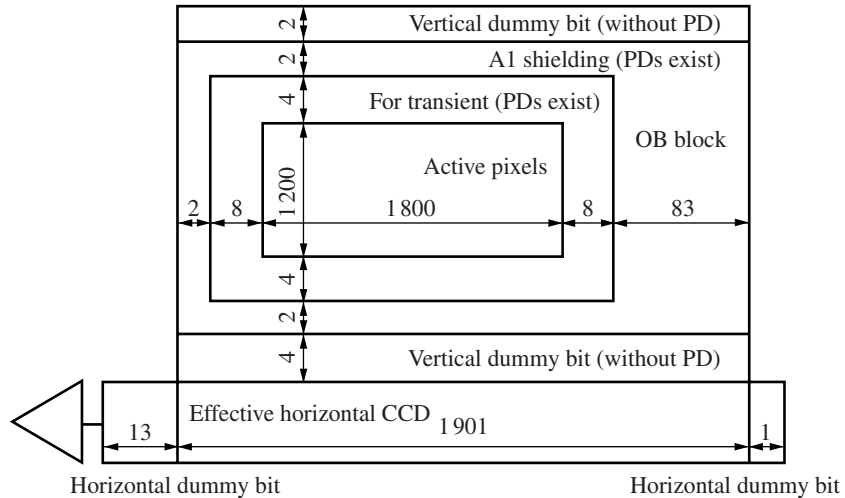


■ Block Diagram

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■ Element Construction



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	PW	P-well	11	SubSW	Substrate potential control
2	RG	Reset gate	12	PT	P-well for protection circuit
3	RD	Reset drain	13	ϕ_{V8}	Vertical shift register clock pulse 8
4	OD	Output drain	14	ϕ_{V7}	Vertical shift register clock pulse 7
5	VO	CCD output	15	ϕ_{V6}	Vertical shift register clock pulse 6
6	LG	Output load transistor gate	16	ϕ_{V5}	Vertical shift register clock pulse 5
7	OG	Output gate	17	ϕ_{V4}	Vertical shift register clock pulse 4
8	ϕ_{H1}	Horizontal shift register clock pulse 1	18	ϕ_{V3}	Vertical shift register clock pulse 3
9	ϕ_{H2}	Horizontal shift register clock pulse 2	19	ϕ_{V2}	Vertical shift register clock pulse 2
10	Sub	Substrate	20	ϕ_{V1}	Vertical shift register clock pulse 1

■ Device Parameter (H × V)

Parameter	Value	Unit
Total pixel number	1 901 × 1 212	pixel
Effective pixel number	1 816 × 1 208	pixel
Active pixel number	1 800 × 1 200	pixel
Image sensing block dimension	5.76 × 3.84	mm ²
Pixel dimension	3.2 × 3.2	μm ²

■ Absolute Maximum Ratings and Operating Conditions

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		min	max	min	typ	max		
Output drain voltage	V_{OD}	-0.2	18.0	15.0	15.5	16.0	V	
Reset drain voltage	V_{RD}	-0.2	18.0	15.0	15.5	16.0	V	
Protection P-well voltage ^{*5, 7}	V_{PT}	-10.0	0.2	-8.5	-8.0	-7.5	V	
P-well voltage	V_{PW}	Reference voltage		—	0	—	V	
Output load transistor gate voltage ^{*6}	V_{LG}	—	—	Supplied internally			V	
Output gate voltage ^{*6}	V_{OG}	—	—	Supplied internally			V	
Reset pulse voltage ^{*1}	High-Low	$V_{\phi R}$	—	8.0	3.0	3.3	3.6	V
	Bias		-0.5	—	Supplied internally			
Horizontal register clock pulse voltage 1 ^{*3}	High	$V_{\phi H1}$	—	8.0	3.0	3.3	3.6	V
	Low		-0.2	—	-0.2	0	0.2	
Horizontal register clock pulse voltage 2 ^{*3}	High	$V_{\phi H2}$	—	8.0	3.0	3.3	3.6	V
	Low		-0.2	—	-0.2	0	0.2	
Substrate voltage ^{*2}		V_{Sub}	—	—	Supplied internally			V
		ϕV_{Sub}	-0.2	35.5	25.0	26.0	27.0	
For electronic shutter substrate potential control voltage	High	SubSW	—	8.0	3.0	3.3	3.6	V
	Low		-0.2	—	-0.2	0	+0.2	
Vertical shift register clock pulse voltage 1, 5 ^{*4, 5, 7}	High	$V_{\phi V1}$,	—	18.0	15.0	15.5	16.0	V
	Middle	$V_{\phi V5}$	—	—	-0.2	0	0.2	
	Low		-10.0	—	-8.5	-8.0	-7.5	
Vertical shift register clock pulse voltage 2, 6 ^{*4, 5, 7}	Middle	$V_{\phi V2}$,	—	15.0	-0.2	0	0.2	V
	Low	$V_{\phi V6}$	-10.0	—	-8.5	-8.0	-7.5	
Vertical shift register clock pulse voltage 3, 7 ^{*4, 5, 7}	High	$V_{\phi V3}$,	—	18.0	15.0	15.5	16.0	V
	Middle	$V_{\phi V7}$	—	—	-0.2	0	0.2	
	Low		-10.0	—	-8.5	-8.0	-7.5	
Vertical shift register clock pulse voltage 4, 8 ^{*4, 5, 7}	Middle	$V_{\phi V4}$,	—	15.0	-0.2	0	0.2	V
	Low	$V_{\phi V8}$	-10.0	—	-8.5	-8.0	-7.5	
Operating temperature	T_{opr}	-10	60	—	25	—	°C	
Storage temperature	T_{stg}	-30	70	—	—	—	°C	

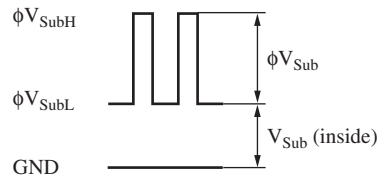
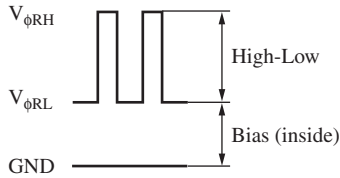
■ Absolute Maximum Ratings and Operating Conditions (continued)

Note) 1. Standard photo detecting condition

Standard photo detecting condition stands for detecting image with a light source of color temperature of 2 856K, luminance of 1 050 cd/m², and using a color temperature conversion filter LB-40 (HOYA), infrared cut filter CAW-500S with thickness 2.5 mm for a light path and with F8 lens aperture. The quantity of the incidental light to a photo-detecting surface under the above condition is defined as the standard quantity of light.

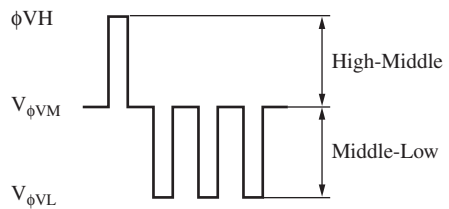
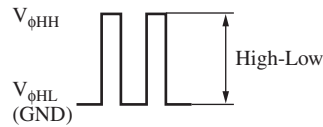
2.*1: Reset

*2: V_{Sub} for electronic shutter



*3: Horizontal transfer pulse ($V_{\phi H}$)

*4: Vertical transfer pulse (readout pulse)



*5: Absolute maximum ratings $-0.2 < V_{\phi V} - V_{PT} < 28.0$ (V)

*6: GND

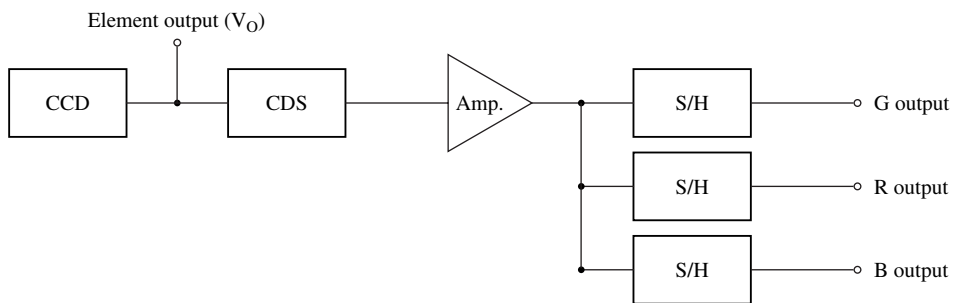
Ground LG and OG pin with each capacitor of 0.047 μ F or more.

*7: Relation between V_{PT} and $V_{\phi VL}$

Set V_{PT} under the following condition against VL of a vertical transfer clock waveform.

$$V_{PT} \leq VL (V_{\phi VL} \text{ to } V_{\phi VL})$$

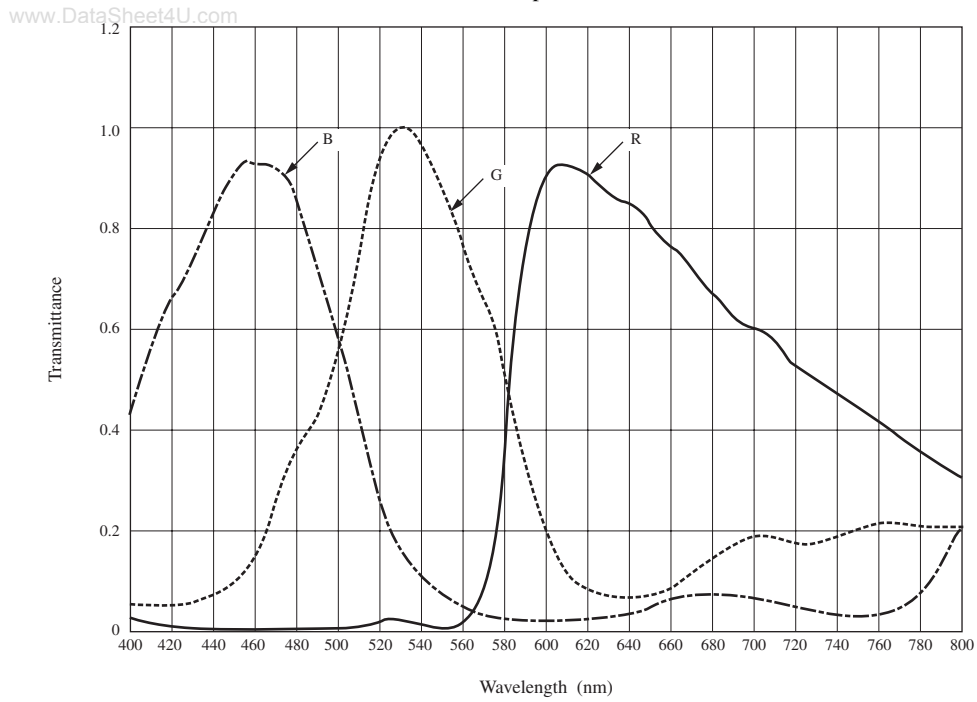
3. Measuring point



Adjust the amp. gain for 1 regarding V_{O-G} , V_{O-R} and V_{O-B} outputs.

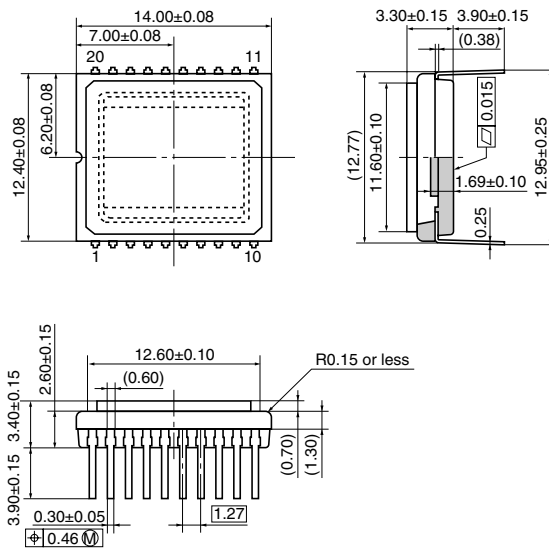
■ Graphs of Characteristics

CCD Color Filter Spectral Characteristics



■ Package Dimensions (Unit: mm)

- WDIP020-P-0500A



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