VITESSE
SEMICONDUCTOR CORPORATION

Data Sheet

VSC864A-2

200 Mb/s 64 x 64 Crosspoint Switch

Features

- 200 Mb/s Operation
- Duty-cycle Distortion: ≤ 10%
- Clocked or Flow-through Operation
- ECL 100K Compatible I/O
- ≤ 1500 ps Output to Output Skew (clocked mode)
- 25Ω Output Drive
- Power Dissipation: 9.4 Watts (Typ.)
- Single Power Supply: -2 V ± 5%
- Commercial (0° to +70° C) or Industrial (-40° to +85° C) Temperature Ranges
- Full Diagnostic Monitors
- Cascadable for Larger System Requirements
- Package: 344-pin Ceramic LDCC

General Description

The VSC864A-2 is a 64 x 64 crosspoint switch intended for high speed (up to 200 Mb/s) digital data communications applications. This product has 64 data inputs and 64 data outputs. Any input can be multiplexed to any, some, or all outputs. High speed digital data up to 200 Mb/s can be switched with less than 20% pulse width distortion. In broadcast mode, any two outputs will exhibit less than 1500 ps of skew. All interfaces are fully compatible with ECL F100K logic levels. The VSC864A-2 requires only a single -2 V power supply.

A separate Q bus is provided to allow observation of individual internal multiplexer address latches. Since the VSC864A-2 outputs are capable of driving 25Ω double-terminated buses with cutoff drivers, the device can be cascaded to form larger crosspoint switches. The VSC864A-2 Crosspoint Switch can be operated in either flow-through or synchronous mode by use of internal input and output data registers. In flow-through mode the data propagation delay is less than 5.8 ns.

The individual address registers in the VSC864A-2 are double buffered. A local strobe signal is used to load an individual address for each output pin. A global strobe is used to simultaneously activate all 64 destination addresses.

This product is ideal for high speed digital applications including data distribution for telecommunications, computer network and multiprocessor switching, and test equipment. In a telecommunications SONET application, for example, the VSC864A-2 can be used as an STS-3 protection switch, or in the fabric of a large switching system.

The VSC864A-2 is packaged in a 344 pin ceramic LDCC package and typically dissipates less than 10 W. This product is fabricated using Vitesse's simple, high yielding, E/D GaAs MESFET process which achieves high speed coupled with low power dissipation.

Functional Description

The VSC864A-2 may be used to connect any one of 64 inputs to any combination of 64 output channels, according to a user defined bit pattern stored in each channel's control latch.

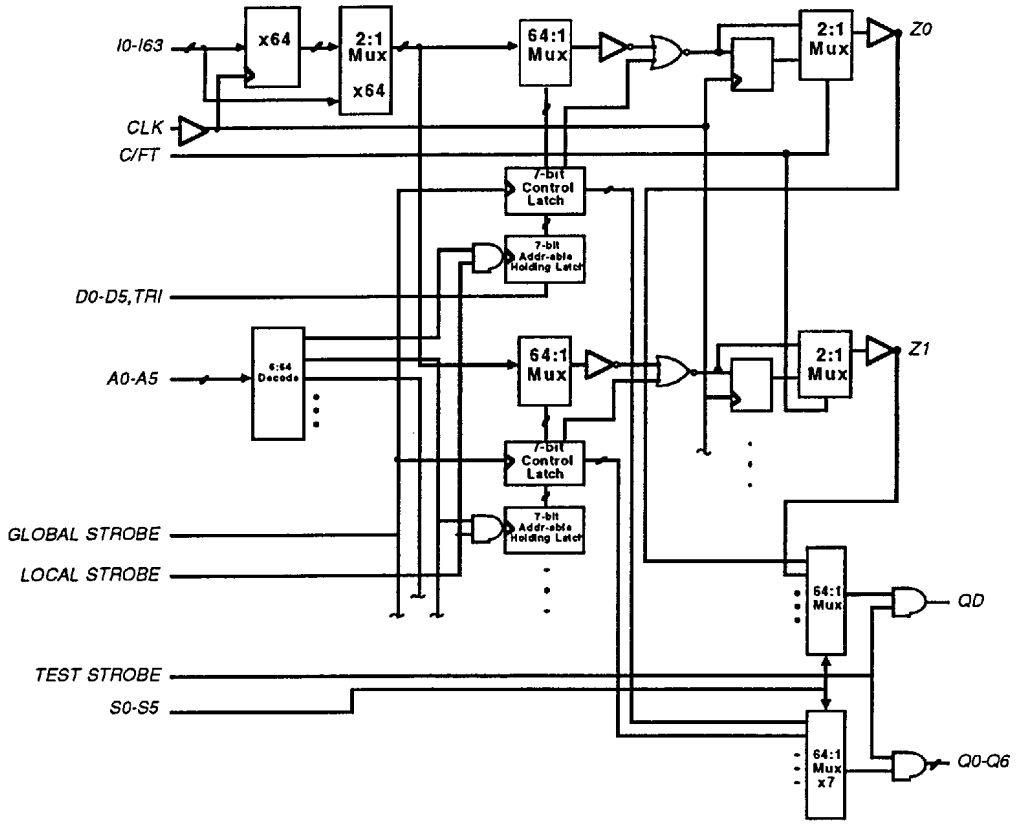
During normal operation, signals flow from inputs (I0 - I63) to output channels (Z0 - Z63) through sixty-four, 64:1 multiplexers. The traffic pattern is controllable by data previously stored in sixty-four 7-bit control registers with each register corresponding to an output channel. The first 6 least significant bits in each control register are reserved for designating the MUX input which will be connected to its corresponding output, the most significant bit is used to tri-state this output if desired. The 6 LSBs are a binary numerical representation of the input channel selected (i.e.., 000000 corresponds to I0, 000001 corresponds to I1, etc.).

The Write mode is used to alter any one or all signal paths. During Write mode, inputs A0 - A5 select which output channel's control register will be altered (also by a binary numerical representation). Inputs D0- D5 describe the new input signal to be selected for that channel. When a high pulse is applied to LOCAL STROBE, D0- D5 and the TRI bit is transferred into a holding latch. After some or all control registers are programmed, a high pulse is applied to GLOBAL STROBE to transfer the information from the holding latch into all the control registers. In this way the entire crosspoint switch can be reconfigured simultaneously.

The Read mode is a diagnostic feature used to examine the data stored in any one control register and its corresponding 64:1 multiplexer output. The control register to be examined is selected by inputs S0- S5 (by a binary numerical representation). When a high pulse is applied to the TEST STROBE, the contents of the selected control register will be displayed at the Q0- Q6 outputs and the corresponding 64:1 mux output will appear at the QD output. When TEST STROBE is "low" the Q bus has all low outputs (which is equivalent to being tri-stated).

The VSC864A-2 can be configured to run in either synchronous clocked mode or asynchronous flow-through mode. This feature is controlled by the C/FT input. When C/FT is high, the chip is in clocked mode and will require an input clock at its CK pin. In this mode all input and output data is registered. When C/FT is low the chip is in flow-through mode and will ignore the CK input. In clocked mode, the outputs on the monitor bus (Q0- Q6, and QD), and input data (I0 - I63) are registered by the master clock (CK).

Figure 1: Block Diagram



Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), VTT potential to GND ..... -3.0V to +0.5V
Input Voltage Applied, VE CLIN ..... -2.5V to +0.5V
Output Current, IOUT,(DC, output HI) ..... 100 mA
Case Temperature Under Bias, TC. ..... -55° to +125°C
Storage Temperature (ambient), TSTG. ..... -65°C to +150°C

Recommended Operating Conditions

ECL Supply Voltage, VTT. ..... -2.0V ± 0.1V
Commercial Operating Temperature Range, T(2). ..... 0° to 70°C
Industrial Operating Temperature Range, T(2). ..... -40° to 85°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extendedperiods may affect device reliability.

(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

AC Characteristics *(Over recommended operating conditions V_{CC} = V_{CCA} = GND Output load 25Ω to V_{TT}.)*

Table 1: Flow-Through Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
PW	Minimum data valid time	5	—	—	ns	≤ 20% Duty Cycle Distortion; 50% input
t_{DR}	Propagation delay (rising)	2800	—	5800	ps	—
t_{DF}	Propagation delay (falling)	2800	—	5800	ps	—
—	Duty cycle distortion	—	10	20	%	at 200 Mb/s(1)
skew	Output to output skew	—	—	2500	ps	On a given part broadcast mode
BER	Bit Error Rate	—	—	10^{-13}	—	Note (2)

(1) Duty cycle distortion = duty cycle out - duty cycle in / duty cycle in x 100%
(2) Based on limited measurement time, not device performance limitations

Table 2: Clocked Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
f_{MAX}	Maximum clock rate	—	—	200	MHz	—
t_{ISU}	Input data set-up time	50	—	—	ps	—
t_{IH}	Input data hold time	2000	—	—	ps	—
t_{CZR}	Clock to output delay (rising)	2000	—	3500	ps	—
t_{CZF}	Clock to output delay (falling)	2000	—	3500	ps	—
skew	Output to output skew	—	—	1500	ps	On a given part, broadcast mode

Table 3: Write Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{RECON}	Reconfiguration time	650	1300	—	ns	—
t_{ALSSU}	A but to LOCAL STROBE set-up time	300	—	—	ps	—
t_{ALSH}	a bus to LOCAL STROBE hold time	0	-	—	ps	—
t_{DLSSU}	D bus to LOCAL STROBE set-up time	400	—	—	ps	—
t_{DLSH}	D bus to LOCAL STROBE hold time	2	—	—	ns	—
t_{GLSU}	GLOBAL STROBE to LOCAL STROBE set-up time	5	—	—	ns	—
t_{GS},t_{LS}	GLOBAL STROBE and LOCAL STROBE pulse widths	5	—	—	ns	Recommended local strobe frequency = 50MHz
t_{LSL}	LOCAL STROBE low time	5	—	—	ns	—
t_{TS}	TEST STROBE pulse width	6.5	—	—	ns	—
t_{GLH}	GLOBAL STROBE to LOCAL STROBE hold time	0	—	—	ps	—

Parameters	Description	Min	Typ	Max	Units	Conditions
t_{GSZ}	GLOBAL STROBE to valid output (flow-through mode)	2.7	—	5.6	ns	—
t_{CGSU}	CLK to GLOBAL STROBE set-up time (clocked mode)	200	—	—	ps	Data being clocked in at this time is invalid
t_{GCL}	GLOBAL STROBE to CLK hold time (clocked mode)	3.5	—	—	ns	Data being clocked in at this time is invalid
t_{TSQ}	TEST STROBE to valid Q output	—	—	7.1	ns	—
t_{TSBQ}	S bus to valid output	—	—	7.1	ns	—
t_{TSQT}	TEST STROBE to tri-state condition on Q	—	—	6.5	ns	—

AC Timing Waveforms

Figure 2: Flow-through Mode

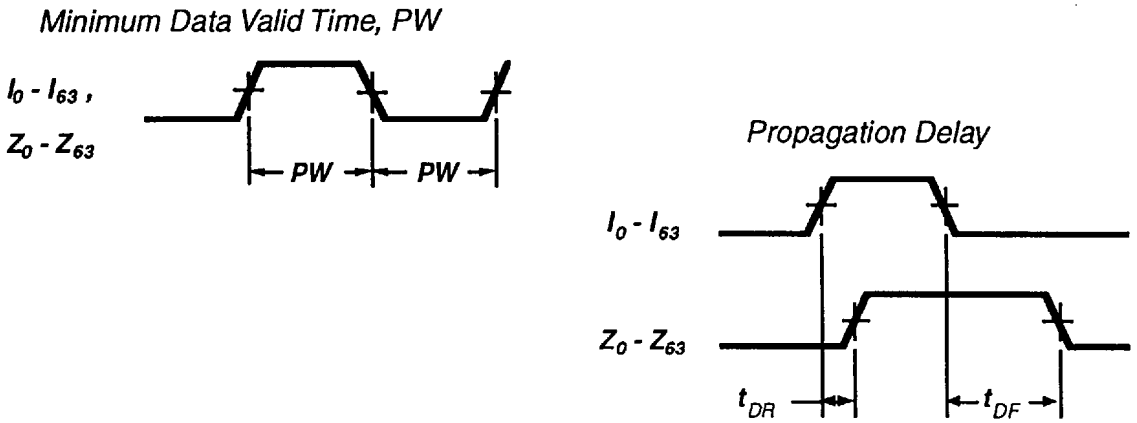


Figure 3: Clocked Mode

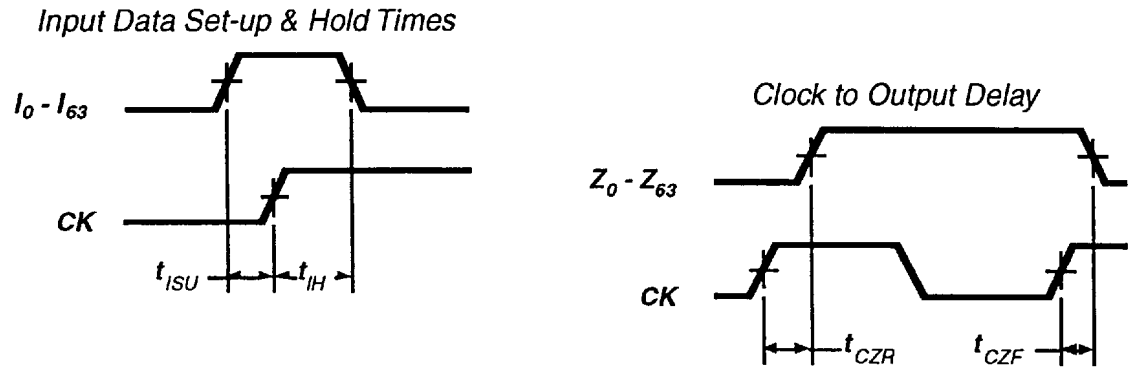
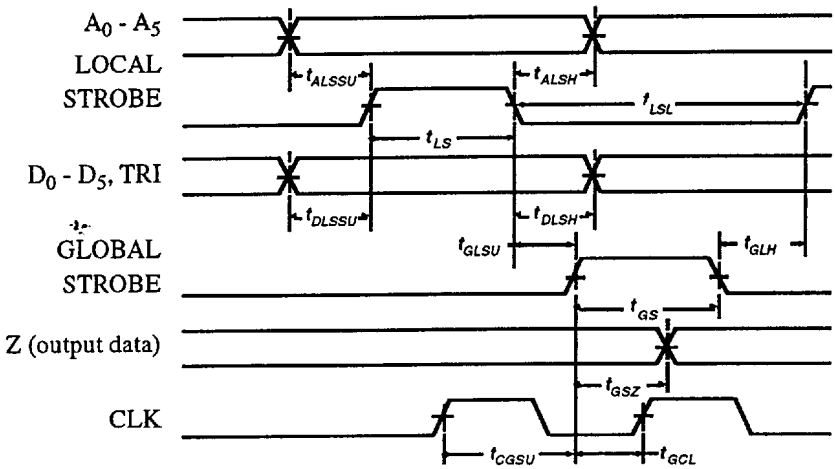


Figure 4: Write Mode



A address setup and hold relative to LOCAL STROBE.

D data setup and hold relative to LOCAL STROBE.

LOCAL STROBE to GLOBAL STROBE timing relationship.

CLOCKED MODE - GLOBAL STROBE to CLK timing relationship.

Figure 5: Read Mode

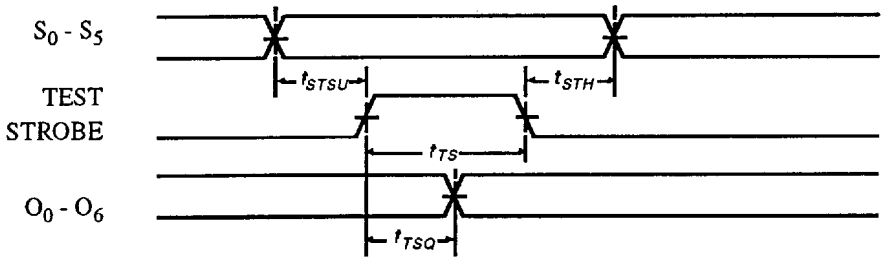


Figure 6: Block Diagram of Internal Write Mode Circuits

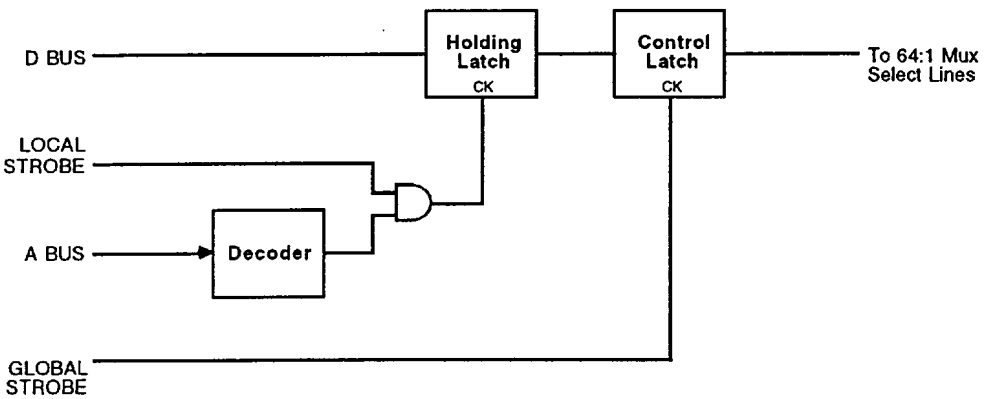


Table 4: Pin Description

Pin #	Name	I/O	Description
12-16, 20-30, 35-45, 49-53,184-188, 192- 202, 207-217, 221-225	I_0 - I_{63}	I	The 64 ECL signal inputs.
11	TRI	I	ECL input containing Tristate data to be loaded into a 64:1 Mux holding latch. (Tristate = HIGH) Combined with a control register's destination address. Used to tristate the corresponding output.
5-10	D_0 - D_5	I	ECL inputs containing the destination address to be loaded into the 64:1 Mux holding latch.
178-183	A_0 - A_5	I	ECL inputs containing the address of the 64:1 Mux holding/ control latch to be programmed.
177	LOCAL STROBE	I	Active HIGH, ECL input used to load the D0-D5 and TRI data into the 64:1 Mux holding latch.
34	GLOBAL STROBE	I	Active HIGH, ECL input used to load destination addresses to all 64:1 S Mux control latches simultaneously from the data contained in their corresponding holding latches.
54-59	S_0 - S_5	I	ECL inputs containing the address of the control latch to be observed at the QD output when the TEST STROBE is HIGH.
60	TEST STROBE	I	Active HIGH, ECL input used to enable Test Mode and observation of a selected 64:1 Mux control latch's destination address.
206	C/FT	I	ECL input used to enable Clocked or Flow-through Mode (Clocked = HIGH/Flow-Thru = LOW).
203	CK	I	ECL clock input for Clocked Mode.
68, 71, 73, 78, 80, 83, 85, 88, 92,95,97,100,102,107,109,112, 126, 129, 131, 136,138, 141,143, 148, 150, 153, 155,158, 162, 165, 167, 170, 240, 243, 245, 250, 252, 255, 257, 260, 264, 267, 269, 272, 274, 279, 281, 284, 298, 301, 303, 308, 310, 313, 315, 320, 322, 325, 327, 330, 334, 337, 339, 342	Z_0 - Z_{63}	O	The 64 ECL signal outputs.
296	QD	O	ECL output used to observe the output of a selected 64:1 Mux in Test Mode.
114,117,121,124,286,289,293	Q_0 - Q_6	O	ECL outputs containing the selected 64:1 Mux control register's destination address and TRI bit in Test Mode

Pin #	Name	I/O	Description
3, 17, 32, 47, 61, 76, 90, 104, 118,132, 146, 160, 175, 189, 204, 219, 233, 248, 262,276, 290, 304, 318, 332	VCC		ØV ground connection for internal logic.
2, 63, 69, 74, 81, 86, 93, 98, 103, 110, 115, 122, 127, 134, 139, 144, 151, 156, 163, 168, 174, 235, 241, 246, 253, 258, 265, 270, 275, 282, 287, 294, 299, 306, 311, 316, 323, 328, 335, 340	VCCA		ØV 'dirty' ground connection for outputs.
4, 18, 33, 48, 62, 77, 91, 105,119, 133, 147, 161, 176, 190,205, 220, 234, 249, 263, 277,305, 319, 333	VTT		-2V supply connection.
291	VSUB		-2V supply connection to substrate (most negative supply).
1, 19, 31, 46, 64-67, 70, 72, 75, 79, 82, 84, 87, 89, 94, 96, 99, 101, 106, 108, 111, 113, 116, 120, 123, 125, 128, 130, 135, 137, 140, 142, 145, 149, 152, 154, 157, 159, 164, 166, 169,171-173, 191, 218, 226-232, 236-239, 242, 244, 247, 251, 254, 256, 259, 261, 266, 268, 271, 273, 278, 280, 283, 285, 288, 292, 295, 297, 300, 302, 307, 309, 312, 314, 317, 321, 324, 326, 329, 331, 336, 338, 341, 343, 344	N/C		No Connection. These pins are not internally connected.

Table 5: Pin Identification

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
I_0	12	I_{22}	26	I_{44}	41	D_2	7	Z_6	85	Z_{28}	162	Z_{50}	303
I_1	225	I_{23}	211	I_{45}	196	D_3	8	Z_7	88	Z_{29}	165	Z_{51}	308
I_2	13	I_{24}	27	I_{43}	42	D_4	9	Z_8	92	Z_{30}	167	Z_{52}	310
I_3	224	I_{25}	210	I_{43}	195	D_5	10	Z_9	95	Z_{31}	170	Z_{53}	313
I_4	14	I_{26}	28	I_{43}	43	A_0	183	Z_{10}	97	Z_{32}	240	Z_{54}	315
I_5	223	I_{27}	209	I_{43}	194	A_1	182	Z_{11}	100	Z_{33}	243	Z_{55}	320
I_6	15	I_{28}	29	I_{43}	44	A_2	181	Z_{12}	102	Z_{34}	245	Z_{56}	322
I_7	222	I_{29}	208	I_{43}	193	A_3	180	Z_{13}	107	Z_{35}	250	Z_{57}	325
I_8	16	I_{30}	30	I_{43}	45	A_4	179	Z_{14}	109	Z_{36}	252	Z_{58}	327
I_9	221	I_{31}	207	I_{43}	192	A_5	178	Z_{15}	112	Z_{37}	255	Z_{59}	330
I_{10}	20	I_{32}	35	I_{43}	49	S_0	54	Z_{16}	126	Z_{38}	257	Z_{601}	334
I_{11}	217	I_{33}	202	I_{43}	188	S_1	55	Z_{17}	129	Z_{39}	260	Z_{61}	337
I_{12}	21	I_{34}	36	I_{43}	50	S_2	56	Z_{18}	131	Z_{40}	264	Z_{62}	339
I_{13}	216	I_{35}	201	I_{43}	187	S_3	57	Z_{19}	136	Z_{41}	267	Z_{63}	342
I_{14}	22	I_{36}	37	I_{43}	51	S_4	58	Z_{20}	138	Z_{42}	269	Q_0	114
I_{15}	215	I_{37}	200	I_{43}	186	S_5	59	Z_{21}	141	Z_{43}	272	Q_1	117
I_{16}	23	I_{38}	38	I_{43}	52	Z_0	68	Z_{22}	143	Z_{44}	274	Q_2	121
I_{17}	214	I_{39}	199	I_{43}	185	Z_1	71	Z_{23}	148	Z_{45}	279	Q_3	124
I_{18}	24	I_{40}	39	I_{43}	53	Z_2	73	Z_{24}	150	Z_{46}	281	Q_4	286
I_{19}	213	I_{41}	198	I_{43}	184	Z_3	78	Z_{25}	153	Z_{47}	284	Q_5	289
I_{20}	25	I_{42}	40	D_0	5	Z_4	80	Z_{26}	155	Z_{48}	298	Q_6	293
I_{21}	212	I_{43}	197	D_1	6	Z_5	83	Z_{27}	158	Z_{49}	301		

Package Information

Figure 7: 344 Pin Ceramic LDCC Package

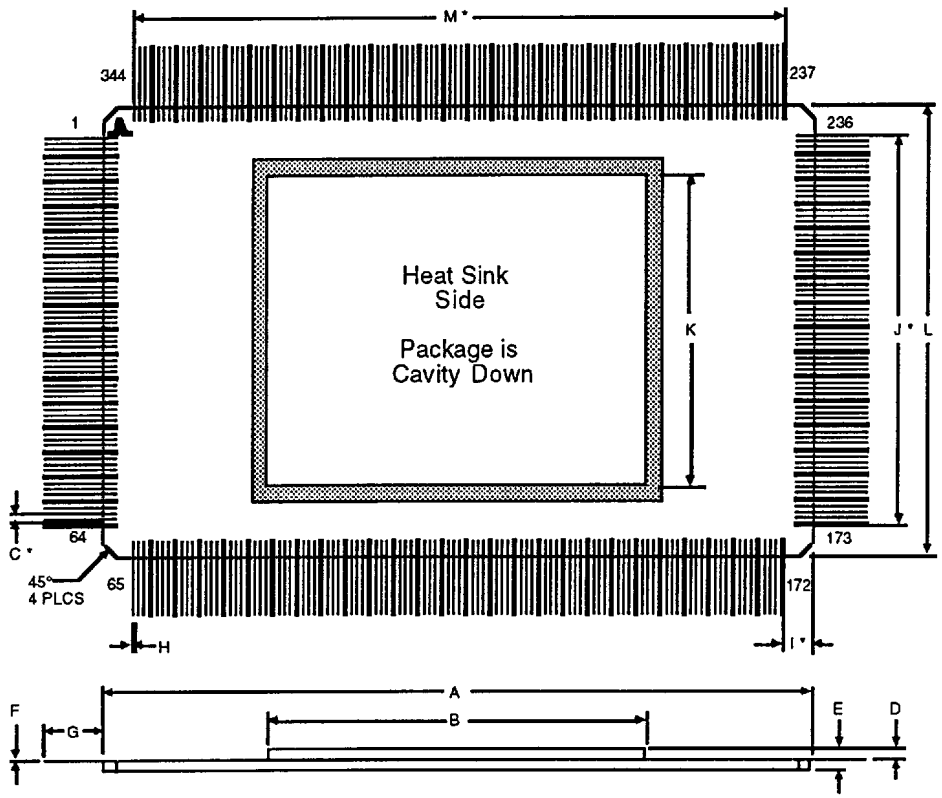


Table 6: 344 Pin Ceramic LDCC Tolerance Table

Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	58.93/59.94	2.320/2.340	H	0.15/0.25	0.006/0.010
B	34.54 TYP	1.36 TYP	I*	REF 2.54 TYP	REF 0.100 TYP
C*	0.51 TYP	0.020 TYP	J*	32.00 TYP	1.26 TYP
D	0.38/0.63	0.015/0.025	K	39.46 TYP	1.08 TYP
E	2.16/2.92	0.085/0.115	L	36.57/37.59	1.440/1.480
F	0.09/0.216	0.0004/0.008	M*	54.36 TYP	2.140 TYP
G	5.08/7.62	0.200/0.300	—	—	—

**At package body*

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

Expandability

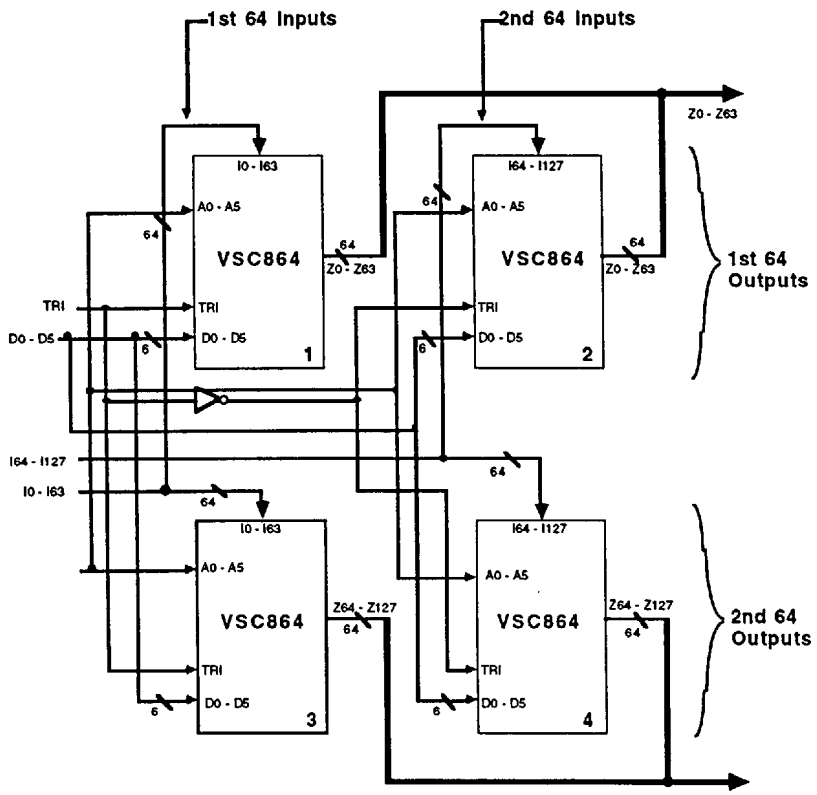
The VSC864A-2 can be expanded to larger crosspoint switches by configuring it so that any input can be multiplexed to any output. The figure below is an example of a 128 x 128 crosspoint switch. The top two VSC864A-2s (1&2) correspond to the first 64 outputs and the bottom two VSC864A-2s (3&4) correspond to the last 64 outputs. The VSC864A-2s on the left (1&3) correspond to the first 64 inputs, and the two VSC864A-2s on the right (2&4) correspond to the last inputs. All like outputs are then joined to form a 128 bit Z output bus. The ability of the VSC864A-2 to tri-state its outputs will prevent contention on the Z bus.

The TRI input is configured such that when it is active on the left hand chips (which are responsible for routing the first 64 inputs) it is inactive on the two right hand chips (which are responsible for routing the last 64 inputs). The TRI input thus functions as the MSB of a 7-bit channel address word (A-bus plus TRI). Chips can share A-bus information. The destination (D) bus can be shared among the four chips with the local strobe for each device being used to select which output address gets reconfigured.

The layout and placement of the VSC864A-2 is such that inputs are on the top and bottom of the chip and outputs are to the right and left. In this way a PC board design for a large crosspoint is facilitated.

In the read mode tri-stateability on the Q-bus can be controlled with the TEST STROBE input. A "low" level on this input will tri-state its corresponding Q-bus. In this way the Q-bus from all chips can be wire-OR'ed. Individual TEST STROBE signals to each chip, however, are required.

Figure 8: 128 X 128 Crosspoint Switch Diagram



200 Mb/s 64 x 64
Crosspoint Switch

Data Sheet

VSC864A-2

Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC864A-2xx

Device Type:

VSC864A-2: 64X64 Crosspoint Switch

Package Type

F: 344-pin Leaded Chip Carrier (LDCC)

Notice

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