M8289
BUS ARBITER

Military

- **Provides Multi-Master System Bus Protocol**
- **Synchronizes M8086, M8088, M8089, and M80186**
- **Provides Simple Interface with M8288 Bus Controller**
- **Military Temperature Range: −55°C to +125°C (T_C)**
- **Four Operating Modes for Flexible System Configuration**
- **Single +5V ±10% Power Supply**
- **Provides System Bus Arbitration for M8089 IOP in Remote Mode**

The Intel M8289 Bus Arbiter is a 5-volt-only bipolar component for use with medium to large M8086, M8088, M8089 and M80186 multimaster/multiprocessing systems. The M8289 provides system bus arbitration for systems with multiple bus masters, such as an M8086 CPU with capability. For new designs, see the M82289 Bus Arbiter data sheet.

NOTE:
Not for new designs.

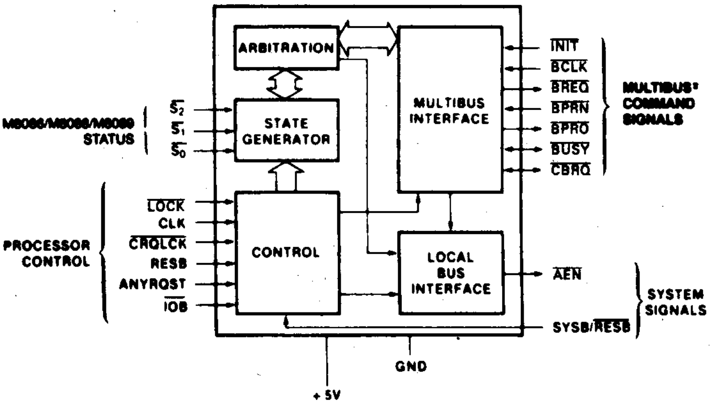

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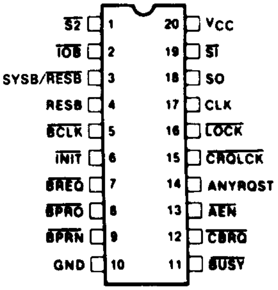
Figure 1. Block Diagram



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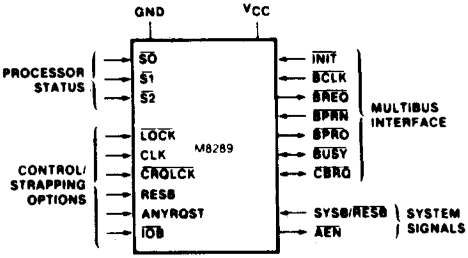

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Figure 2. Functional Pinout

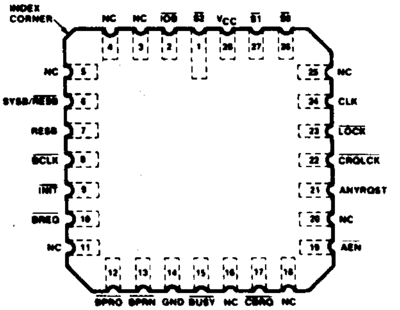

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Figure 3. M8289 Pin Diagram

December 1989
Order Number: 271027-004

Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**POWER:** +5V supply ±10%.
GND		**GROUND.**
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	I	**STATUS INPUT PINS:** The status input pins from an M8086, M8088, M8089 or M80186 processor. The M8289 decodes these pins to initiate bus request and surrender actions. (See Table 2)
CLK	I	**CLOCK:** From the M8284A clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	I	**LOCK:** A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	I	**COMMON REQUEST LOCK:** An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	I	**RESIDENT BUS:** A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. Strapped low, the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	I	**ANY REQUEST:** A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table 2. If ANYRQST is strapped high and $\overline{CBRQ}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{CBRQ}$ low and ANYRQST high forces the M8289 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs BREQ is driven false (high).
$\overline{IOB}$	I	**IO BUS:** A strapping option which configures the M8289 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{AEN}$	O	**ADDRESS ENABLE:** The output of the M8289 Arbiter to the processor's address latches, to the M8288 Bus Controller and M8284A Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to tri-state their output drivers.
SYSB/$\overline{RESB}$	I	**SYSTEM BUS/RESIDENT BUS:** An input signal when the arbiter is configured in the S.R. Mode (RESB is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from $\phi1$ of T4 to $\phi1$ of T2 of the processor cycle. During the period from $\phi2$ of T1 to $\phi1$ of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the S.R. Mode when the state of the SYSB/$\overline{RESB}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{CBRQ}$	I/O	**COMMON BUS REQUEST:** An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{CBRQ}$ pins (open-collector output) of all the M8289 Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{CBRQ}$ line low. Any other arbiter connected to the $\overline{CBRQ}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{BREQ}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{CBRQ}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{INIT}$	I	**INITIALIZE:** An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
BCLK	I	**BUS CLOCK:** The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
BREQ	O	**BUS REQUEST:** An active low output signal in the parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
BPRN	I	**BUS PRIORITY IN:** The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of BCLK. BPRN indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of BPRN instructs the arbiter that it has lost priority to a higher priority arbiter.
BPRO	O	**BUS PRIORITY OUT:** An active low output signal used in the serial priority resolving scheme where BPRO is daisy-chained to BPRN of the next lower priority arbiter.
BUSY	I/O	**BUSY:** An active low open collector multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by BPRN) seizes the bus and pulls BUSY low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the BUSY signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

FUNCTIONAL DESCRIPTION

The M8289 Bus Arbiter operates in conjunction with the M8288 Bus Controller to interface M8086, M8088 processors to a multi-master system bus (both the M8086 and M8088 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (M8288), the data transceivers and the address latches from accessing the system bus (e.g., all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the M8288, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration Between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the halt state. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multi-master system bus is surrendered or requested under different sets of conditions.

Priority Resolving Techniques

Since there can be many bus masters on a multi-master system bus, some means of resolving priority between bus masters simultaneously requesting the bus must be provided. The M8289 Bus Arbiter provides several resolving techniques. All the techniques are based on a priority concept that at a given time one bus master will have priority above all the rest. There are provisions for using parallel priority resolving techniques, serial priority resolving techniques, and rotating priority techniques.

Parallel Priority Resolving

The parallel priority resolving technique uses a separate bus request line (BREQ) for each arbiter on the multi-master system bus; see Figure 4. Each BREQ line enters into a priority encoder which generates the binary address of the highest priority BREQ line which is active. The binary address is decoded by a decoder to select the corresponding BPRN (Bus Priority In) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority (BPRN true) then allows its associated bus master onto the multi-master system bus as soon as it becomes available (i.e., the bus is no longer busy). When one bus arbiter gains priority over another arbiter it cannot immediately seize the bus, it must wait until the present bus transaction is complete.

Upon completing its transaction, the present bus occupant recognizes that it no longer has priority and surrenders the bus by releasing $\overline{\text{BUSY}}$. $\overline{\text{BUSY}}$ is an active low "OR" tied signal line which goes to every bus arbiter on the system bus. When $\overline{\text{BUSY}}$ goes inactive (high), the arbiter which presently has bus priority ($\overline{\text{BPRN}}$ true) then seizes the bus and pulls $\overline{\text{BUSY}}$ low to keep other arbiters off the bus. See waveform timing diagram, Figure 5. Note that all multi-master system bus transactions are synchronized to the bus clock (BCLK). This allows the parallel priority resolving circuitry or any other priority resolving scheme employed to settle.

SERIAL PRIORITY RESOLVING

The serial priority resolving technique eliminates the need for the priority encoder-decoder arrangement by daisy-chaining the bus arbiters together, connecting the higher priority bus arbiters's $\overline{\text{BPRO}}$ (Bus Priority Out) output to the $\overline{\text{BPRN}}$ of the next lower priority. See Figure 6.

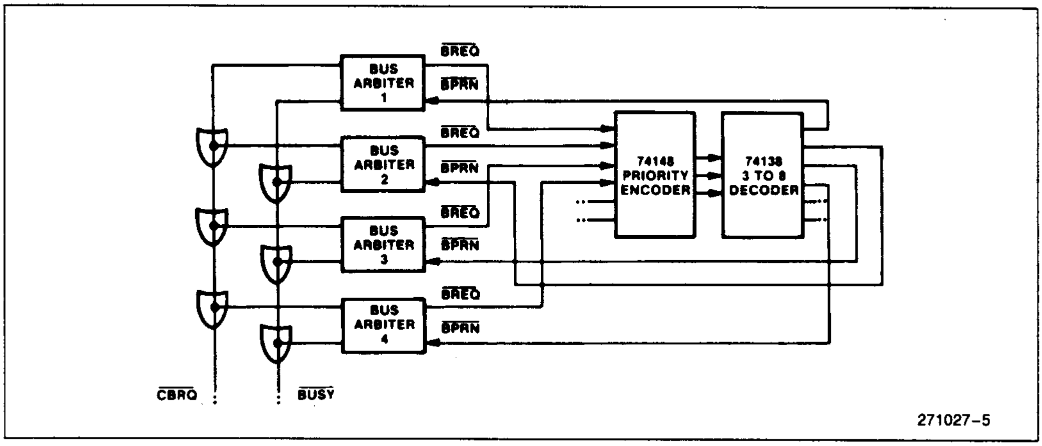
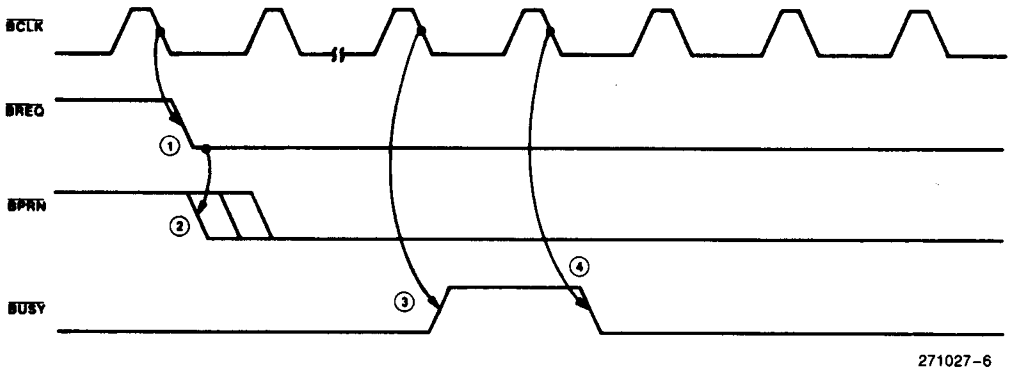


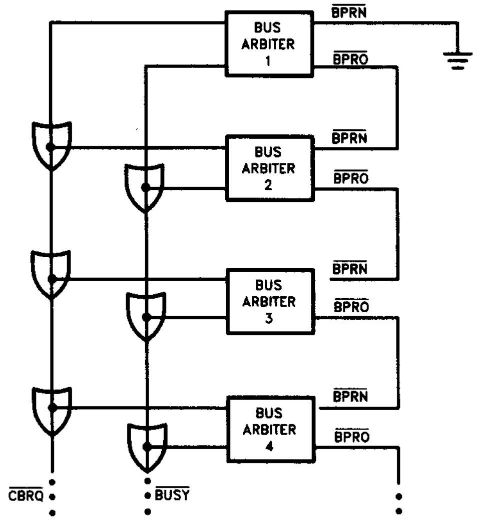
Figure 4. Parallel Priority Resolving Technique



NOTES:

1. Higher priority bus arbiter requests the multi-master system bus.
2. Attains priority.
3. Lower priority bus arbiter releases busy.
4. Higher priority bus arbiter then acquires the bus and pulls busy down.

Figure 5. Higher Priority Arbiter Obtaining the Bus from a Lower Priority Arbiter



The number of arbiters that may be daisy-chained together in the serial priority resolving scheme is a function of BCLK and the propagation delay from arbiter to arbiters. Normally, at 10 MHz only 3 arbiters may be daisy-chained.

Figure 6. Serial Priority Resolving

ROTATING PRIORITY RESOLVING

The rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuit which rotates priority between requesting arbiters thus allowing each arbiter an equal chance to use the multi-master system bus, over time.

Which Priority Resolving Technique to Use

There are advantages and disadvantages for each of the techniques described above. The rotating priority resolving technique requires substantial external logic to implement while the serial technique uses no external logic but can accommodate only a limited number of bus arbiters before the daisy-chain propagation delay exceeds the multi-master's system bus clock ($\overline{\text{BCLK}}$). The parallel priority resolving technique is in general a good compromise between the other two techniques. It allows for many arbiters to be present on the bus while not requiring too much logic to implement.

***NOTE:**
In some system configurations it is possible for a non-I/O Processor to have access to more than one Multi-Master System Bus.

M8289 MODES OF OPERATION

There are two types of processors in the M8086 family. An Input/Output processor (the M8089 IOP) and the M8086, M8088 CPUs. Consequently, there are two basic operating modes in the M8289 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{\text{IOB}}$ strapping option configures the M8289 Bus Arbiter into the $\overline{\text{IOB}}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only (Figure 7). With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{\text{IOB}}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus.

The M8086 and M8088 processors can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration. In such a system configuration the processor would have access to memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{\text{RESB}}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{\text{RESB}}$ also enables or disables commands from one of the bus controllers.

A summary of the modes that the M8289 has, along with its response to its status lines inputs, is summarized in Table 2.

Table 2. Summary of M8289 Modes, Requesting and Relinquishing the Multi-Master System Bus

	Status Lines From M8086 or M8088 or M8089			IOB Mode Only	RESB (Mode Only) IOB = High RESB = High		IOB Mode RESB Mode IOB = Low RESB = High		Single Bus Mode IOB = High RESB = Low
	$\overline{\text{S2}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$	$\overline{\text{IOB}}$ = Low	SYSB/RESB = High	SYSB/$\overline{\text{RESB}}$ = Low	SYSB/$\overline{\text{RESB}}$ = High	SYSB/$\overline{\text{RESB}}$ = Low	
I/O Commands	0	0	0	X	✓	X	X	X	✓
	0	0	1	X	✓	X	X	X	✓
	0	1	0	X	✓	X	X	X	✓
HALT	0	1	1	X	X	X	X	X	X
MEM Commands	1	0	0	✓	✓	X	✓	X	✓
	1	0	1	✓	✓	X	✓	X	✓
	1	1	0	✓	✓	X	✓	X	✓
IDLE	1	1	1	X	X	X	X	X	X

NOTES:
1. X = Multi-Master System Bus is allowed to be surrendered.
2. ✓ = Multi-Master System Bus is requested.

Mode	Pin Strapping	Multi-Master System Bus	
		Requested**	Surrendered*
Single Bus Multi-Master Mode	$\overline{\text{IOB}}$ = High RESB = Low	Whenever the Processor's Status Lines Go Active	HLT + TI • CBRQ + HPBRQ†
RESB Mode Only	$\overline{\text{IOB}}$ = High RESB = High	SYSB/$\overline{\text{RESB}}$ = High • ACTIVE STATUS	(SYSB/$\overline{\text{RESB}}$ = Low + TI) • CBRQ + HLT + HPBRQ
IOB Mode Only	$\overline{\text{IOB}}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • CBRQ + HLT + HPBRQ
IOB Mode • RESB Mode	$\overline{\text{IOB}}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{\text{RESB}}$ = High)	[(I/O Status Commands) + SYSB/$\overline{\text{RESB}}$ = LOW] • CBRQ + HPBRQ† + HLT

NOTES:

*$\overline{\text{LOCK}}$ prevents surrender of Bus to any other arbiter. $\overline{\text{CRQLCK}}$ prevents surrender of Bus to any lower priority arbiter.

**Except for HALT and Passive or IDLE Status.

†HPBRQ. Higher priority Bus request or $\overline{\text{BPRN}}$ = 1.

1. $\overline{\text{IOB}}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and • as "AND".
4. TI = Processor Idle Status $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ = 111.
5. HLT = Processor Halt Status $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ = 011.

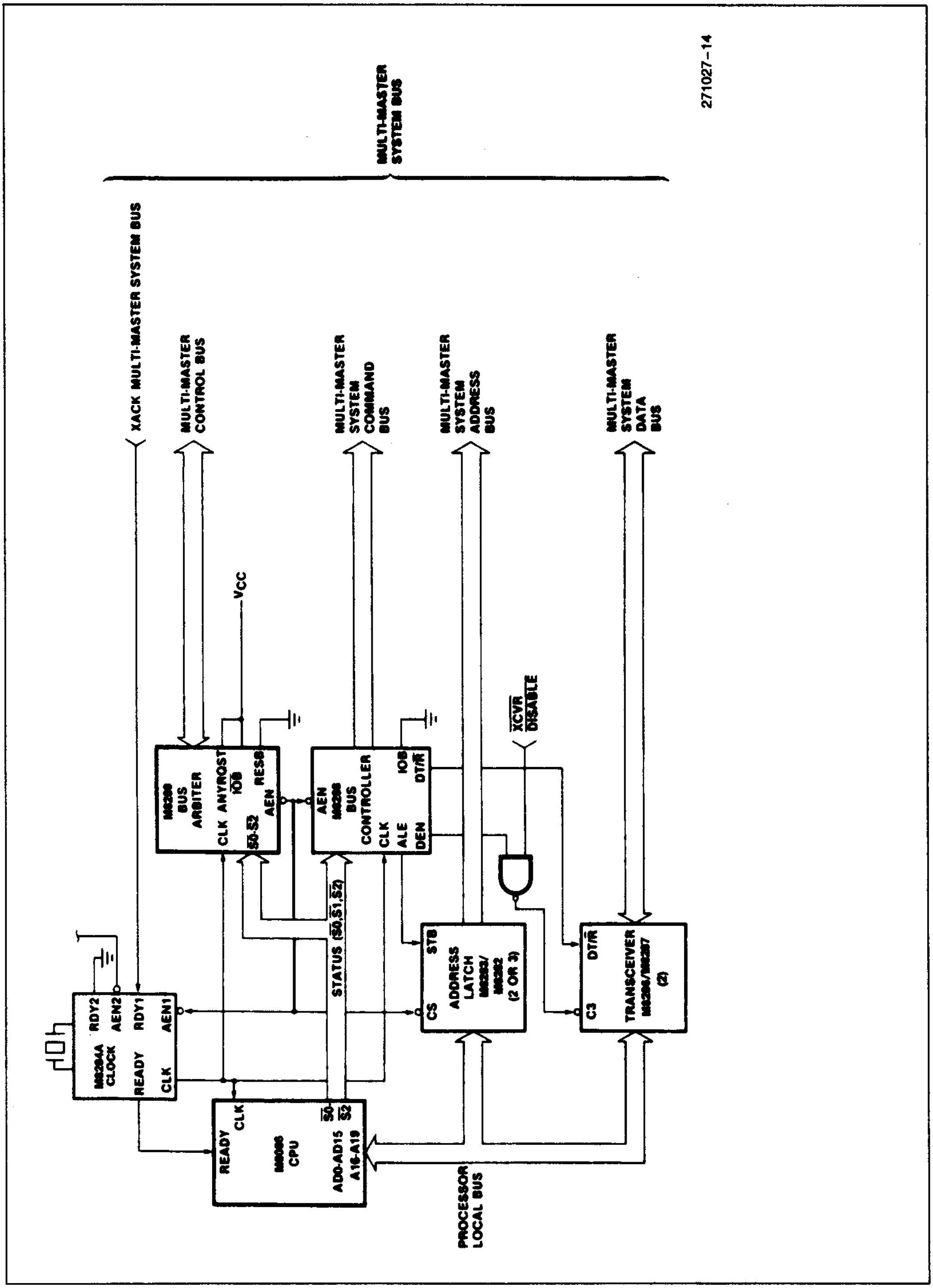


Figure 7. Typical Medium Complexity CPU System

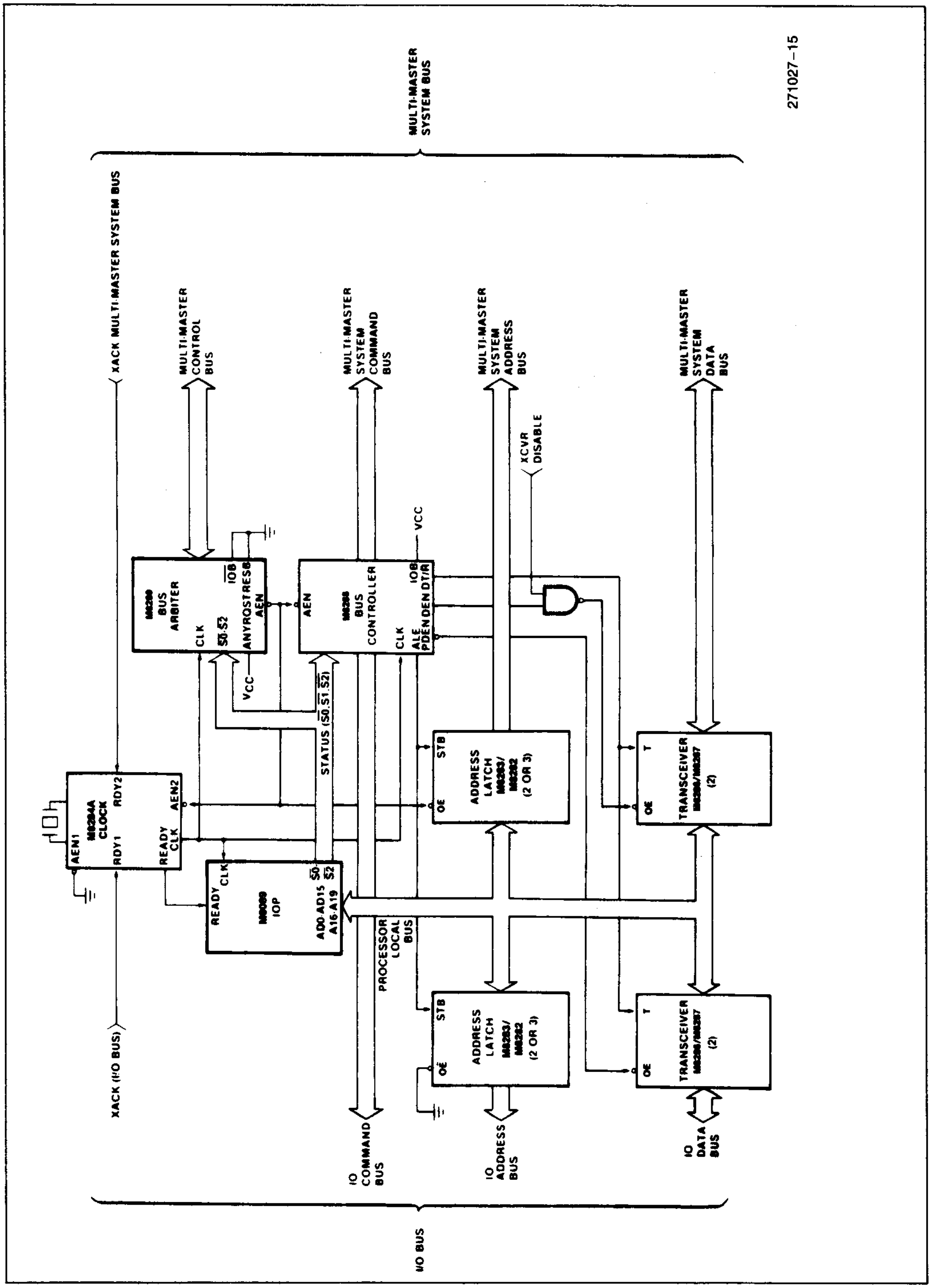


Figure 8. Typical Medium Complexity IOB System

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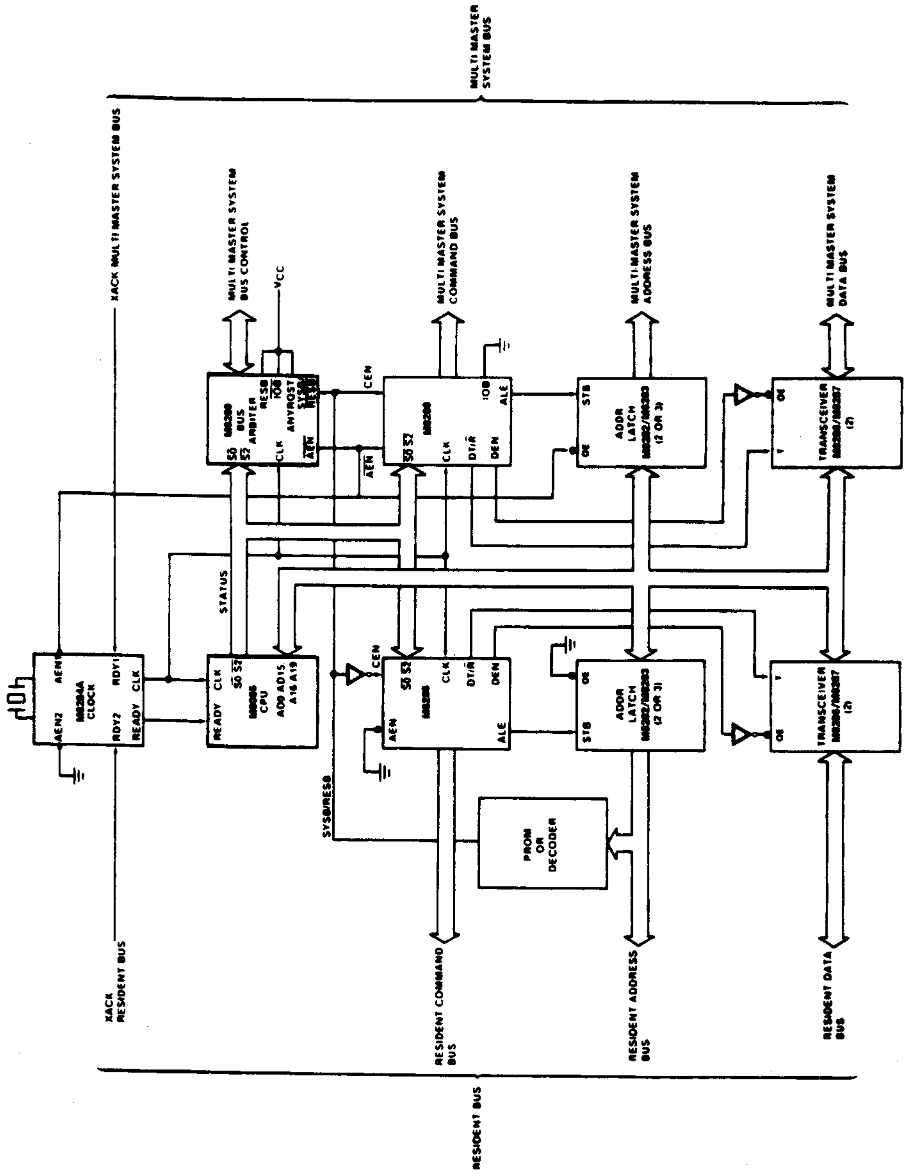


*By adding another M8289 arbiter and connecting its $\overline{\text{AEN}}$ to the M8288 whose $\overline{\text{AEN}}$ is presently grounded, the processor could have access to two multi-master buses.

Figure 9. M8289 Bus Arbiter Shown in System-Resident Bus Configuration

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias(1). −55°C to +125°C
Storage Temperature .... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages................ −1.0V to +5.5V
Power Dissipation.......................... 1.5W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Comments
V_C	Input Clamp Voltage		−1.0	V	$V_{CC} = 4.50V$, $I_C = -5$ mA
I_F	Input Forward Current		−0.5	mA	$V_{CC} = 5.50V$, $V_F = 0.45V$
I_R	Reverse Input Leakage Current		60	µA	$V_{CC} = 5.50$, $V_R = 5.50$
V_{OL}	Output Low Voltage				
	$\overline{\text{BUSY}}$, $\overline{\text{CBRQ}}$		0.50	V	$I_{OL} = 18$ mA
	$\overline{\text{AEN}}$		0.50	V	$I_{OL} = 14$ mA
	$\overline{\text{BPRO}}$, $\overline{\text{BREQ}}$		0.50	V	$I_{OL} = 9$ mA
V_{OH}	Output High Voltage $\overline{\text{BUSY}}$, $\overline{\text{CBRQ}}$	Open Collector			
	All Other Outputs	2.4		V	$I_{OH} = -350$ µA
I_{CC}	Power Supply Current		165	mA	
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
Cin Status	Input Capacitance		25	pF	
Cin (Others)	Input Capacitance		12	pF	

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Unit	Comments
TCLCL	CLK Cycle Period	125		ns	
TCLCH	CLK Low Time	65		ns	
TCHCL	CLK High Time	35		ns	
TSVCH	Status Active Setup	65	TCLCL−10	ns	
TSHCL	Status Inactive Setup	50	TCLCL−10	ns	
THVCH	Status Active Hold	10		ns	

A.C. CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

TIMING REQUIREMENTS (Continued)

Symbol	Parameter	Min	Max	Unit	Comments
THVCL	Status Inactive Hold	10		ns	
TBYSBL	$\overline{\text{BUSY}}$ ↑ ↓ Setup to $\overline{\text{BCLK}}$ ↓	20		ns	
TCBSBL	$\overline{\text{CBRQ}}$ ↑ ↓ Setup to $\overline{\text{BCLK}}$ ↓	20		ns	
TBLBL	$\overline{\text{BCLK}}$ Cycle Time	100		ns	
TBHCL	$\overline{\text{BCLK}}$ High Time	30	0.65 [TBLBL]	ns	
TCLLL1	$\overline{\text{LOCK}}$ Inactive Hold	20		ns	
TCLLL2	$\overline{\text{LOCK}}$ Active Setup	40		ns	
TPNBL	$\overline{\text{BPRN}}$ ↑ ↓ to $\overline{\text{BCLK}}$ ↓ Setup Time	15		ns	
TCLSR1	SYSB/$\overline{\text{RESB}}$ Setup	0		ns	
TCLSR2	SYSB/$\overline{\text{RESB}}$ Hold	20		ns	
TIVIH	Initialization Pulse Width	3 TBLBL + 3 TCLCL		ns	
TILIH	Input Rise Time		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time		12	ns	From 2.0V to 0.8V

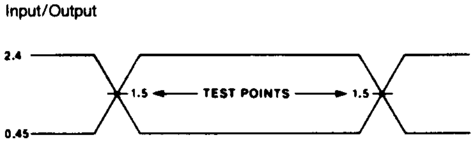
TIMING RESPONSES

Symbol	Parameter	Min	Max	Unit	Comments
TBLBRL	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ Delay ↑ ↓		35	ns	
TBLPOH	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ ↑ ↓ (Note 1)		40	ns	
TPNPO	$\overline{\text{BPRN}}$ ↑ ↓ to $\overline{\text{BPRO}}$ ↑ ↓ Delay (Note 1)		25	ns	
TBLBYL	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Low		60	ns	
TBLBYH	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Float (Note 2)		35	ns	
TCLAEH	CLK to $\overline{\text{AEN}}$ High		65	ns	
TBLAEL	$\overline{\text{BCLK}}$ to $\overline{\text{AEN}}$ Low		40	ns	
TBLCBL	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ Low		60	ns	
TBLCBH	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ Float (Note 2)		35	ns	
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12	ns	From 2.0V to 0.8V

↑ ↓ Denotes that spec applies to both transitions of the signal.

NOTES:
1. BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRN.
2. Measured at 0.5V above GND.

A.C. TESTING INPUT, OUTPUT WAVEFORM



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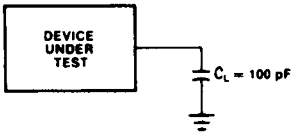
A.C. Testing: Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". The Clock is Driven at 4.3V and 0.25V. Timing Measurements are Made at 1.5V for Both a Logic "1" and "0".

A.C. TESTING LOAD CIRCUIT



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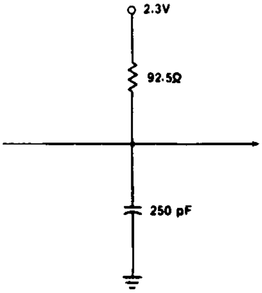
$C_L = 100$ pF
C_L Includes Jig Capacitance

A.C. TEST CIRCUITS

1) $\overline{\text{BUSY}}$, $\overline{\text{CBRQ}}$



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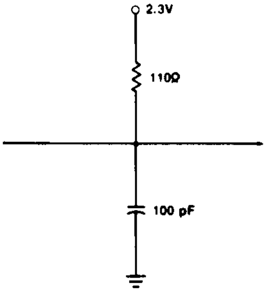
2) $\overline{\text{AEN}}$



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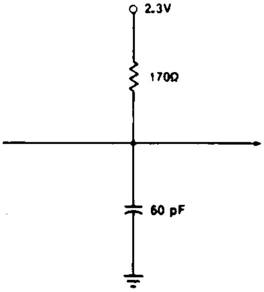
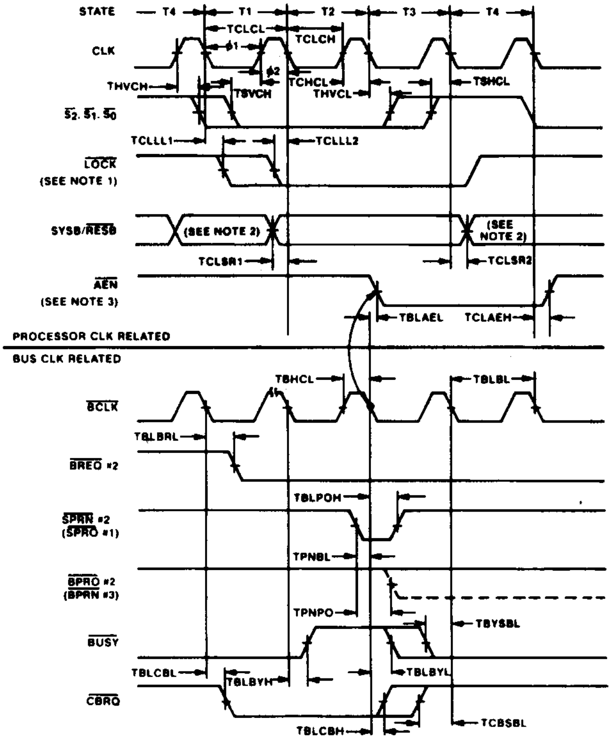
3) $\overline{\text{BPRO}}$, $\overline{\text{BREQ}}$



271027-11

WAVEFORMS



271027-12

NOTES:

1. $\overline{\text{LOCK}}$ active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained $\overline{\text{LOCK}}$ inactive has no critical time and can be asynchronous. -$\overline{\text{CRQLCK}}$ has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/$\overline{\text{RESB}}$ is permitted during this time. After φ2 of T1 and before φ1 of T4, SYSB/$\overline{\text{RESB}}$ should be stable to maintain system efficiency.
3. $\overline{\text{AEN}}$ leading edge is related to $\overline{\text{BCLK}}$, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

ADDITIONAL NOTES:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to $\overline{\text{BCLK}}$. The signals shown related to the $\overline{\text{BCLK}}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme (see footnote on page 5). Assume arbiter #1 has the bus and is holding busy low. Arbiter #2 detects its processor wants the bus and pulls low BREQ #2. If BPRN #2 is high (as shown), arbiter #2 will pull low $\overline{\text{CBRQ}}$ line. $\overline{\text{CBRQ}}$ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{\text{CBRQ}}$].** Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its $\overline{\text{BPRO}}$ #1 (tied to $\overline{\text{BPRN}}$ #2) and releasing BUSY. Arbiter #2 now sees that it has priority from $\overline{\text{BPRN}}$ #2 being low and releases $\overline{\text{CBRQ}}$. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{\text{BPRO}}$ #2 [TPNPO].

**Note that even a higher priority arbiter which is acquiring the bus through $\overline{\text{BPRN}}$ will momentarily drop $\overline{\text{CBRQ}}$ until it has acquired the bus.