Semiconductor Corporation

CSZ5116

16-Bit, 50kHz Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 3-State Output Buffers
  - Microprocessor Interface
- Sampling Rates up to 50kHz
- Ultra-Low Distortion
  - Total Harmonic Distortion: 0.001%
  - Peak Harmonic or Noise: −104dB
- Low Power Dissipation: 120mW
- Pin Compatible with CSZ5112/CSZ5114

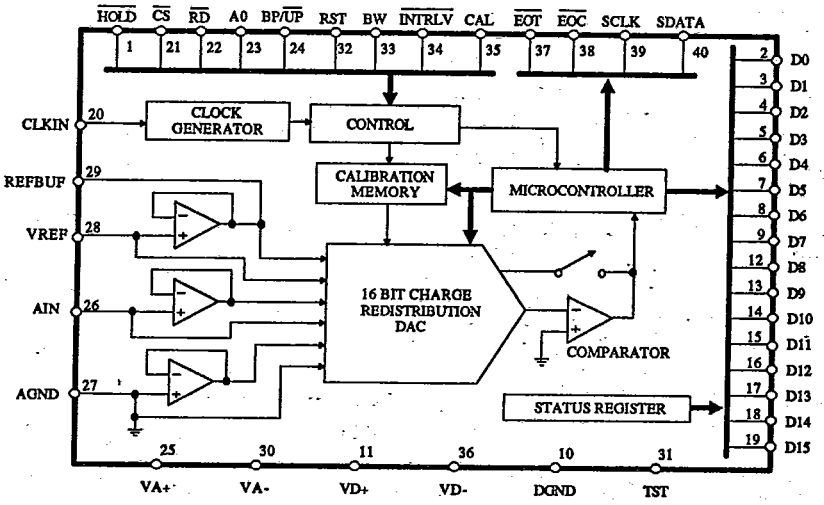
General Description

The CSZ5116 CMOS analog-to-digital converter is an ideal front-end for single- or multi-channel digital signal processing systems. It needs no external sample/hold amplifier at its input to convert ac signals - the sampling function is inherent to its charge redistribution design.

Using a standard successive-approximation algorithm, the CSZ5116 sequences through a 16-bit conversion in 16.25 microseconds. With 3.75 microseconds needed between conversions for acquisition, the CSZ5116 can support throughput rates up to 50kHz. It is therefore ideal for processing audioband signals.

The CSZ5116 features an on-chip self-calibration scheme which calibrates its bit weights to true 16-bit accuracy. This insures low distortion and maintains good signal-to-noise performance with low-level signals.

ORDERING INFORMATION: Page 89



S-to-Z™ Converter

Crystal Semiconductor Corporation
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ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V;
Full-Scale Input Sinewave, 1kHz; f_{clk} = 4MHz for -16, 2MHz for -32; f_s = 50kHz for -16, 25kHz for -32;
Bipolar Mode ; Analog Source Impedance = 200Ω unless otherwise specified)

Parameter*		CSZ5116-J,K,L min	typ	max	CSZ5116-A,B,C min	typ	max	CSZ5116-S,T,U min	typ	max	Units
Specified Temperature Range		0 to 70			-40 to 85			-55 to 125			°C
Dynamic Performance											
Peak Harmonic or Spurious Noise											
	-J,A,S	92	94		92	94		92	94		dB
1kHz Input	-K,B,T	96	100		96	100		96	100		dB
T_{min} to T_{max}	-L,C,U	100	104		100	104		100	104		dB
(Note 1)	-J,A,S	82	84		82	84		82	84		dB
12kHz Input	-K,B,T	85	88		85	88		85	88		dB
	-L,C,U	85	91		85	91		85	91		dB
Total Harmonic Distortion											
	-J,A,S		0.004			0.004			0.004		%
	-K,B,T		0.002			0.002			0.002		%
	-L,C,U		0.001			0.001			0.001		%
Signal-to-Noise Ratio											
	-J,A,S	84	87		84	87		84	87		dB
0dB Input	-K,B,T	87	90		87	90		87	90		dB
T_{min} to T_{max}	-L,C,U	90	92		90	92		90	92		dB
	-J,A,S		27			27			27		dB
-60dB Input	-K,B,T		30			30			30		dB
(Note 2)	-L,C,U		32			32			32		dB
dc Accuracy											
Differential Linearity	(Note 3)	16			16			16			Bits
Full Scale Error	T_{min} to T_{max}		±2			±2			±2		LSB
Unipolar Offset	T_{min} to T_{max}		±1			±1			±1		LSB
Bipolar Offset	T_{min} to T_{max}		±1			±1			±1		LSB
Bipolar Zero Error	T_{min} to T_{max}		±2			±2			±2		LSB

Notes: 1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest.
2. A detailed plot of S/(N+D) vs. input amplitude appears on page 79.
3. Minimum resolution for which no missing codes is guaranteed.

*Refer to *Error Definitions* on page 88.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter		CSZ5116-J,K,L min	typ	max	CSZ5116-A,B,C min	typ	max	CSZ5116-S,T,U min	typ	max	Units
Analog Input											
Aperture Time			25			25			25		ns
Aperture Jitter			100			100			100		ps
Full Power Bandwidth	(Note 4)		25			25			25		kHz
Input Capacitance (Note 5)	Unipolar Mode		275	375		275	375		275	375	pF
	Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput											
Conversion Time (Notes 6, 7)	–16			16.25			16.25			16.25	us
	–32			32.5			32.5			32.5	us
Acquisition Time (Note 7)	–16		3.0	3.75		3.0	3.75		3.0	3.75	us
	–32		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput (Note 7)	–16	50			50			50			kHz
	–32	26.5			26.5			26.5			kHz
Power Supplies											
Power Supply Currents (Note8)											
I_{A+}			9	19		9	19		9	19	mA
I_{A-}			–9	–19		–9	–19		–9	–19	mA
I_{D+}			3	6		3	6		3	6	mA
I_{D-}			–3	–6		–3	–6		–3	–6	mA
Power Dissipation	(Note 8)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 9)											
Positive Supplies			84			84			84		dB
Negative Supplies			84			84			84		dB

Notes:
4. Refer to the *Analog Input* section on page 75 for a discussion of input slew capabilities.
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15pF.
6. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
7. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CSZ5116's conversion clock, interleave calibrate is disabled, and operation is from the full-rated external clock. A detailed discussion of conversion timing appears on page 69.
8. All outputs unloaded. All inputs CMOS levels.
9. With 300mV p-p, 1kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection appears on page 82.

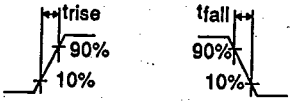
T-51-10-16

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF)

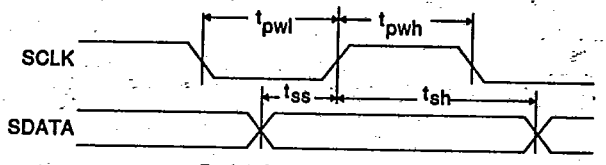
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: -16	f_{CLK}	2	-	-	MHz
-32		1	-	-	
Externally Supplied: -16		-	-	4	
-32		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 10)	-	(Note 10)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 11)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-J, K, L, A, B, C	t_{ca}	-	90	120	ns
-S, T, U		-	115	150	
$\overline{RD}$ Low to Data Valid					
-J, K, L, A, B, C	t_{ra}	-	90	120	ns
-S, T, U		-	115	150	
Output Float Delay: -J, K, L, A, B, C	t_{fd}	-	50	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -S, T, U		-	50	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Notes: 10. See Table 1 and master clock frequencies above.

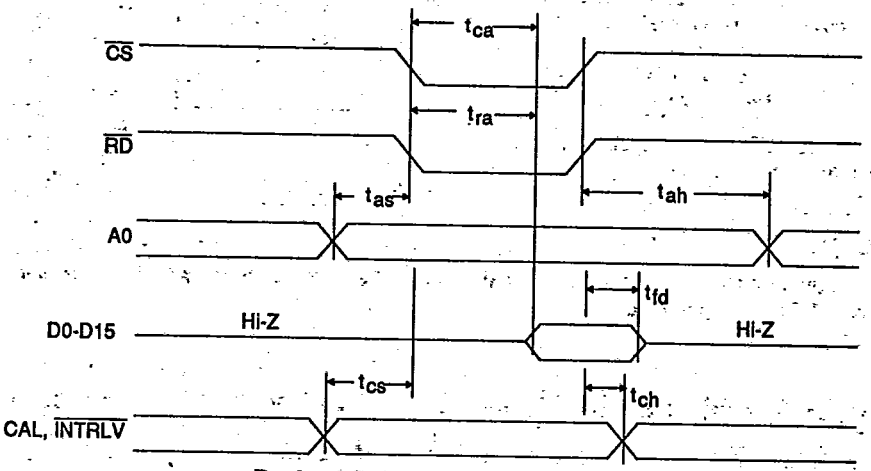
11. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



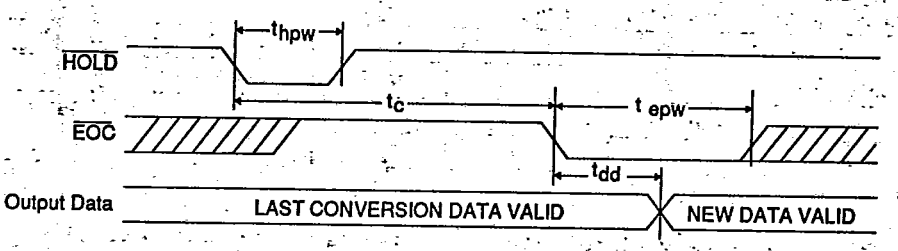
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

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DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 12. I_{OUT} = -100µA. This specification guarantees TTL compatibility (VOH = 2.4V @ Iout = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 13.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage: (Note 14)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 13. All voltages with respect to ground.
14. The CSZ5116 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 15)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Note: 15. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

The CSZ5116 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the input to the DAC output set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next-MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

The CSZ5116 implements the successive-approximation algorithm using a unique charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All legs of the array share a common node at the comparator's input, with their other terminals capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all bits are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps

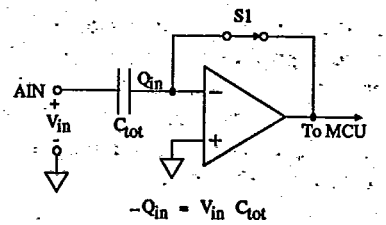


Figure 2a. Tracking Mode

charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

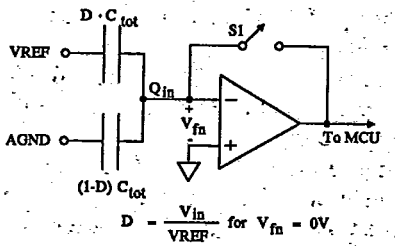


Figure 2b. Convert Mode

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of

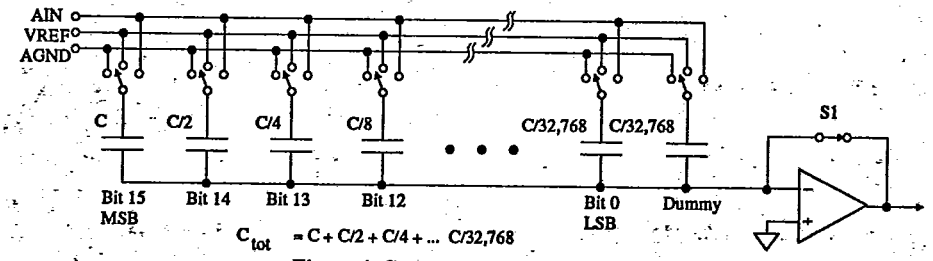


Figure 1. Charge Redistribution DAC

capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

The CSZ5116's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range doubles and offsets half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CSZ5116 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The CSZ5116 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CSZ5116 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). During calibration, the CSZ5116 implements statistical noise reduction to calibrate accurately to ± 1/4 LSB. It performs multiple experiments per calibration decision to reduce the effective noise bandwidth and the probability of making an incorrect decision. The resulting probability of obtaining a 1/4 LSB error is less than one in a thousand, with a negligible chance of obtaining a calibration error of 1/2 LSB.

DIGITAL CIRCUIT CONNECTIONS

The CSZ5116 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8- and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CSZ5116 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by hard-wiring the CLKIN input low. Alternatively, the CSZ5116 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

a. Asynchronous Sampling

b. Synchronous Sampling

Figure 3. Sampling Connections

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CSZ5116's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -16 version of the CSZ5116 is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2.0MHz. The -32 version can handle external clocks up to 2MHz; its internal clock can range as low as 1.0MHz (see *Switching Characteristics*, page 64).

Sampling/Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CSZ5116 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CSZ5116 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CSZ5116, in turn, depends on the sampling, calibration, and master clock conditions.

Asynchronous Sampling

The CSZ5116 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{\text{HOLD}}$ goes low even though the charge is trapped immediately. In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 65 clock cycles to define the maximum conversion time (see Figure 4a and Table 1).

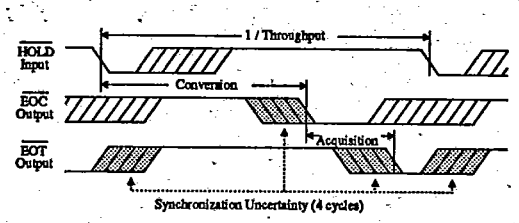


Figure 4a. Asynchronous Sampling (External Clock)

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	65T	65T	80T	80T
Asynchronous	65T	69T + 235ns	N/A	75T + 2.25µs

(T = one master clock cycle)

Table 1. Conversion and Throughput Times

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CSZ5116's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/80th of the master clock frequency (see Figure 4b and Table 1).

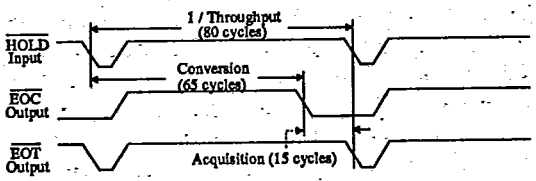


Figure 4b. Synchronous (Loopback) Mode

Also, the CSZ5116's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CSZ5116 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

The $\overline{EOT}$ output is an accurate indicator of the CSZ5116's acquisition requirement when operating at the -16 version's full rated speed (3.75µs with a 4MHz master clock). However, $\overline{EOT}$ will allow the CSZ5116 more acquisition time than necessary when operating with a clock less than 4MHz. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$. The CSZ5116 only needs 3.75µs (six cycles @4MHz plus 2.25µs). When operating the -32 with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of $\overline{EOC}$ and count the appropriate number of clock cycles after each conversion. When the total time is greater than six clock cycles plus 2.25µs the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

Upon power up, the CSZ5116 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CSZ5116's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before RST falls to guarantee an accurate calibration. Later, the CSZ5116 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CSZ5116 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CSZ5116 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles (approximately

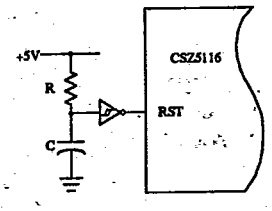


Figure 5. Power-On Reset Circuitry

360ms with a 4MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 5). The CSZ5116 can also be reset in software when under microprocessor control. The CSZ5116 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CSZ5116 is ready for operation. Six master clock cycles plus 2.25µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; AO high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CSZ5116's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (8.75µs @ 4MHz clock) must be allowed before a conversion is initiated to ensure the CSZ5116 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 89.)

The CSZ5116 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CSZ5116 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CSZ5116's effective conversion time by 20 master clock cycles. Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CSZ5116 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be hard-wired low.

Microprocessor Interface

The CSZ5116 features an intelligent microprocessor interface which offers detailed status

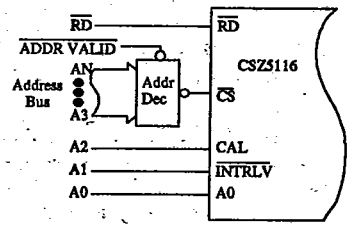


Figure 6. Address/Control Bus Connections

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/HIGH BYTE	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

information and allows software control of the self-calibration functions. Output data is available in either 8- or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low enables the CSZ5116's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 6 thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{\text{HOLD}}$ is low, or a software reset will result* (see *Reset*, page 70).

Alternatively, the End-of-Convert ($\overline{\text{EOC}}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{\text{EOC}}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle. To interface with 16-bit data busses, the BW input to the CSZ5116 should be held high and all 16 data bits read in parallel. With 8-bit buses, the converter's 16-bit result must be read in two 8-bit bytes. In this instance, BW should be held low and the MSB's obtained on the first read cycle following a conversion and the LSB's on the second. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S4 indicates which byte will appear on the next data read operation.

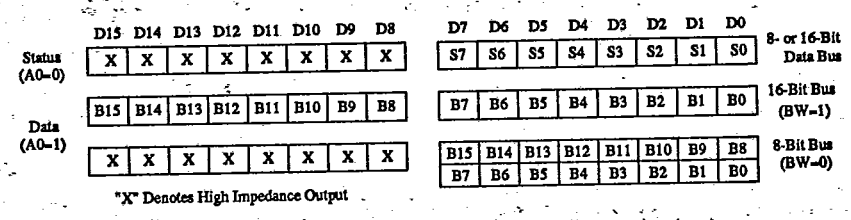


Figure 7. Data Format

The CSZ5116 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CSZ5116 is converting will not introduce conversion errors. When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The two calibration control inputs, CAL and $\overline{\text{INTRLV}}$, are level-triggered and latched on the rising edge of $\overline{\text{CS}}$. Calibration can be placed under software control by connecting address lines to the CAL and $\overline{\text{INTRLV}}$ inputs as shown in Figure 6. Any read or write cycle to the CSZ5116's base address will thereby initiate or terminate calibration.

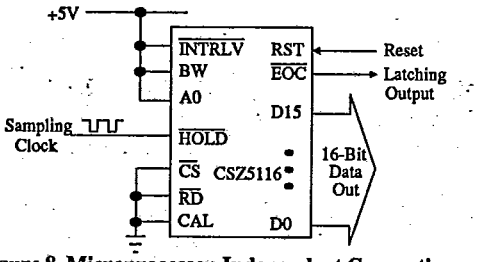
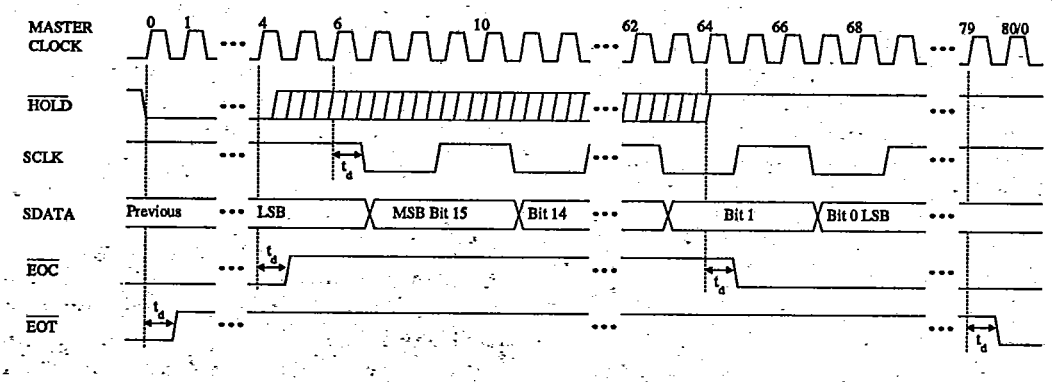


Figure 8. Microprocessor-Independent Connections

Microprocessor Independent Operation

The CSZ5116 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{\text{HOLD}}$ is continually strobed low or tied to $\overline{\text{EOT}}$. The CSZ5116's $\overline{\text{EOC}}$ output can be used to externally latch the output data if desired. With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ hard-wired low, $\overline{\text{EOC}}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{\text{EOC}}$ falls, so it should be latched on the rising edge of $\overline{\text{EOC}}$.



notes: 1. t_d can vary from 135ns - 235ns over military temerature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{\text{EOC}}$, $\overline{\text{EOT}}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SCLK, SDATA, $\overline{\text{EOC}}$, and $\overline{\text{EOT}}$ is fixed.

Figure 9. Serial Output Timing

Serial Output

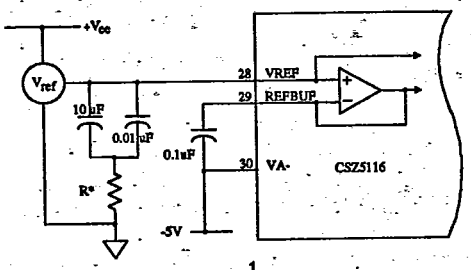
All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CSZ5116 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CSZ5116 (See Figure 9).

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CSZ5116 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage references for the CS501X/CSZ511X Series of A/D Converters*" is available for the CSZ5116. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.



$$R = \frac{1}{2\pi (C_1 + C_2) f_{peak}}$$

Figure 10. Reference Connections

During conversion, the members of the calibrated capacitor array are switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CSZ5116 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CSZ5116 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly.

As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4MHz clock), the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 2Ω will therefore yield a maximum error of 20µV. With a 4.5V reference and LSB size of 69µV this would insure approximately 1/4 LSB accuracy. A 10µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz, and voltage references with dc output impedances less than one 2Ω are readily available. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CSZ5116 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CSZ5116 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

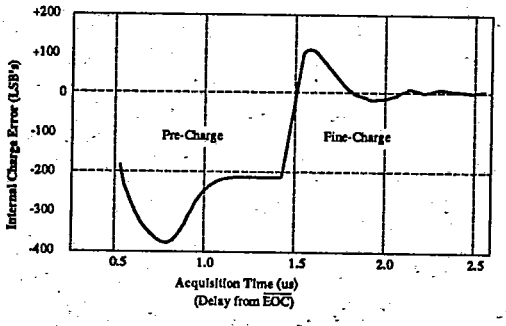


Figure 11. Internal Acquisition Time

The acquisition time of the CSZ5116 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -16 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω.

In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN

to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CSZ5116 can track full power signals up to 25kHz in the track mode. During the first six clock cycles following a conversion, the CSZ5116 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CSZ5116 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CSZ5116 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CSZ5116 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111111, and negative full scale gives a digital output of 0000000000000000.

Grounding and Power Supply Decoupling

The CSZ5116 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CSZ5116 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If significant lowfrequency noise is present on the supplies, 1µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

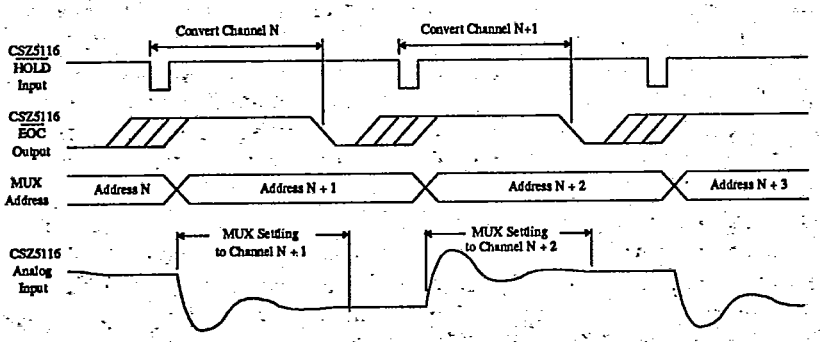


Figure 12. Pipelined MUX Input Channels

The positive digital power supply of the CSZ5116 must never exceed the positive analog supply by more than a diode drop or the CSZ5116 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 83 shows a decoupling scheme which allows the CSZ5116 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CSZ5116 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CSZ5116. The CDB5116 evaluation board is available for the CSZ5116, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CSZ5116, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CSZ5116 PERFORMANCE

The CSZ5116 offers 100% tested dynamic performance. Due to the broad range of operating conditions and performance requirements in signal processing applications, the following section is included to illustrate the CSZ5116's error sources and their effect on a signal's spectral content.

FFT Tests and Windowing

In the factory, the CSZ5116 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CSZ5116, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CSZ5116.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CSZ5116 has a maximum side-lobe level of -92dB. Figure 13 shows an FFT computed from an ideal 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics

and the -92dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83.

Nonlinearity

Analog-to-digital converters have traditionally been specified using dc specifications such as Integral and Differential Nonlinearity at worst-case points on the transfer curve. These specifications are not particularly useful in signal processing applications since they offer little information on the overall shape of converter's transfer curve, and therefore do not directly correlate to the converter's effect on a signal's spectral content.

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows and waves in the transfer curve generate harmonic distortion. However, the most prevalent source of nonlinearity in high-resolution converters is bit-weight errors; that is, the deviation of bits from their ideal binary-weighted ratios. At dc, bit-weight errors most visibly affect the converter's Differential Nonlinearity, or the deviation of codes from their ideal widths. Due to the limitations of factory trim techniques, the worst-case condition of bit-weight errors has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CSZ5116 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CSZ5116 calibrates its bit weights to ± 1/4 LSB at 16-bits (± 0.0004% FS) yielding peak distortion as low as -105dB (see Figure 14). Unlike traditional ADC's, the linearity of the CSZ5116 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

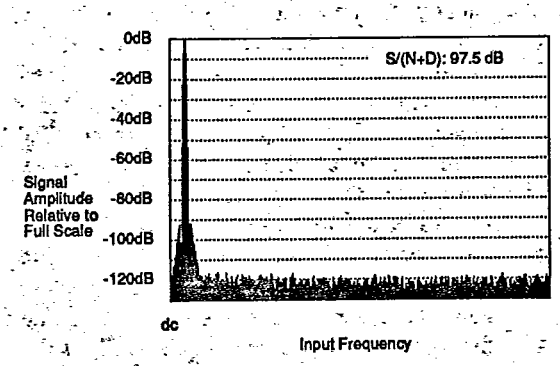


Figure 13. FFT Plot of Ideal 16-bit Signal

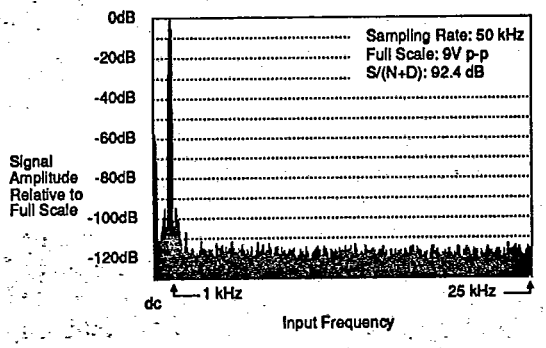


Figure 14. FFT Plot with 1kHz Full-Scale Input

Sampling Distortion

The ultimate limitation on the CSZ5116's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 14).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figure 15 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. With signals 20dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figure 16).

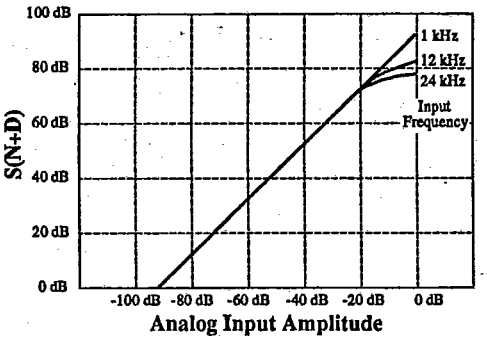


Figure 15. S/(N+D) vs. Input Amplitude (9V p-p Full-Scale Input)

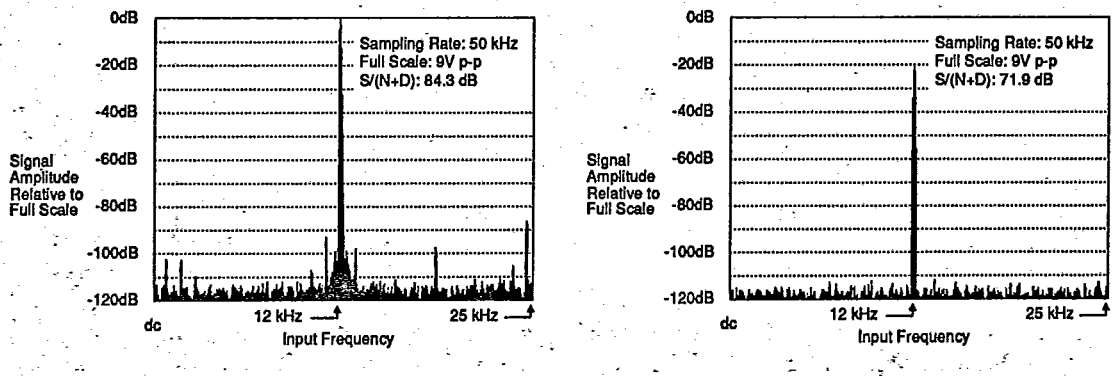


Figure 16. FFT Plots of 12kHz Signals at Full-Scale and 20dB Below Full-Scale

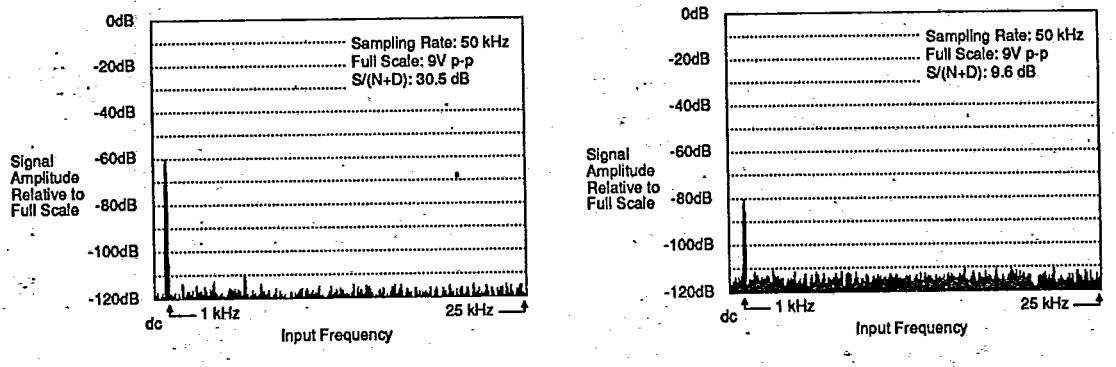


Figure 17. FFT plots of 1kHz Signals 60dB and 80dB Below Full Scale

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop accross the switches. Since the CSZ5116 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurance. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 16-bit signal-to-noise ratio of 98.1dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

As illustrated in Figures 15 and 17, the CSZ5116's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the CSZ5116 which dictates the converter's signal-to-noise performance.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CSZ5116 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CSZ5116's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CSZ5116's output. The offset could theoretically reach the peak coupling magnitude (Figure 18), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50Ω	15uV	70uV
External	2MHz	50Ω	25uV	110uV
External	4MHz	50Ω	40uV	150uV
External	4MHz	25Ω	25uV	110uV
External	4MHz	200Ω	80uV	325uV

Figure 18. Examples of Measured Clock Feedthrough

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CSZ5116's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (Nf_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CSZ5116's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 18, a typical CSZ5116 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance will exhibit only 15μV rms of clock feedthrough (-116dB with a 9V p-p full scale). However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25μV rms(-111dB). Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms (-107dB). Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 18, reducing source impedance from 50Ω to 25Ω yields a 15μV rms reduction in feedthrough. Therefore, when operating the CSZ5116 with high-frequency external master clocks, it is important to minimize source impedance applied to the CSZ5116's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CSZ5116 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependancy causes distortion at high frequencies. The CSZ5116's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter assumes a random nature and appears in an FFT as a spreading in the fundamental. With only 100ps peak-to-peak aperture jitter, the CSZ5116 can process full-scale signals up to 24kHz with 16-bit accuracy.

Power Supply Rejection

The CSZ5116's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CSZ5116's accuracy. This, of course, is because

the CSZ5116 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 19 shows power supply rejection of the CSZ5116 in the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each supply. Power supply rejection improves by 6dB in the unipolar mode.

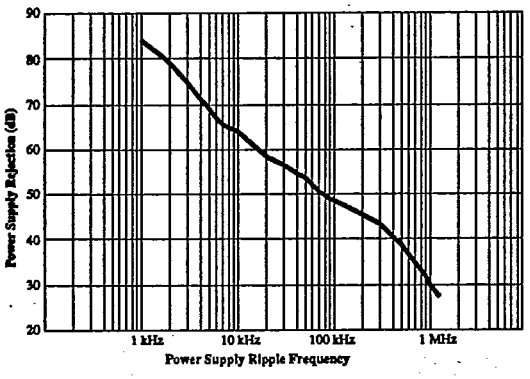


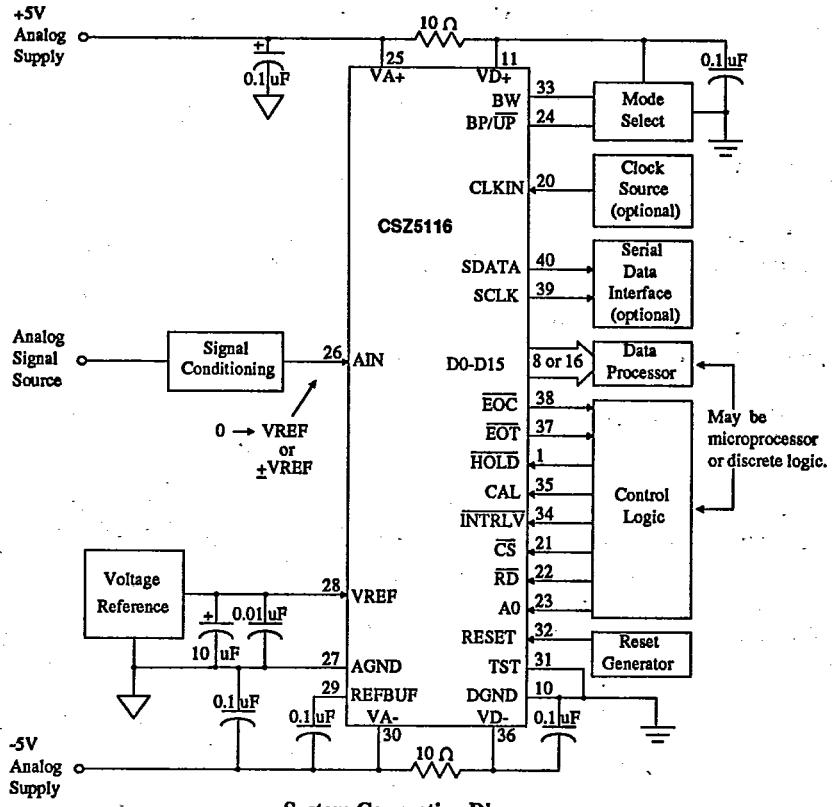
Figure 19. Power Supply Rejection

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

HOLD	CS	CAL	INTRLV	RD	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

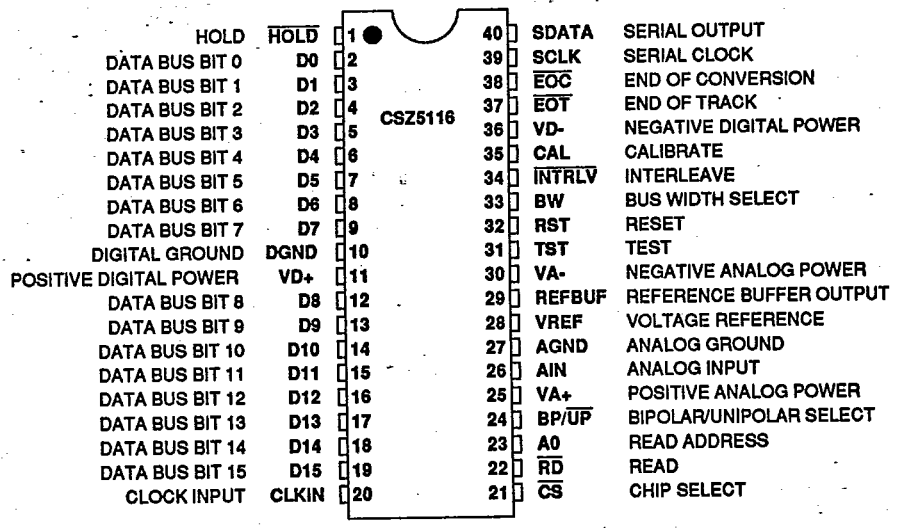
* The status of A0 is not critical to the operation specified. However, A0 should not be low with CS and HOLD low, or a software reset will result.

CSZ5116 Truth Table



System Connection Diagram

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.

Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.

A falling transition on this pin sets the CSZ5116 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.

When high, the data bus outputs are held in a high impedance state and the inputs to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

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$\overline{\text{RD}}$ - Read, PIN 22.

When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 - Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon returing low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When high, all 16 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the eight LSB's on D7-D0. Subsequent reads will toggle the higher/lower order bytes of the same data until the next conversion completes. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 72,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 89.)

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning calibration.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in the bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

Tri-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 16-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer the status register.

$\overline{\text{EOT}}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75µs for 4MHz external clock).

$\overline{\text{EOC}}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or reset calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CSZ5116. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST - Test, PIN 31.

Allows access to the CSZ5116's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been externally compensated. Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Zero Error - The deviation of the first code transition from the ideal (1/2 LSB above -VREF) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

CRYSTAL

T 51-10-16

Ordering Guide

Model	Signal to Noise Ratio	Throughput	Temp. Range	Package
CSZ5116-JC32	87 dB	26.5 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-JC16	87 dB	50 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-KC32	90 dB	26.5 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-KC16	90 dB	50 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-LC32	92 dB	26.5 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-LC16	92 dB	50 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-AC32	87 dB	26.5 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-AC16	87 dB	50 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-BC32	90 dB	26.5 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-BC16	90 dB	50 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-CC32	92 dB	26.5 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-CC16	92 dB	50 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-SC16	87 dB	50 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-TC16	90 dB	50 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-UC16	92 dB	50 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CSZ5116's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.