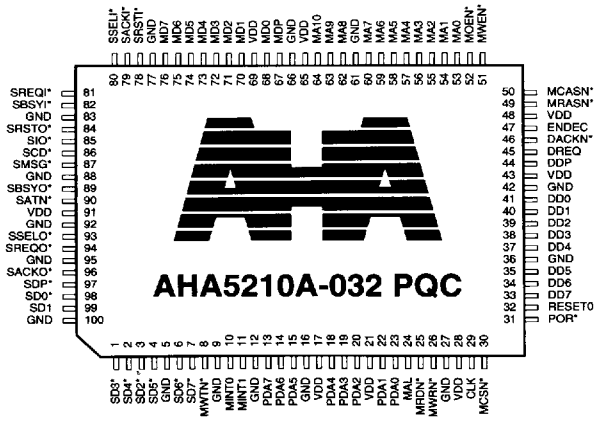
PRODUCT BRIEF*

AHA5210

MAGNETO-OPTICAL CONTROLLER

The AHA5210 is a highly integrated, efficient device optimized for embedded controller applications in an ISO JTC1/SC23 CD10090 (90mm) 3.5 inch Optical Drive. The controller fully supports the ANSI and ISO industry standard optical disk formats for CCS (Continuous Composite Servo). The high level of integration and the optimized pinout of the AHA5210 make it suitable for embedded controller applications especially for 90mm drives where only limited board space is available.

The AHA5210 contains an NCR53C90A compatible SCSI block, full hardware "on-the-fly" error detection and correction, DRAM interface, a complete DMA controller, and 8 bit plus parity DMA-like interface to an external Encoder/Decoder (ENDEC) device. The AHA5210 and the ENDEC, along with buffer memory, a data separator, and a local microcontroller with system ROM and RAM, make a complete high performance optical disk controller subsystem at a low cost. In addition, it is possible to dramatically lower system power consumption by using the power down modes in the AHA5210 device.



NOTE: "" indicates an active low signal.*

FEATURES

DRIVE INTERFACE:

- Performs full "on-the-fly" Reed Solomon Error Correction
- Fully complies with 3.5 inch MO disk ISO/ANSI standard for Continuous Composite Servo and Vendor Unique Bytes (VUB)
- Supports up to 4 Mbytes/sec NRZ data rates

DMA CONTROLLER:

- Directly addresses up to 4 Mbytes DRAM
- Permits concurrent buffer memory throughput up to 10 Mbytes/sec with 80 ns DRAMs
- Provides DRAM refresh
- Generates and checks odd or even parity
- Controls circular buffer with priority resolution for host, refresh, microcontroller and drive interface

SCSI INTERFACE:

- Complies with ANSI SCSI-II standard specification
- 53C90A compatible SCSI controller
- Supports synchronous or asynchronous data rates up to 5.3 Mbytes/second
- Connects directly to single ended SCSI bus with built-in 48 mA bus drivers
- Contains a 31-byte SCSI FIFO

OTHER FEATURES:

- 100 pin QFP for 5210
- Multiple power down modes
- Multiplexed address/data lines

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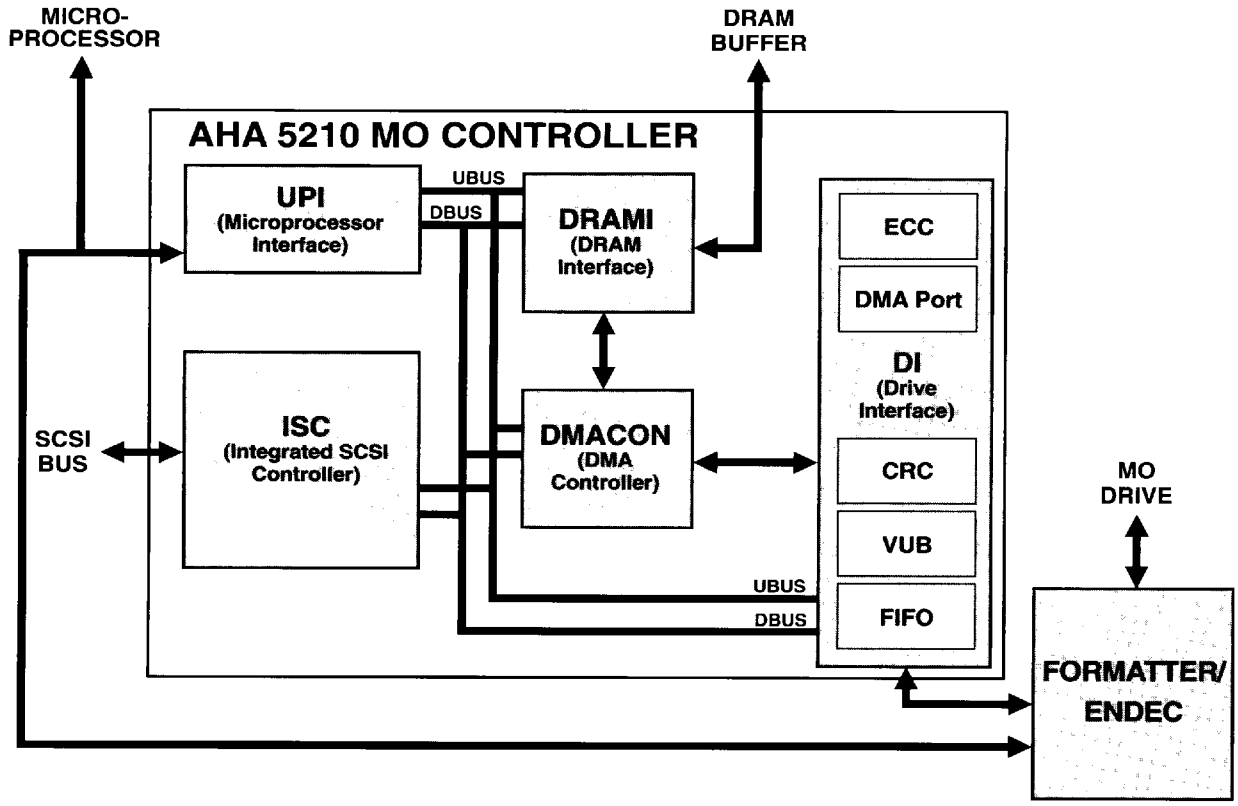
*Request the *AHA5210* Product Specification for complete details



FUNCTIONAL DESCRIPTION

The AHA5210 Controller is typically used in a system including an ENDEC, a data separator, buffer memory and a local microcontroller with system ROM and RAM. The 5210 may either be memory mapped or in the I/O space of the microcontroller. It communicates with the microcontroller via a multiplexed address and data path similar to the Intel class of microcontrollers. All controller functions are programmable by the microcontroller via read/write registers. This provides maximum firmware control over drive operation allowing for various retry methods and other vendor unique requirements. Interrupts are designed for ease of access and simplified interrogation from the microcontroller.

An on-board SCSI interface, compatible with the NCR53C90A IC, provides direct interface to single ended SCSI interface. All of the SCSI functions defined in the ANSI standard are performed by an internal hardware-based sequencer through high level commands from the microcontroller. Most of these common SCSI sequences are performed by a single microcontroller command. Each command can be programmed to transfer data either between the SCSI bus, DRAM buffer, the internal FIFO and the microcontroller. The AHA5210 has synchronous and asynchronous modes.

The on-board DRAM interface allows the AHA5210 to directly connect up to 4 Megabytes of DRAM which may optionally be refreshed in low power mode. The AHA5210 can use 80ns/100ns/120ns DRAMS with very flexible programmable periods. The DRAM can be accessed via an internal register using an auto-increment address function.

The Reed-Solomon error correction block works transparently to the microcontroller and performs all detection and correction of errors and provides statistics to the microcontroller. It provides "on-the-fly" correction of all sector errors (including worst case errors) within the sector "gap-time." This block capitalizes on AHA's world renowned leadership in Reed-Solomon error correction by implementing a high speed detection and correction engine.

The internal DMA controller/buffer manager provides maximum DRAM buffer bandwidth as well as DRAM refreshes. The DMA subsystem is fully buffered allowing efficient transfer of data from the SCSI bus to and from DRAM, data transfers from the MO drive, error correction data from

the ECC block to the DRAM, and microcontroller access to the DRAM.

The AHA5210 represents the first in a line of MO controller devices from AHA. AHA will continue to develop additional MO and QIC formatters and controllers with and without SCSI data compression devices, and error correction devices that optimize firmware compatibility, integration and system cost. Custom versions can be provided.

AHA has a full line of Data Compression Devices, Reed-Solomon CODECs, QIC (Quarter Inch Cartridge) formatters/controllers and MO Controllers as well as a full complement of Full Custom VLSI designers.

AHA5210 REGISTER ADDRESS MAP

ADDRESS	REGISTER
0x00	SAA0-SCSI Active Address 0
0x01	SAA1-SCSI Active Address 1
0x02	SAA2-SCSI Active Address 2
0x03	DMAC-DMA Control
0x04	SAC0-SCSI Active Transfer Count 0
0x05	SAC1-SCSI Active Transfer Count 1
0x06	SAC2-SCSI Active Transfer Count 2
0x07	DMAI-DMA Interrupts
0x08	SPA0-SCSI Pre-arm Address 0
0x09	SPA1-SCSI Pre-arm Address 1
0x0A	SPA2-SCSI Pre-arm Address 2
0x0B	UPC-Microprocessor Control
0x0C	SPC0-SCSI Pre-arm Transfer Count 0
0x0D	SPC1-SCSI Pre-arm Transfer Count 1
0x0E	SPC2-SCSI Pre-arm Transfer Count 2
0x0F	DMAM-DMA Interrupt Mask
0x10	DAA0-Drive Active Address 0
0x11	DAA1-Drive Active Address 1
0x12	DAA2-Drive Active Address 2
0x13	DWS-DRAM Wait States
0x14	DAC0-Drive Active Transfer Count 0
0x15	DAC1-Drive Active Transfer Count 1
0x16	DAC2-Drive Active Transfer Count 2
0x17	RC-DRAM Refresh Count
0x18	DPA0-Drive Pre-arm Address 0
0x19	DPA1-Drive Pre-arm Address 1
0x1A	DPA2-Drive Pre-arm Address 2
0x1B	RIC-DRAM Interface Configuration
0x1C	DPC0-Drive Pre-arm Transfer Count 0
0x1D	DPC1-Drive Pre-arm Transfer Count 1
0x1E	DPC2-Drive Pre-arm Transfer Count 2
0x1F	Reserved

ADDRESS	REGISTER
0x20	UA0-Microprocessor Address 0
0x21	UA1-Microprocessor Address 1
0x22	UA2-Microprocessor Address 2
0x23	MDMA-Microprocessor DMA Data Window
0x24	EC0-Error Threshold/Count Per Sector
0x25	EC1-Error Threshold/Count Per Interleave
0x26	Reserved
0x27	Reserved
0x28	VNUB0-Vendor Unique Byte 0
0x29	VNUB1-Vendor Unique Byte 1
0x2A	VNUB2-Vendor Unique Byte 2
0x2B	NVUB3-Vendor Unique Byte 3
0x2C	DICTR0-Drive Interface Control 0
0x2D	DICTR1-Drive Interface Control 1
0x2E	DII-Drive Interface Interrupts
0x2F	DIM-Drive Interface Interrupt Mask
0x30	Reserved
0x31	Reserved
0x32	ISCFIFO-SCSI FIFO
0x33	ISCCOM-SCSI Command Reg.
0x34	ISCSTAT-SCSI Status/Dest. ID
0x35	ISCINTR-SCSI Int/Timeout Value
0x36	ISCSEQ-SCSI Sequence/Sync Offset
0x37	ISCFCNT-SCSI FIFO Count/Sync Offset
0x38	ISCCFG1-SCSI Configuration 1
0x39	ISCTSF-SCSI Time Scaling Factor
0x3A	ISCTEST-SCSI Test Mode
0x3B	ISCCFG2-SCSI Configuration 2
0x3C	Reserved
0x3D	Reserved
0x3E	Reserved
0x3F	SNP-Select Normal Power

PINOUT LIST

A. MICROPROCESSOR INTERFACE

NAME	TYPE	DEFINITION
MRDN*	I	Microprocessor Read
MWRN*	I	Microprocessor Write
MWTN*	O, O/D	Microprocessor Wait
MCSN*	I	Microprocessor Chip Select
PDA[7:0]	I/O	Local Microprocessor Address/Data
POR*	I	Power on Reset
RESETO	O	Reset Output
MAL	I	Microprocessor Address Larch
MINTO	O	Interrupt 0
MINT1	O	Interrupt 1
CLK	I	Clock

B. INTEGRATED SCSI CONTROLLER (ISC)

NAME	TYPE	DEFINITION
SD[7:0]	I/O, O/D, S	SCSI Data Bus
SDP*	I/O, O/D, S	SCSI Data Bus Parity
SATN*	I/O, O/D, S	SCSI Attention
SBSYI*	I/S	SCSI Busy
SBSYO*	O, O/D	SCSI Busy
SACKI*	I/S	SCSI Acknowledge
SACKO*	O, O/D	SCSI Acknowledge
SRSTI*	I/S	SCSI Reset
SRSTO*	O, O/D	SCSI Reset
SSELI*	I/S	SCSI Select
SSELO*	O, O/D	SCSI Select
SREQI*	I/S	SCSI Request
SREQO*	O, O/D	SCSI Request
SIO*	I/O, O/D, S	SCSI Input/Output
SCD*	I/O, O/D, S	SCSI Command/Data
SMSG*	I/O, O/D, S	SCSI Message

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C. DRAM INTERFACE

NAME	TYPE	DEFINITION
MD[7:0]	I/O	Buffer Memory Data Bus
MDP	I/O	Buffer Memory Parity
MA[0:10]	O	Buffer Memory Address Bus
MOEN*	O	Memory Output Enable
MWEN*	O	Write Enable
MRASN*	O	Row Address Strobe
MCASN*	O	Column Address Strobe

D. DRIVE INTERFACE

NAME	TYPE	DEFINITION
DD[7:0]	I/O	Drive Data
DDP	I/O	Drive Data Parity
DREQ	I	Drive Request
DACKN*	O	Drive Acknowledge
ENDEC	I/O	Encode/Decode

E. OTHERS

NAME	TYPE	DEFINITION
VDD		Supply Voltage
GND		Ground

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
AHA5210A-032 PQC	Magneto Optical Formatter/Controller

TECHNICAL PUBLICATION

DOCUMENT #	DESCRIPTION
PS5210	AHA5210 Product Specification
PS5102	AHA5102 QIC Controller Specification
ANMO01	MO Controller Design Techniques Using the AHA5210
ANMO02	Programming the AHA5210
ANMO03	Customizing the AHA5210 for ISO Applications
GLGEN1	General Glossary of Terms

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