

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789322, 789324, 789326, and 789327 are μPD789327 Subseries (designed for remote controller with on-chip LCD) product in the 78K/0S Series.

In addition to an 8-bit CPU, they have on-chip hardware for a remote controller with on-chip LCD, including a LCD controller/driver, a serial interface, a key return signal detection circuit, and timers with carrier generator that can easily output waveforms for infrared remote control.

The μPD78F9328, a product with on-chip flash memory which can operate on the same supply voltage as for masked ROM products and various development tools are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789327, 789467 Subseries User's Manual: To be prepared

78K/0S Series User's Manual Instructions: U11047E

FEATURES

- ROM and RAM size

| Item Part Number | Program memory (ROM) | Data Memory | | Package |
|---------------------|-------------------------|----------------------------|-----------------|-----------------------------------|
| | | Internal High-Speed RAM | LCD display RAM | |
| μPD789322 | 4 K bytes | 256 bytes | 24 bytes | 52-pin plastic LQFP (10×10 mm) |
| μPD789324 | 8 K bytes | | | |
| μPD789326 | 16 K bytes | 512 bytes | | |
| μPD789327 | 24 K bytes | | | |

- Variable minimum instruction execution time: High speed (0.4 μs: @5.0-MHz operation with main system clock), low speed (1.6 μs: @5.0-MHz operation with main system clock), and ultra low speed (122 μs: @32.768-kHz operation with subsystem clock)
- I/O ports: 21
- Serial interface (3-wire serial I/O mode): 1 channel
- LCD controller/driver
Segment signals: 24
Common signals: 4
- Timer: 4 channels
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Remote-control devices, healthcare equipment, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

| Part Number | Package |
|--------------------------|--------------------------------|
| μ PD789322GB-xxx-8ET | 52-pin plastic LQFP (10×10 mm) |
| μ PD789324GB-xxx-8ET | 52-pin plastic LQFP (10×10 mm) |
| μ PD789326GB-xxx-8ET | 52-pin plastic LQFP (10×10 mm) |
| μ PD789327GB-xxx-8ET | 52-pin plastic LQFP (10×10 mm) |

Remark xxx Indicates ROM code suffix.

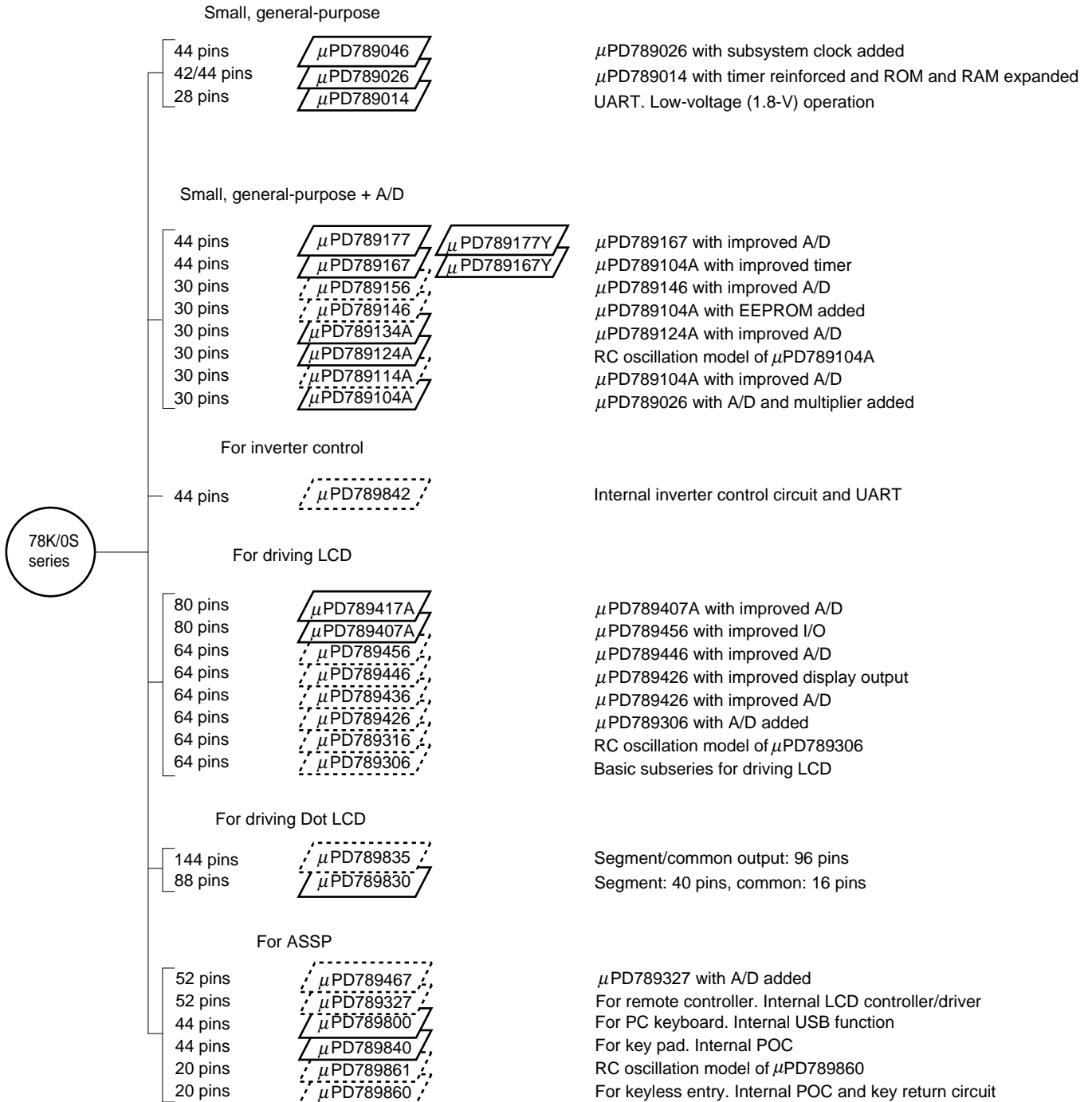
78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.

 Products under mass production

 Products under development

Y subseries supports SMB.



The major differences between subseries are shown below.

| Function Subseries Name | | ROM Capacity | Timer | | | | 8-bit A/D | 10-bit A/D | Serial Interface | I/O | V _{DD} MIN Value | Remark |
|--|------------|-----------------|-------|-------------|-------|------|--------------|---------------|-------------------|--------------------|---------------------------------|--|
| | | | 8-bit | 16-bit | Watch | WDT | | | | | | |
| Small, general- purpose | μPD789046 | 16 K | 1 ch | 1 ch | 1 ch | 1 ch | – | – | 1 ch (UART:1 ch) | 34 pins | 1.8 V | – |
| | μPD789026 | 4 K-16 K | | | – | | | | | | | |
| | μPD789014 | 2 K-4 K | 2 ch | – | | | | | | 22 pins | | |
| Small, general- purpose + A/D | μPD789177 | 16 K-24 K | 3 ch | 1 ch | 1 ch | 1 ch | – | 8 ch | 1 ch (UART: 1 ch) | 31 pins | 1.8 V | – |
| | μPD789167 | | | | | | 8 ch | – | | | | |
| | μPD789156 | 8 K-16 K | 1 ch | – | – | – | – | 4 ch | 20 pins | | | Internal EEPROM |
| | μPD789146 | | | | | | 4 ch | – | | | | |
| | μPD789134A | 2 K-8 K | | | | | – | 4 ch | | | | RC oscillation version |
| | μPD789124A | | | | | | 4 ch | – | | | | |
| | μPD789114A | | | | | | – | 4 ch | | | | |
| | μPD789104A | | | | | | 4 ch | – | | | | |
| For inverter control | μPD789842 | 8 K-16 K | 3 ch | Note | 1 ch | 1 ch | 8 ch | – | 1 ch (UART: 1 ch) | 30 pins | 4.0 V | – |
| For LCD driving | μPD789417A | 12 K-24 K | 3 ch | 1 ch | 1 ch | 1 ch | – | 7 ch | 1 ch (UART: 1 ch) | 43 pins | 1.8 V | – |
| | μPD789407A | | | | | | 7 ch | – | | | | |
| | μPD789456 | 12 K-16 K | 2 ch | | | | – | 6 ch | | 30 pins | | |
| | μPD789446 | | | | | | 6 ch | – | | | | |
| | μPD789436 | | | | | | – | 6 ch | | 40 pins | | |
| | μPD789426 | | | | | | 6 ch | – | | | | |
| | μPD789316 | 8 K to 16K | | | | | – | – | 2 ch (UART: 1 ch) | 23 pins | | RC oscillation version |
| | μPD789306 | | | | | | – | – | – | – | | |
| For Dot LCD driving | μPD789835 | 24 K-60 K | 6 ch | – | 1 ch | 1 ch | 2 ch | – | 1 ch | 27 pins | 1.8 V | – |
| | μPD789830 | 24 K | 1 ch | 1 ch | | | – | – | 1 ch (UART: 1 ch) | 30 pins | 2.7 V | |
| ASSP | μPD789467 | 4 K-24 K | 2 ch | – | 1 ch | 1 ch | 1 ch | – | – | 18 pins | 1.8 V | Internal LCD |
| | μPD789327 | | | | | | – | | 1 ch | 21 pins | | |
| | μPD789800 | 8 K | 2 ch | 1 ch | – | 1 ch | – | | 2 ch (USB: 1 ch) | 31 pins | 4.0 V | – |
| | μPD789840 | | | | | | 4 ch | | 1 ch | 29 pins | 2.8 V | |
| | μPD789861 | 4 K | | – | | | – | | – | 14 pins | 1.8 V | RC oscillation version, Internal EEPROM |
| | μPD789860 | | | | | | – | | – | Internal EEPROM | | |

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

| Item | | μPD789322 | μPD789324 | μPD789326 | μPD789327 |
|--|-----------------|--|-----------|-----------|-----------|
| Internal memory | ROM | 4 Kbytes | 8 Kbytes | 16 Kbytes | 24 Kbytes |
| | High-speed RAM | 256 bytes | | 512 bytes | |
| | LCD display RAM | 24 bytes | | | |
| Main system clock (oscillation frequency) | | Ceramic/crystal resonator (1.0 to 5.0 MHz) | | | |
| Subsystem clock (oscillation frequency) | | Crystal resonator (32.768 kHz) | | | |
| Minimum instruction execution time | | 0.4 μs/1.6 μs (@5.0-MHz operation with main system clock) | | | |
| | | 122 μs (@32.768-kHz operation with subsystem clock) | | | |
| General-purpose registers | | 8 bits × 8 registers | | | |
| Instruction set | | <ul style="list-style-type: none"> • 16-bit operations • Bit manipulation (set, reset, test) etc. | | | |
| I/O ports | | Total: 21 CMOS I/O: 21 | | | |
| Timers | | <ul style="list-style-type: none"> • 8-bit timer: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel | | | |
| Timer outputs | | 1 | | | |
| Serial interface | | 3-wire serial I/O mode: 1 channel | | | |
| LCD controller/driver | | <ul style="list-style-type: none"> • Segment signal outputs: 24 • Common signal outputs: 4 | | | |
| Vectored interrupt sources | Maskable | Internal: 6, External: 2 | | | |
| | Non-maskable | Internal: 1 | | | |
| Reset | | <ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ signal input • Internal reset by watchdog timer • Reset via power-on-clear circuit | | | |
| Supply voltage | | $V_{DD} = 1.8$ to 5.5 V | | | |
| Operating ambient temperature | | $T_A = -40$ to $+85^\circ\text{C}$ | | | |
| Package | | 52-pin plastic LQFP (10×10 mm) | | | |

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1. PIN CONFIGURATION (TOP VIEW)

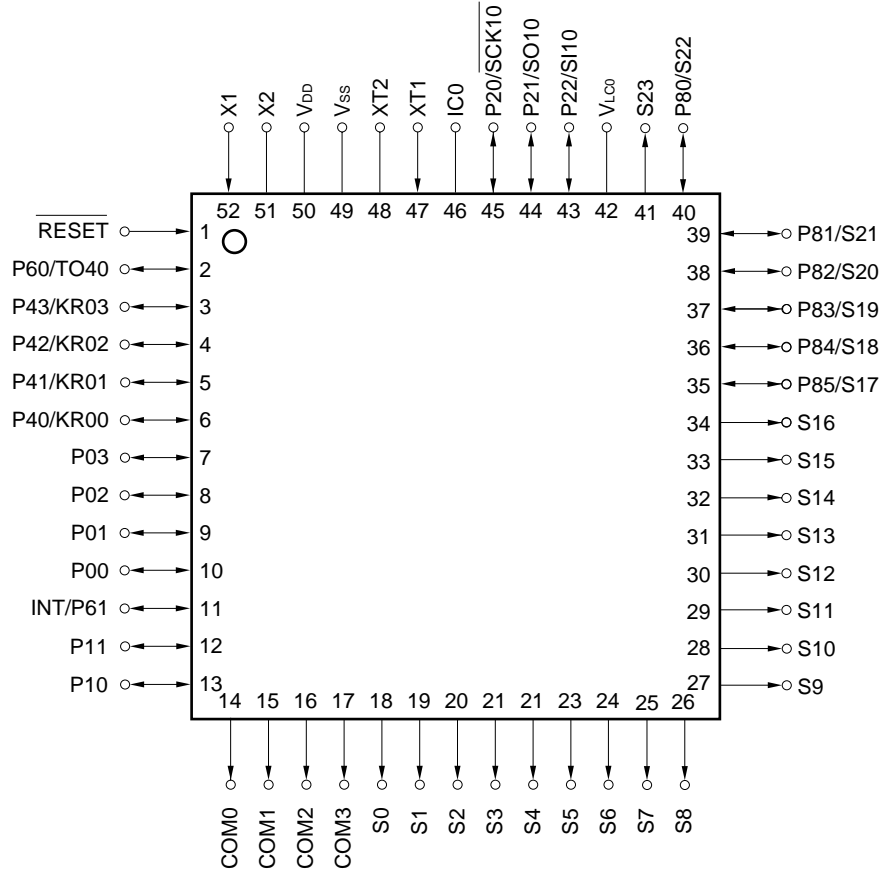
52-pin plastic LQFP (10×10 mm)

μPD789322GB-xxx-8ET

μPD789324GB-xxx-8ET

μPD789326GB-xxx-8ET

μPD789327GB-xxx-8ET



Caution Connect the IC0 (Internally Connected) pin directly to Vss.

COM0 to COM3: Common Output

IC0: Internally connected

INT: Interrupt from Peripherals

KR00 to KR03: Key Return

P00 to P03: Port 0

P10, P11: Port 1

P20 to P22: Port 2

P40 to P43: Port 4

P60, P61: Port 6

P80 to P85: Port 8

TO40: Timer Output

RESET: Reset

S0 to S23: Segment Output

SCK10: Serial Clock Input/Output

SI10: Serial Data Input

SO10: Serial Data Output

VDD: Power Supply

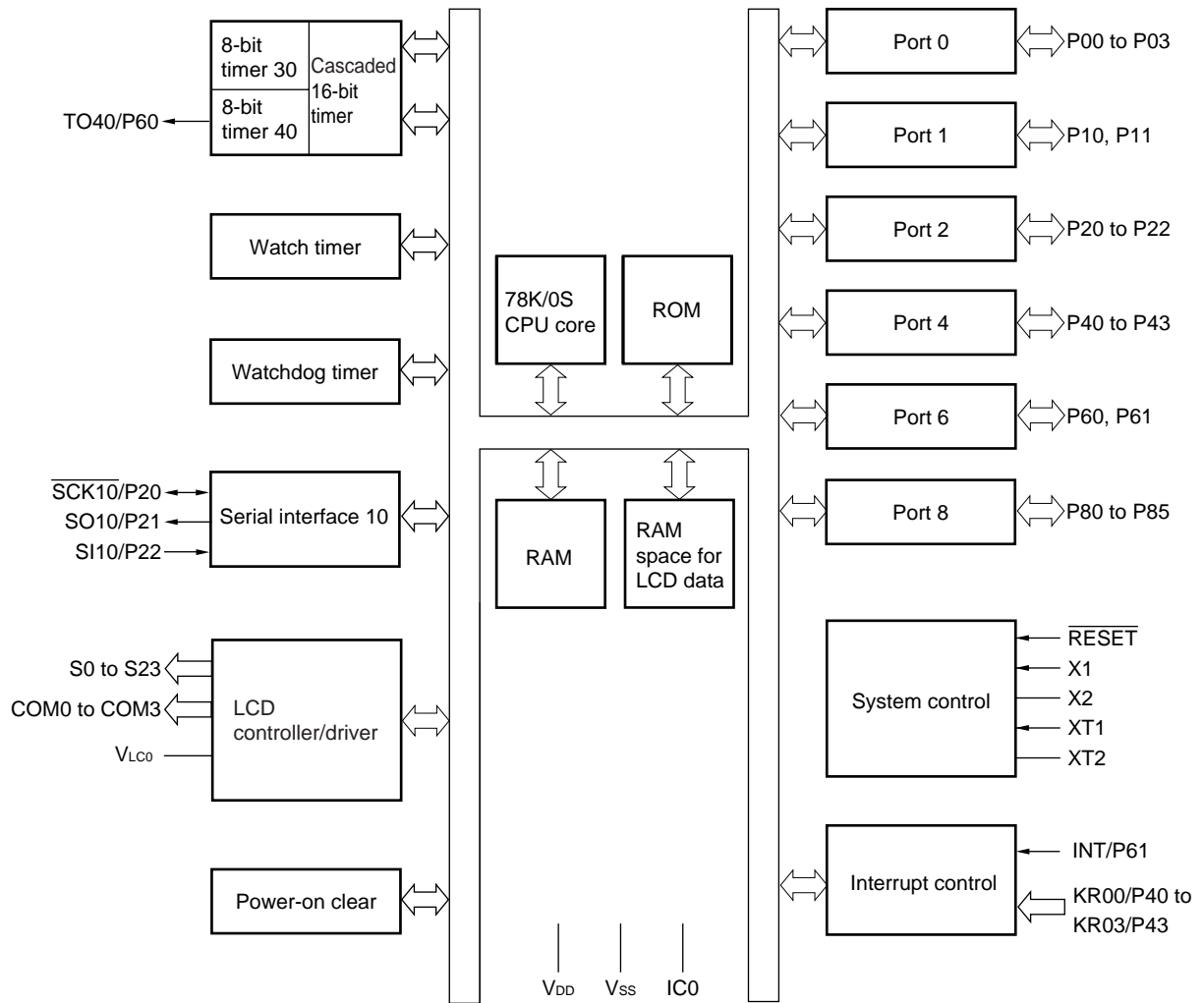
V_LCD: Power Supply for LCD

VSS: Ground

X1, X2: Crystal (Main system clock)

XT1, XT2: Crystal (Subsystem clock)

2. BLOCK DIAGRAM



Remark The Internal ROM and RAM capacities differ depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

| Pin Name | I/O | Function | After Reset | Alternate Function |
|------------|-----|--|------------------|--------------------|
| P00 to P03 | I/O | Port 0. This is a 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified for the whole port using pull-up resistor option register 0 (PU0). | Input | – |
| P10, P11 | I/O | Port 1. This is a 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified for the whole port using pull-up resistor option register 0 (PU0). | Input | – |
| P20 | I/O | Port 2. This is a 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified in 1-bit units using pull-up resistor option register 2 (PUB2). | Input | SCK10 |
| P21 | | | | SO10 |
| P22 | | | | SI10 |
| P40 to P43 | I/O | Port 4. This is a 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified for the whole port using pull-up resistor option register 0 (PU0), or key return mode register 00 (KRM00). | Input | KR00 to KR03 |
| P60 | I/O | Port 6. This is a 2-bit I/O port. Input/output can be specified in 1-bit units. | Input | TO40 |
| P61 | | | | INT |
| P80 to P85 | I/O | Port 8. This is a 6-bit I/O port. Input/output can be specified in 1-bit units. | Low-level output | S22 to S17 |

3.2 Non-Port Pins

| Pin Name | I/O | Function | After Reset | Alternate Function |
|------------------|--------|---|------------------|--------------------|
| INT | Input | External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified. | Input | P61 |
| KR00 to KR03 | Input | Key return signal detection | Input | P40 to P43 |
| TO40 | Output | 8-bit timer 40 output | Input | P60 |
| SCK10 | I/O | Serial clock input/output of serial interface 10 | Input | P20 |
| SI10 | Input | Serial data input of serial interface 10 | Input | P22 |
| SO10 | Output | Serial data output of serial interface 10 | Input | P21 |
| S0 to S16 | Output | LCD controller/driver segment signal outputs | Low-level output | – |
| S17 to S22 | | | | P85 to P80 |
| S23 | | | | – |
| COM0 to COM3 | Output | LCD controller/driver common signal outputs | Low-level output | – |
| V _{Lco} | – | LCD drive voltage | – | – |
| X1 | Input | Connecting crystal resonator for main system clock oscillation | – | – |
| X2 | – | | – | – |
| XT1 | Input | Connecting crystal resonator for subsystem clock oscillation | – | – |
| XT2 | – | | – | – |
| RESET | Input | System reset input | Input | – |
| V _{BD} | – | Positive power supply | – | – |
| V _{SS} | – | Ground potential | – | – |
| IC0 | – | Internally connected. Connect to V _{SS} directly. | – | – |

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins is shown in Table 3-1.
 For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

| Pin Name | I/O Circuit Type | I/O | Recommend Connection of Unused Pins |
|----------------------|------------------|--------|---|
| P00 to P03 | 5-A | I/O | Input: Independently connect to V _{DD} or V _{SS} via a resistor. Output: Leave open. |
| P10, P11 | | | |
| P20/SCK10 | | | |
| P21/SO10 | | | |
| P22/SI10 | | | |
| P40/KR00 to P43/KR03 | | | |
| P60/TO40 | 5 | | |
| P61/INT | 8 | | Input: Independently connect to V _{SS} via a resistor. Output: Leave open. |
| P80/S22 to P85/S17 | 17-G | | Input: Independently connect to V _{DD} or V _{SS} via a resistor. Output: Leave open. |
| S0 to S16, S23 | 17-D | Output | Leave open. |
| COM0 to COM3 | 18-B | | |
| V _{LCO} | - | - | |
| XT1 | | Input | Connect to V _{SS} . |
| XT2 | | - | Leave open. |
| RESET | 2 | Input | - |
| IC0 | - | - | Connect directly to V _{SS} directly. |

Figure 3-1. I/O Circuit Type (1/2)

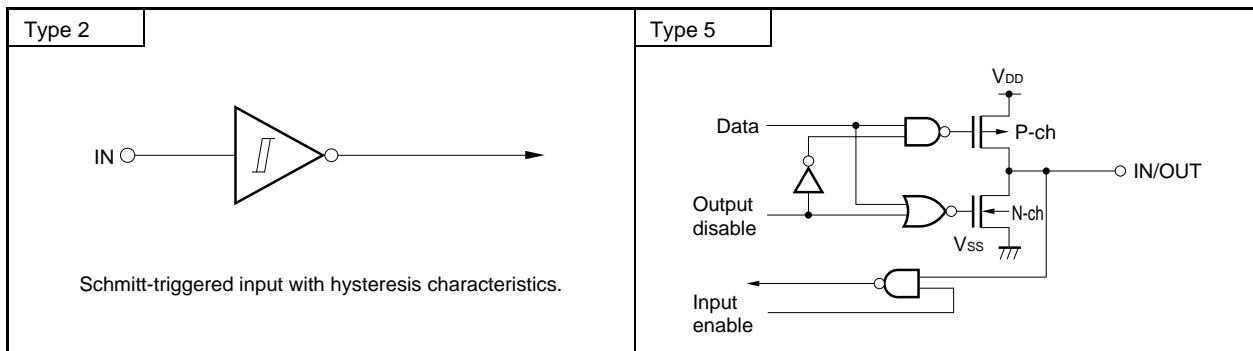
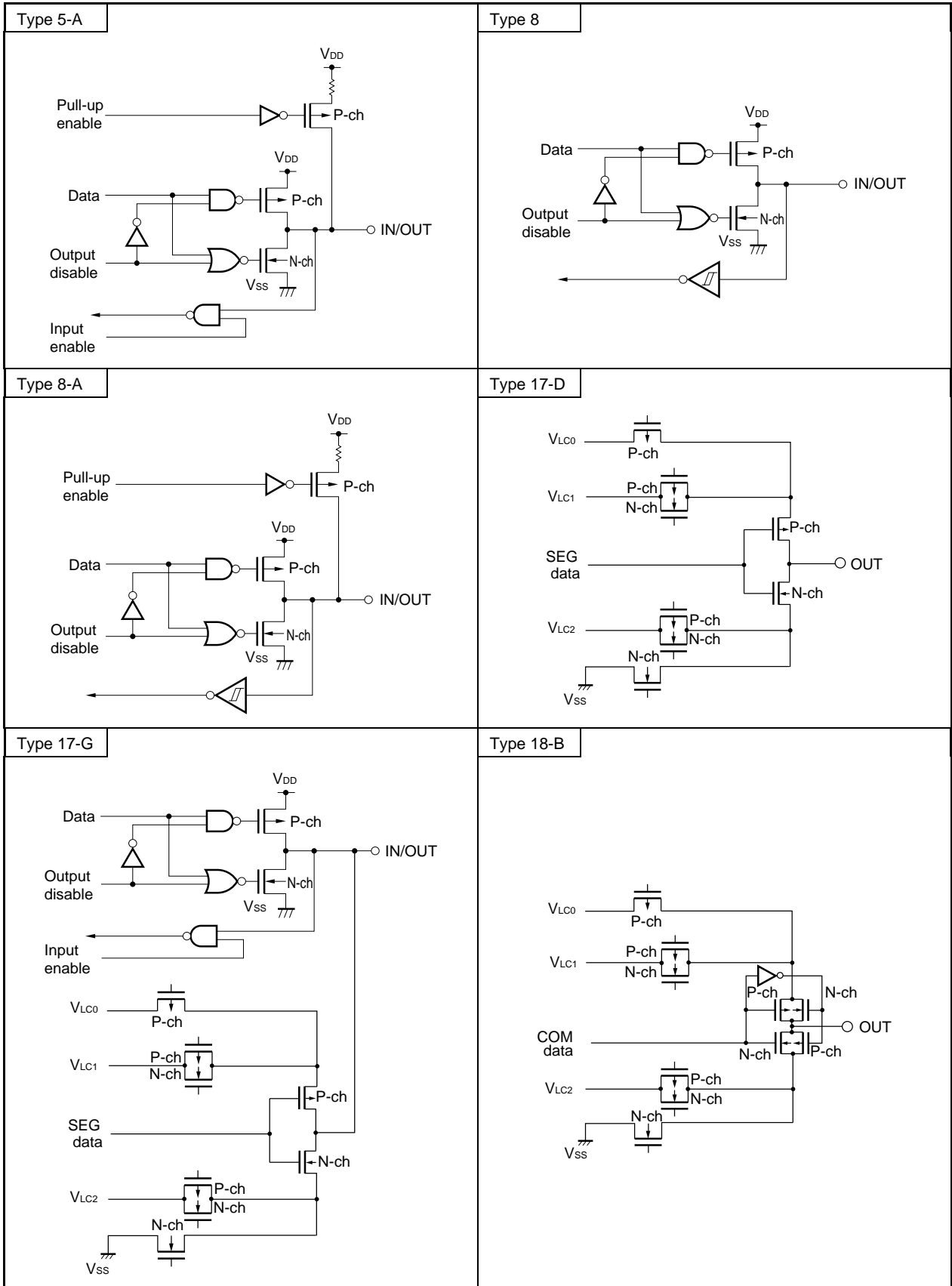


Figure 3-1. I/O Circuit Type (2/2)



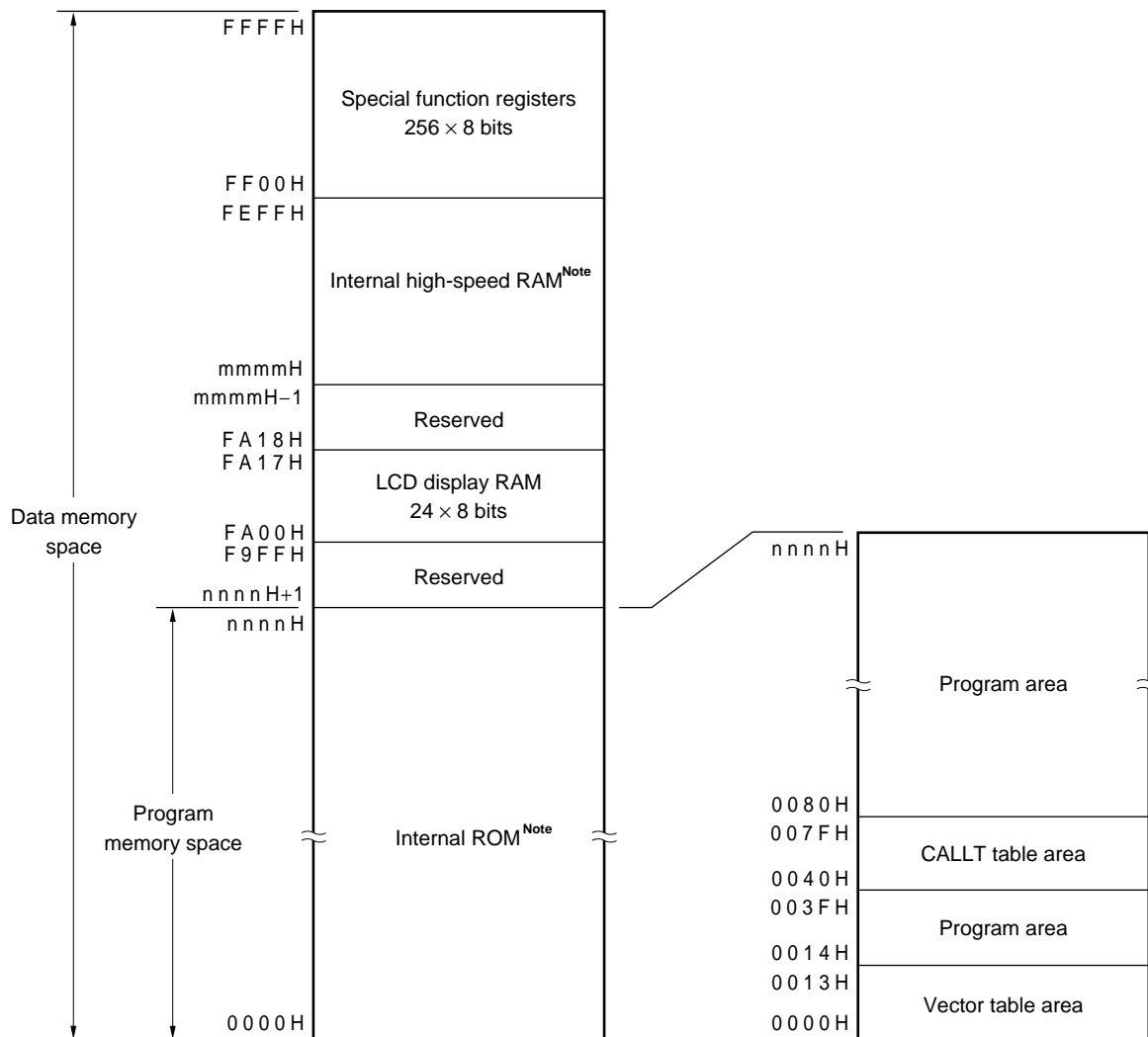
Remark V_{Lc1}: V_{Lc0} × 2/3, V_{Lc2}: V_{Lc0}/3

4. CPU ARCHITECTURE

4.1 Memory Space

The μPD789322, 789324, 789326, and 789327 are provided with 64 Kbytes of accessible memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



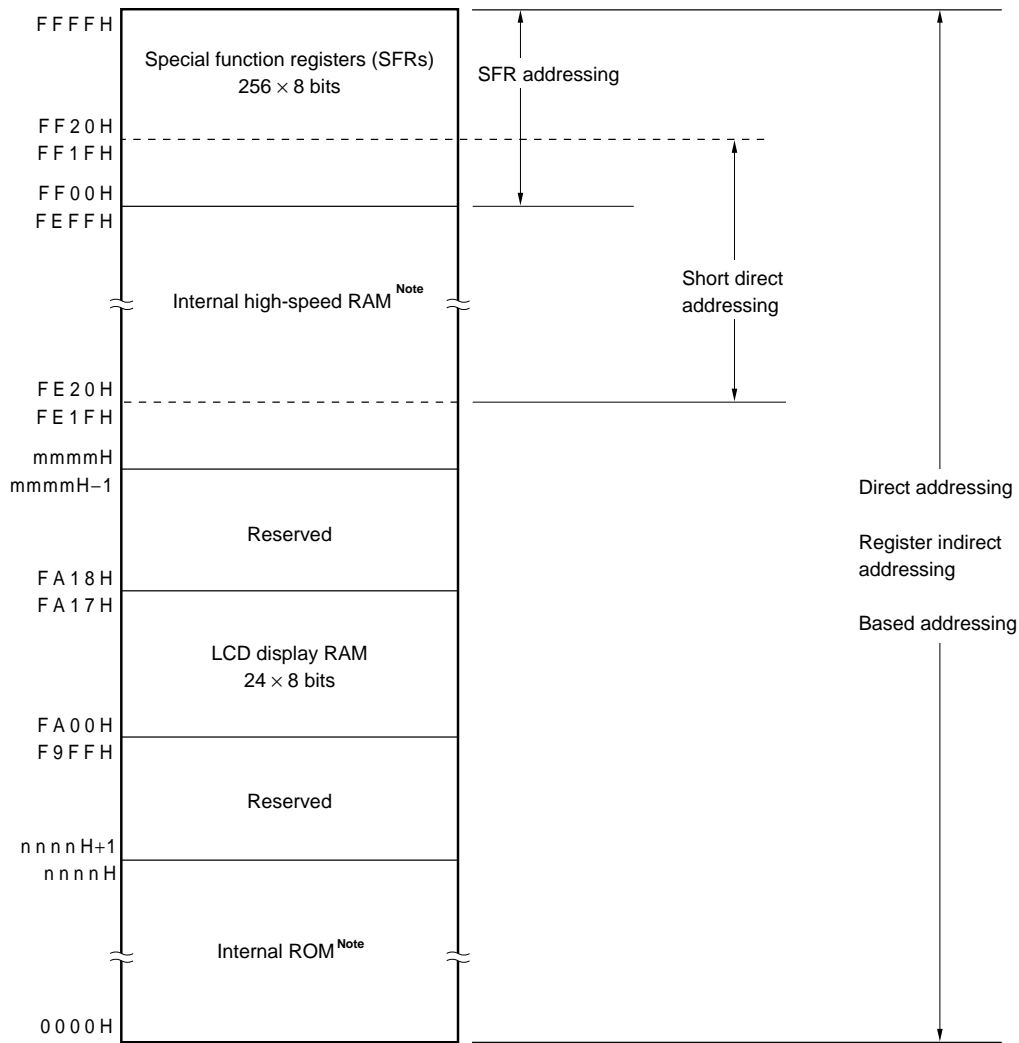
Note The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the next table).

| Relevant Product Name | Internal ROM Last Address nnnnH | Internal High-Speed RAM Start Address mmmH |
|-----------------------|------------------------------------|---|
| μPD789322 | 0FFFH | FE00H |
| μPD789324 | 1FFFH | |
| μPD789326 | 3FFFH | FD00H |
| μPD789327 | 5FFFH | |

4.2 Data Memory Addressing

The μPD789322, 789324, 789326, and 789327 are provided with a variety of addressing modes to improve the operability of the memory. In the area that incorporates data memory (FD00H to FFFFH) in particular, specific addressing modes that correspond to the particular functions of an area, such as the special function registers (SFRs), are available. Figure 4-2 shows the data memory addressing modes.

Figure 4-2. Data Memory Addressing Modes



Note The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the next table).

| Relevant Product Name | Internal ROM Last Address nnnnH | Internal High-Speed RAM Start Address mmmmH |
|-----------------------|------------------------------------|--|
| μPD789322 | 0FFFH | FE00H |
| μPD789324 | 1FFFH | |
| μPD789326 | 3FFFH | FD00H |
| μPD789327 | 5FFFH | |

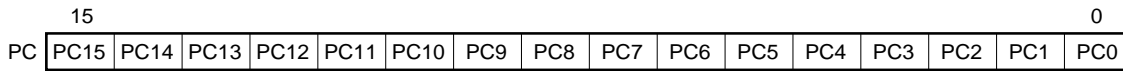
4.3 Processor Registers

4.3.1 Control registers

(1) Program counter (PC)

The PC is a 16-bit register that holds the address information of the next program to be executed.

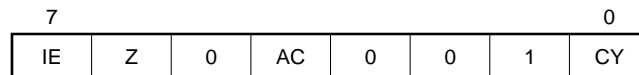
Figure 4-3. Program Counter Configuration



(2) Program status word (PSW)

The PSW is an 8-bit register that indicates the status of the CPU according to the results of instruction execution.

Figure 4-4. Program Status Word Configuration



(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledgement of the CPU.

(b) Zero flag (Z)

This flag is set (1) if the result of an operation is zero; otherwise it is reset (0).

(c) Auxiliary carry flag (AC)

AC is set (1) if the result of the operation has a carry from bit 3 or a borrow at bit 3; otherwise it is reset (0).

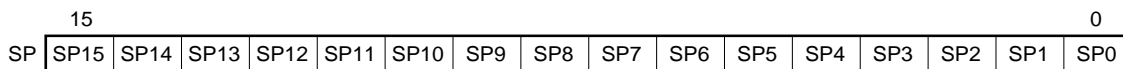
(d) Carry flag (CY)

CY is used to indicate whether an overflow or underflow has occurred during the execution of a subtract or add instruction.

(3) Stack pointer (SP)

The SP is a 16-bit register that holds the start address of the stack area. Only the internal RAM area (FD00H to FEFFH) can be specified as the stack area.

Figure 4-5. Stack Pointer Configuration



Caution $\overline{\text{RESET}}$ input makes the SP contents undefined, so be sure to initialize the SP before instruction execution.

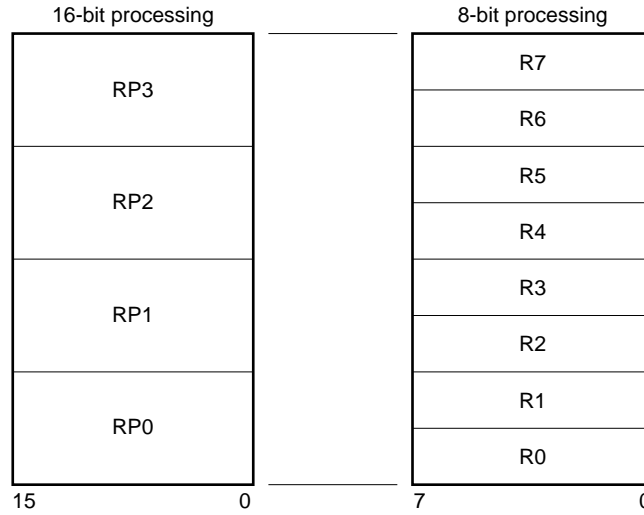
4.3.2 General-purpose registers

The μPD789322, 789324, 789326, and 789327 have eight 8-bit general-purpose registers (X, A, C, B, E, D, L, and H).

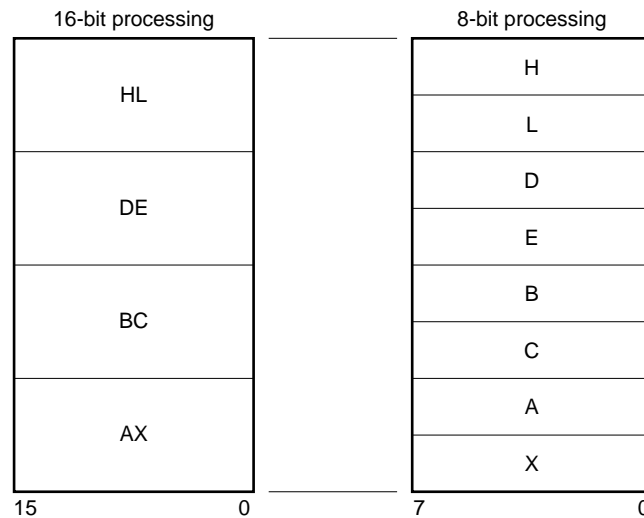
These registers can be used either singly as 8-bit registers or in pairs as 16-bit registers (AX, BC, DE, and HL), and can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Figure 4-6. General-Purpose Register Configuration

(a) Absolute register names



(b) Functional register names



4.3.3 Special function registers (SFRs)

Special function registers are used as peripheral hardware mode registers and control registers, and are mapped in the 256-byte space from FF00H to FFFFH.

Note that the bit number of a bit name that is a reserved word in the RA78K0S and defined under the header file “sfrbit.h” in the CC78K0S appears enclosed in a circle in the register formats. Refer to the register formats in 5.

PERIPHERAL HARDWARE FUNCTIONS.

Table 4-1. Special Function Registers (1/2)

| Address | Special Function Register (SFR) Name | Symbol | R/W | Bit Unit for Manipulation | | | After Reset |
|---------|--|--------|-----|---------------------------|--------|---------------------|-------------|
| | | | | 1 Bit | 8 Bits | 16 Bits | |
| FF00H | Port 0 | P0 | R/W | √ | √ | – | 00H |
| FF01H | Port 1 | P1 | | √ | √ | – | |
| FF02H | Port 2 | P2 | | √ | √ | – | |
| FF03H | port 4 | P4 | | √ | √ | – | |
| FF05H | Port 6 | P6 | | √ | √ | – | |
| FF08H | Port 8 | P8 | | √ | √ | – | |
| FF20H | Port mode register 0 | PM0 | | √ | √ | – | FFH |
| FF21H | Port mode register 1 | PM1 | | √ | √ | – | |
| FF22H | Port mode register 2 | PM2 | | √ | √ | – | |
| FF24H | Port mode register 4 | PM4 | | √ | √ | – | |
| FF26H | Port mode register 6 | PM6 | | √ | √ | – | |
| FF28H | Port mode register 8 | PM8 | | √ | √ | – | |
| FF32H | Pull-up resistor option register B2 | PUB2 | | √ | √ | – | 00H |
| FF4AH | Watch timer mode control register | WTM | | √ | √ | – | |
| FF58H | Port function register 8 | PF8 | √ | √ | – | | |
| FF63H | 8-bit compare register 30 | CR30 | W | – | √ | – | Undefined |
| FF64H | 8-bit timer counter 30 | TM30 | R | – | √ | – | 00H |
| FF65H | 8-bit timer mode control register 30 | TMC30 | R/W | √ | √ | – | |
| FF66H | 8-bit compare register 40 | CR40 | W | – | √ | – | Undefined |
| FF67H | 8-bit H width compare register 40 | CRH40 | | – | √ | – | |
| FF68H | 8-bit timer counter 40 | TM40 | R | – | √ | – | 00H |
| FF69H | 8-bit timer mode control register 40 | TMC40 | R/W | √ | √ | – | |
| FF6AH | Carrier generator output control register 40 | TCA40 | W | – | √ | – | |
| FF72H | Serial operation mode register 10 | CSIM10 | R/W | √ | √ | – | Undefined |
| FF74H | Transmission/reception shift register 10 | SIO10 | | √ | √ | – | |
| FFB0H | LCD display mode register 0 | LCDM0 | | √ | √ | – | |
| FFB2H | LCD clock control register 0 | LCDC0 | √ | √ | – | 00H ^{Note} | |
| FFDDH | Power-on-clear register 1 | POCF1 | √ | √ | – | | |

Note This value is 04H only after a power-on-clear reset.

Table 4-1. Special Function Registers (2/2)

| Address | Special Function Register (SFR) Name | Symbol | R/W | Bit Unit for Manipulation | | | After Reset |
|---------|---|--------|-----|---------------------------|--------|---------|-------------|
| | | | | 1 Bit | 8 Bits | 16 Bits | |
| FFE0H | Interrupt request flag register 0 | IF0 | R/W | √ | √ | – | 00H |
| FFE4H | Interrupt mask flag register 0 | MK0 | | √ | √ | – | FFH |
| FFECH | External interrupt mode register 0 | INTM0 | | – | √ | – | 00H |
| FFF0H | Subclock oscillation mode register | SCKM | | √ | √ | – | |
| FFF2H | Subclock control register | CSS | | √ | √ | – | |
| FFF5H | Key return mode register 00 | KRM00 | | √ | √ | – | |
| FFF7H | Pull-up resistor option register 0 | PU0 | | √ | √ | – | |
| FFF9H | Watchdog timer mode register | WDTM | | √ | √ | – | |
| FFFAH | Oscillation stabilization time selection register | OSTS | | – | √ | – | 04H |
| FFFBH | Processor clock control register | PCC | | √ | √ | – | 02H |

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

5.1.1 Port functions

Various kinds of control operations are possible using the ports provided in the μPD789322, 789324, 789326, and 789327. These ports are illustrated in Figure 5-1 and their functions are listed in Table 5-1.

A number of alternate functions are also provided, except for those ports functioning as digital I/O ports. Refer to **3. PIN FUNCTIONS** for details of the alternate function pins.

Figure 5-1. Ports

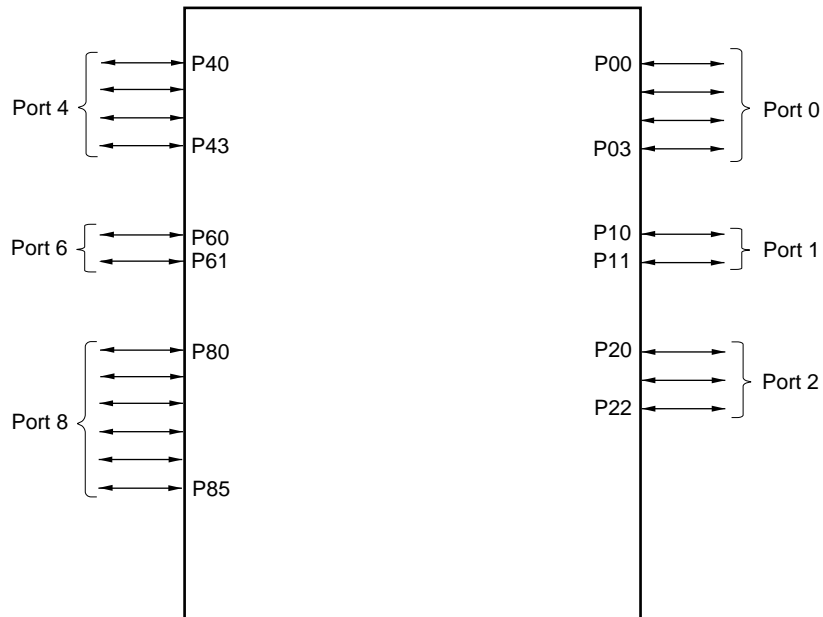


Table 5-1. Port Functions

| Port Name | Pin Name | Function |
|-----------|------------|--|
| Port 0 | P00 to P03 | This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0). |
| Port 1 | P10, P11 | This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0). |
| Port 2 | P20 to P22 | This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register B2 (PUB2). |
| Port 4 | P40 to P43 | This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0), or key return mode register 00 (KRM00). |
| Port 6 | P60, P61 | This is an I/O port for which input and output can be specified in 1-bit units. |
| Port 8 | P80 to P85 | This is an I/O port for which input and output can be specified in 1-bit units. |

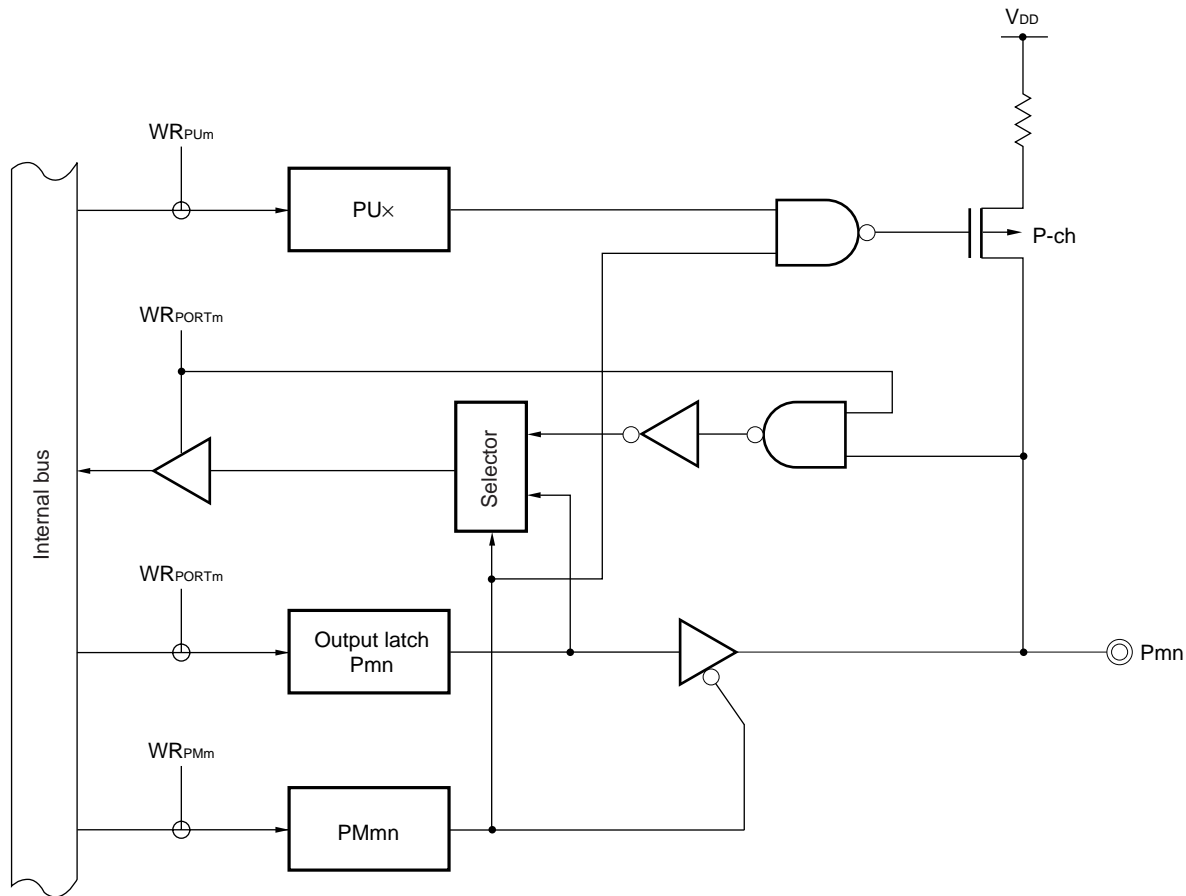
5.1.2 Port configuration

The ports consist of the following hardware.

Table 5-2. Port Configuration

| Item | Configuration |
|-------------------|---|
| Control registers | Port mode registers (PMm: m = 0 to 2, 4, 6, 8) Pull-up resistor option registers (PU0, PUB2) Port function register 8 (PF8) |
| Ports | Total: 21 (CMOS I/O: 21) |
| Pull-up resistors | Total: 13 (software control: 13) |

Figure 5-2. Basic Configuration of CMOS Port



Caution Figure 5-2 shows the basic configuration of a CMOS I/O port. This configuration differs depending on the functions of alternate function pins. Also, an on-chip pull-up resistor can be connected to port 4 by means of a setting in key return mode register 00 (KRM00).

- Remark**
- PU_x: Pull-up resistor option register (x = 0, B2)
 - PM_n: Bit n of port mode register m (m = 0 to 2, 4, 6, 8 n = 0 to 5)
 - P_{mn}: Bit n of port m
 - RD: Port read signal
 - WR: Port write signal

5.1.3 Port function control registers

The ports are controlled by the following three types of registers.

- Port mode registers (PM0 to PM2, PM4, PM6, PM8)
- Pull-up resistor option registers (PU0, PUB2)
- Port function register 8 (PF8)

(1) Port mode registers (PM0 to PM2, PM4, PM6, PM8)

Input and output can be specified in 1-bit units.

These registers can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

When using the port pins as their alternate functions, set the port mode register and the output latch as shown in Table 5-3.

Caution Because P61 functions alternately as an external interrupt input, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) before using the port in output mode.

Figure 5-3. Port Mode Register Format

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|------|------|------|------|------|------|---------|-------------|-----|
| PM0 | 1 | 1 | 1 | 1 | PM03 | PM02 | PM01 | PM00 | FF20H | FFH | R/W |
| PM1 | 1 | 1 | 1 | 1 | 1 | 1 | PM11 | PM10 | FF21H | FFH | R/W |
| PM2 | 1 | 1 | 1 | 1 | 1 | PM22 | PM21 | PM20 | FF22H | FFH | R/W |
| PM4 | 1 | 1 | 1 | 1 | PM43 | PM42 | PM41 | PM40 | FF24H | FFH | R/W |
| PM6 | 1 | 1 | 1 | 1 | 1 | 1 | PM61 | PM60 | FF26H | FFH | R/W |
| PM8 | 1 | 1 | PM85 | PM84 | PM83 | PM82 | PM81 | PM80 | FF28H | FFH | R/W |
| PMmn | Pmn pin input/output mode selection (m = 0 to 2, 4, 6, 8 n = 0 to 5) | | | | | | | | | | |
| 0 | Output mode (output buffer on) | | | | | | | | | | |
| 1 | Input mode (output buffer off) | | | | | | | | | | |

Table 5-3. Port Mode Registers and Output Latch Settings When Using Alternate Functions

| Pin Name | Alternate Function | | PM _{xx} | P _{xx} |
|------------|----------------------------|--------|------------------|-----------------|
| | Name | I/O | | |
| P20 | SCK10 | Input | 1 | × |
| | | Output | 0 | 1 |
| P21 | SO10 | Output | 0 | 1 |
| P22 | SI10 | Input | 1 | × |
| P40 to P43 | KR00 to KR03 | Input | 1 | × |
| P60 | TO40 | Output | 0 | 0 |
| P61 | INT | Input | 1 | × |
| P80 to P85 | S22 to S17 ^{Note} | Output | × | × |

Note When using P80 to P85 pins as S22 to S17, set port function register 8 (PF8) to 3FH.

Remark ×: don't care
 PM_{xx}: Port mode register
 P_{xx}: Port output latch

(2) Pull-up resistor option register 0 (PU0)

This register sets whether to use on-chip pull-up resistors for ports 0, 1, and 4 on a port by port basis. An on-chip pull-up resistor can be used only for those bits set to the input mode of a port for which the use of the on-chip pull-up resistor has been specified using PU0.

For those bits set to the output mode, on-chip pull-up resistors cannot be used, regardless of the setting of PU0. This also applies to alternate-function pins used as output pins.

PU0 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-4. Format of Pull-Up Resistor Option Register 0

| | | | | | | | | | | | |
|--------|---|---|---|------|---|---|------|------|---------|-------------|-----|
| Symbol | 7 | 6 | 5 | <4> | 3 | 2 | <1> | <0> | Address | After reset | R/W |
| PU0 | 0 | 0 | 0 | PU04 | 0 | 0 | PU01 | PU00 | FFF7H | 00H | R/W |

| | |
|------------------|--|
| PU0 _m | Port m on-chip pull-up resistor selection (m = 0, 1, 4) |
| 0 | An on-chip pull-up resistor is not connected |
| 1 | An on-chip pull-up resistor is connected |

Caution Always set bits 2, 3, and 5 to 7 to 0.

(3) Pull-up resistor option register B2 (PUB2)

This register sets whether to use on-chip pull-up resistors for P20 to P22 in bit units. An on-chip pull-up resistor can be used only for those bits set to the input mode of a port for which the use of the on-chip pull-up resistor has been specified using PUB2.

For those bits set to the output mode, on-chip pull-up resistors cannot be used, regardless of the setting of PUB2. This also applies to alternate-function pins used as output pins.

PUB2 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-5. Format of Pull-Up Resistor Option Register B2

| Symbol | 7 | 6 | 5 | 4 | 3 | <2> | <1> | <0> | Address | After reset | R/W |
|--------|---|---|---|---|---|-------|-------|-------|---------|-------------|-----|
| PUB2 | 0 | 0 | 0 | 0 | 0 | PUB22 | PUB21 | PUB20 | FF32H | 00H | R/W |

| PUB2n | P2n on-chip pull-up resistor selection (n = 0 to 2) |
|-------|--|
| 0 | An on-chip pull-up resistor is not connected |
| 1 | An on-chip pull-up resistor is connected |

Caution Always set bits 3 to 7 to 0.

(4) Port function register 8 (PF8)

This register sets the port function of port 8 in 1-bit units.

The pins of port 8 are selected as either LCD segment signal outputs or general-purpose port pins according to the setting of PF8.

PF8 can be set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-6. Format of Port Function Register 8

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|------|------|------|------|------|------|---------|-------------|-----|
| PF8 | 0 | 0 | PF85 | PF84 | PF83 | PF82 | PF81 | PF80 | FF58H | 00H | R/W |

| PF8n | P8n port function (n = 0 to 5) |
|------|--|
| 0 | Operates as a general-purpose port |
| 1 | Operates as an LCD segment signal output |

5.2 Clock Generator

5.2.1 Clock generator function

The clock generator generates the clock pulse to be supplied to the CPU and peripheral hardware.

There are two types of system clock oscillators:

- Main system clock oscillator (ceramic/crystal resonator)
This circuit generates a frequency of 1.0 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction or by means of a processor clock control register (PCC) setting.
- Subsystem clock oscillator
This circuit generates a frequency of 32.768 kHz. Oscillation can be stopped using the subclock oscillation mode register (SCKM).

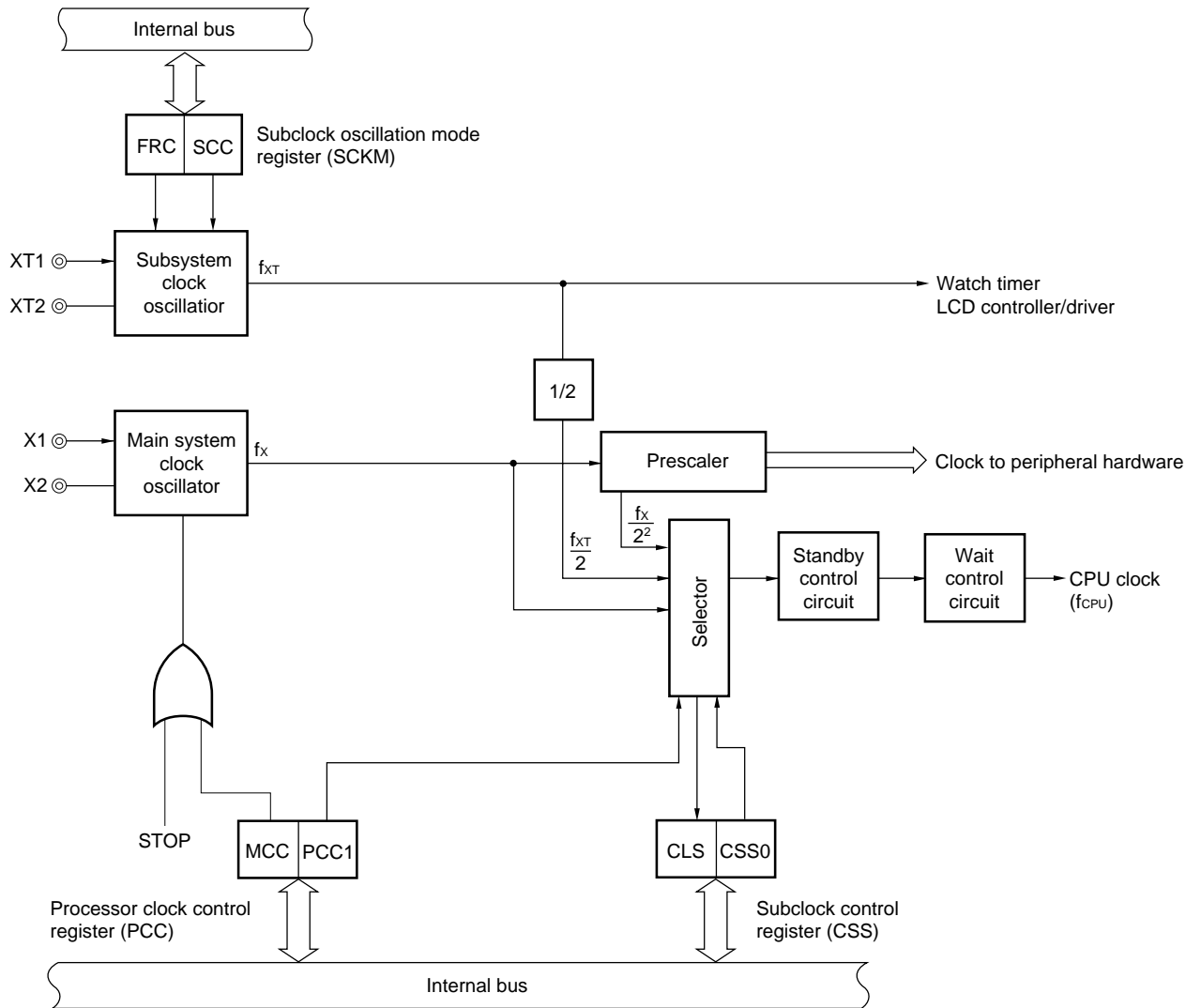
5.2.2 Clock generator configuration

The clock generator consists of the following hardware.

Table 5-4. Clock Generator Configuration

| Item | Configuration |
|-------------------|--|
| Control registers | Processor clock control register (PCC) Subclock oscillation mode register (SCKM) Subclock control register (CSS) |
| Oscillators | Main system clock oscillator Subsystem clock oscillator |

Figure 5-7. Clock Generator Block Diagram



5.2.3 Clock generator control registers

The clock generator is controlled by the following three registers.

- Processor clock control register (PCC)
- Subclock oscillation mode register (SCKM)
- Subclock control register (CSS)

(1) Processor clock control register (PCC)

This register is used to select the CPU clock and set the frequency division ratio.

PCC is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 02H.

Figure 5-8. Format of Processor Clock Control Register

| | | | | | | | | | | | |
|--------|-----|---|---|---|---|---|------|---|---------|-------------|-----|
| Symbol | <7> | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
| PCC | MCC | 0 | 0 | 0 | 0 | 0 | PCC1 | 0 | FFFBH | 02H | R/W |

| | |
|-----|--|
| MCC | Main system clock oscillator operation control |
| 0 | Operation enabled |
| 1 | Operation stopped |

| CSS0 | PCC1 | CPU clock (f _{cpu}) selection ^{Note} | Minimum instruction execution time: 2f _{cpu} |
|------|------|---|---|
| 0 | 0 | f _x (0.2 μs) | 0.4 μs |
| 0 | 1 | f _x /2 ² (0.8 μs) | 1.6 μs |
| 1 | x | f _{XT} /2 (61 μs) | 122 μs |

Note The CPU clock is selected by a combination of flag settings in the PCC and CSS registers. (Refer to 5.2.3 (3) Subclock control register (CSS).)

- Cautions**
1. Always set bits 0 and 2 to 6 to 0.
 2. MCC can be set only when the subsystem clock is selected as the CPU clock. Setting MCC to 1 while the main system clock is operating is invalid.

- Remarks**
1. f_x: Main system clock oscillation frequency
 2. f_{XT}: Subsystem clock oscillation frequency
 3. The parenthesized values apply to operation at f_x = 5.0 MHz or f_{XT} = 32.768 kHz.

(2) Subclock oscillation mode register (SCKM)

This register is used to select a feedback resistor for the subsystem clock and control the oscillation of the clock.

SCKM is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-9. Format of Subclock Oscillation Mode Register

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | <0> | Address | After reset | R/W |
|--------|---|---|---|---|---|---|-----|-----|---------|-------------|-----|
| SCKM | 0 | 0 | 0 | 0 | 0 | 0 | FRC | SCC | FFF0H | 00H | R/W |

| FRC | Feedback resistor selection |
|-----|--|
| 0 | An on-chip feedback resistor is used |
| 1 | An on-chip feedback resistor is not used |

| SCC | Control of subsystem clock oscillator operation |
|-----|---|
| 0 | Operation enabled |
| 1 | Operation stopped |

Caution Always set bits 2 to 7 to 0.

(3) Subclock control register (CSS)

This register is used to specify whether the main system or subsystem clock oscillator is selected and to indicate the operating status of the CPU clock.

CSS is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-10. Format of Subclock Control Register

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|-----|------|---|---|---|---|---------|-------------|---------------------|
| CSS | 0 | 0 | CLS | CSS0 | 0 | 0 | 0 | 0 | FFF2H | 00H | R/W ^{Note} |

| CLS | CPU clock operating status |
|-----|--|
| 0 | Operating on the output of the (divided) main system clock |
| 1 | Operating on the output of the subsystem clock |

| CSS0 | Selection of main system clock or subsystem clock oscillator |
|------|--|
| 0 | Main system clock oscillator (divided) output |
| 1 | Subsystem clock oscillator output |

Note Bit 5 is read-only.

Caution Always set bits 0 to 3, 6, and 7 to 0.

5.3 8-Bit Timer 30, 40

5.3.1 Functions of 8-bit timer 30, 40

The 8-bit timer in the μPD789322, 789324, 789326, and 789327 have 2 channels (timer 30 and timer 40). The operation modes in the following table are possible by means of mode register settings.

Table 5-5. List of Modes

| Mode \ Channel | Timer 30 | Timer 40 |
|---|----------|----------|
| 8-bit timer counter mode (discrete mode) | √ | √ |
| 16-bit timer counter mode (cascade connection mode) | √ | |
| Carrier generator mode | √ | |
| PWM output mode | – | √ |

(1) 8-bit timer counter mode (discrete mode)

The timer can be used for the following functions in this mode.

- 8-bit resolution interval timer
- 8-bit resolution square wave output (timer 40 only)

(2) 16-bit timer counter mode (cascade connection mode)

These timers can be used for 16-bit timer operations via a cascade connection. The timer can be used for the following functions in this mode.

- 16-bit resolution interval timer
- 16-bit resolution square wave output

(3) Carrier generator mode

In this mode the carrier clock generated by timer 40 is output in the cycle set by timer 30.

(4) PWM output mode

In this mode, a pulse with an arbitrary duty ratio, which is set by timer 40, is output.

5.3.2 Configuration of 8-bit timer 30, 40

8-bit timers 30 and 40 consist of the following hardware.

Table 5-6. Configuration of 8-Bit Timer 30, 40

| Item | Configuration |
|-------------------|--|
| Timer counter | 8 bits \times 2 (TM30, TM40) |
| Registers | Compare registers: 8 bits \times 3 (CR30, CR40, CRH40) |
| Timer outputs | 1 (TO40) |
| Control registers | 8-bit timer mode control register 30 (TMC30) 8-bit timer mode control register 40 (TMC40) Carrier generator output control register 40 (TCA40) Port mode register 6 (PM6) |

Figure 5-11. Block Diagram of Timer 30

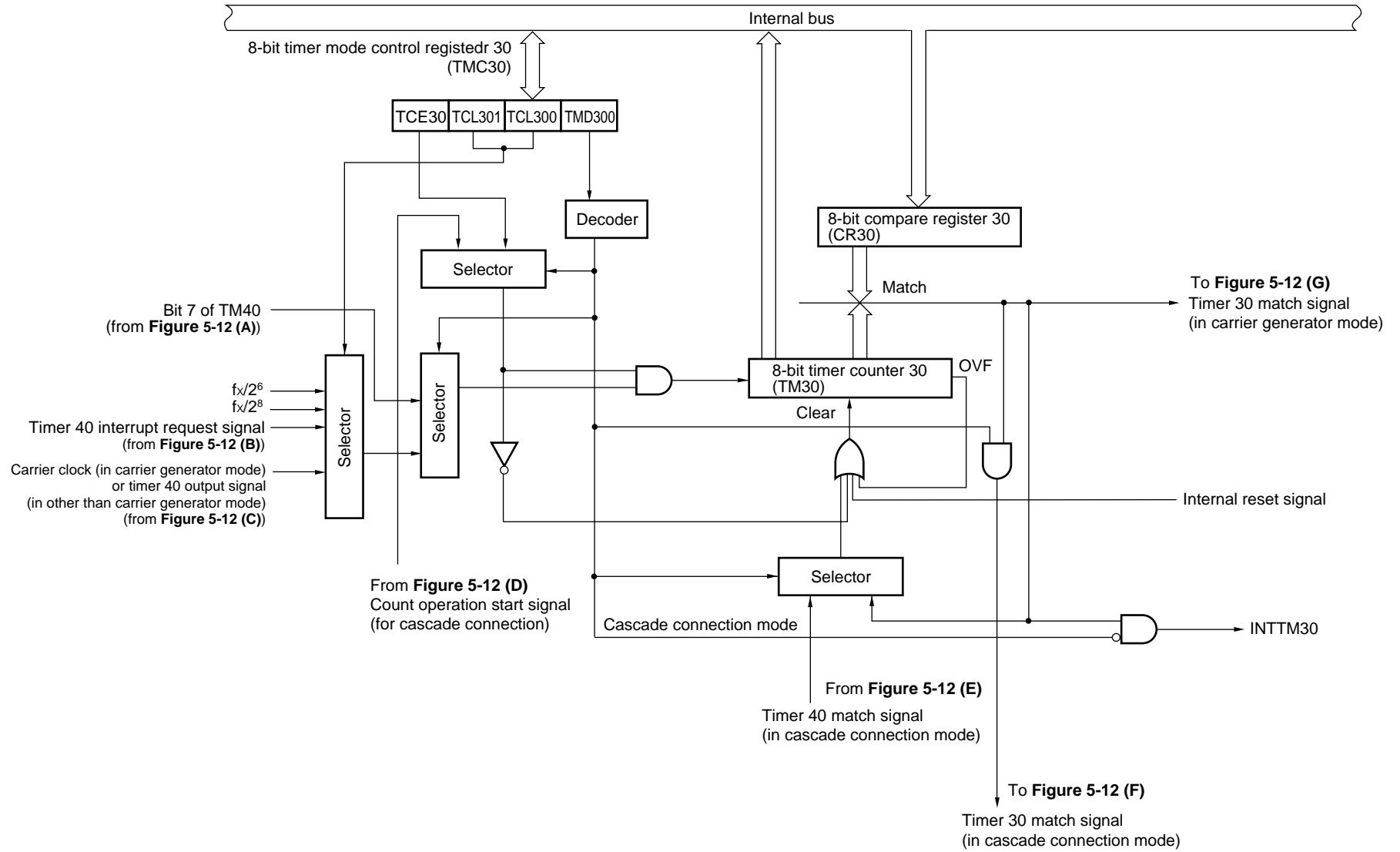
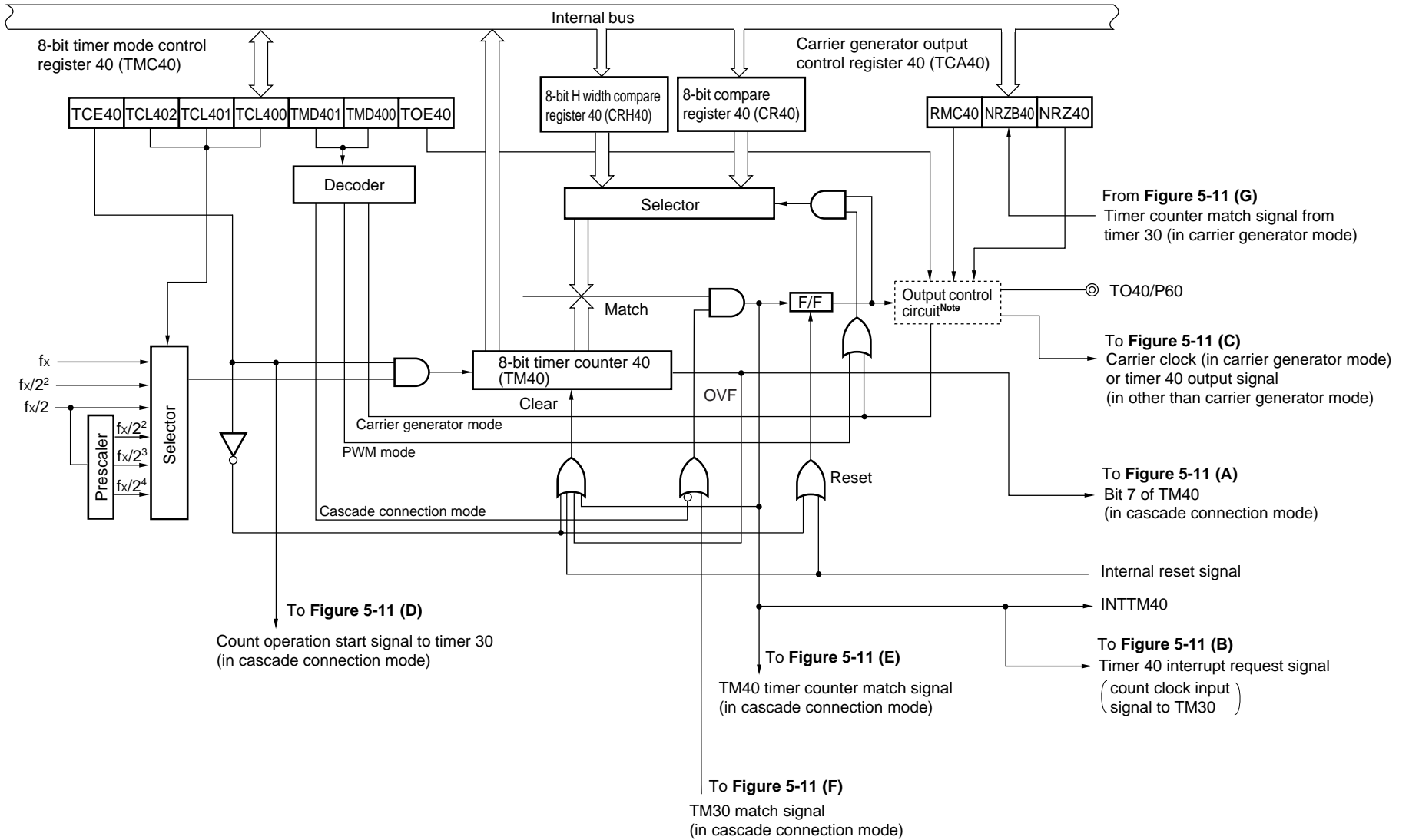
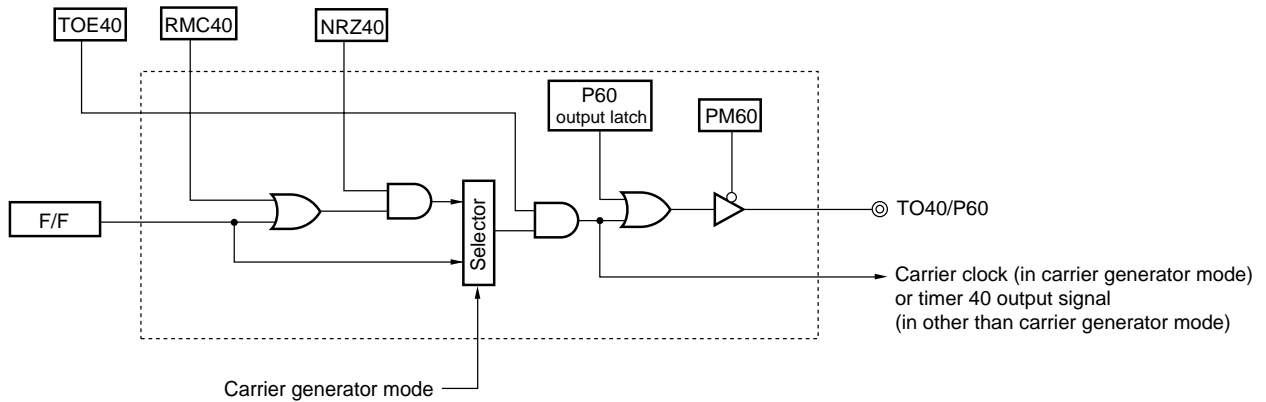


Figure 5-12. Block Diagram of Timer 40



Note Refer to Figure 5-13 for details.

Figure 5-13. Block Diagram of Output Control Circuit (Timer 40)



(1) 8-bit compare register 30 (CR30)

A value specified in CR30 is compared with the count value in 8-bit timer counter 30 (TM30), and if they match, an interrupt request (INTTM30) is generated.

CR30 is set using an 8-bit memory manipulation instruction.

RESET input makes this register undefined.

Caution CR30 cannot be used in carrier generator mode or PWM output mode.

(2) 8-bit compare register 40 (CR40)

A value specified in CR40 is compared with the count value in 8-bit timer counter 40 (TM40), and if they match, an interrupt request (INTTM40) is generated. When operating as a 16-bit timer in cascade connection with TM30, an interrupt request (INTTM40) is only generated if both CR30 and TM30, and CR40 and TM40 match simultaneously (INTTM30 is not issued).

CR40 is set using an 8-bit memory manipulation instruction.

RESET input makes this register undefined.

(3) 8-bit H width compare register (CRH40)

In carrier generator mode or PWM output mode, a timer output high-level width can be set by writing a value to CRH40.

CRH40 is set using an 8-bit memory manipulation instruction.

RESET input makes this register undefined.

(4) 8-bit timer counter 30, 40 (TM30, TM40)

This is an 8-bit register for counting the count pulses.

TM30 and TM40 can be read with a 1-bit or 8-bit memory manipulation instruction.

RESET input sets these registers to 00H.

The conditions under which TM30 and TM40 are cleared to 00H are listed below.

(a) Discrete mode**(i) TM30**

- Upon a reset
- When TCE30 (bit 7 of 8-bit timer mode control register 30 (TMC30)) is cleared to 0
- Upon a match between TM30 and CR30
- If the TM30 count value overflows

(ii) TM40

- Upon a reset
- When TCE40 (bit 7 of 8-bit timer mode control register 40 (TMC40)) is cleared to 0
- Upon a match between TM40 and CR40
- If the TM40 count value overflows

(b) Cascade connection mode (TM30 and TM40 cleared to 00H simultaneously)

- Upon a reset
- When the TCE40 flag is cleared to 0
- Upon a simultaneous match between TM30 and CR30, and TM40 and CR40
- If the TM30 and TM40 count values overflow simultaneously

(c) Carrier generator/PWM output mode (TM40 only)

- Upon a reset
- When the TCE40 flag is cleared to 0
- Upon a match between TM40 and CR40
- Upon a match between TM40 and CRH40
- If the TM40 count value overflows

5.3.3 8-bit timer 30, 40 control registers

8-bit timers 30 and 40 are controlled by the following 4 registers.

- 8-bit timer mode control register 30 (TMC30)
- 8-bit timer mode control register 40 (TMC40)
- Carrier generator output control register 40 (TCA40)
- Port mode register 6 (PM6)

(1) 8-bit timer mode control register 30 (TMC30)

This register is used to control the timer 30 count clock and operation mode settings.
 TMC30 is set using a 1-bit or 8-bit memory manipulation instruction.
 RESET input sets this register to 00H.

Figure 5-14. Format of 8-Bit Timer Mode Control Register 30

| Symbol | <7> | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|-------|---|---|--------|--------|---|--------|---|---------|-------------|-----|
| TMC30 | TCE30 | 0 | 0 | TCL301 | TCL300 | 0 | TMD300 | 0 | FF65H | 00H | R/W |

| TCE30 | TM30 count control operation ^{Note 1} |
|-------|--|
| 0 | TM30 count value cleared and operation stopped |
| 1 | Count operation starts |

| TCL301 | TCL300 | Timer 30 count clock selection |
|--------|--------|--|
| 0 | 0 | $f_x/2^5$ (78.1 kHz) |
| 0 | 1 | $f_x/2^8$ (19.5 kHz) |
| 1 | 0 | Timer 40 match signal |
| 1 | 1 | Carrier clock (in carrier generator mode) or timer 40 output signal (in other than carrier generator mode) |

| TMD300 | TMD401 | TMD400 | Timer 30, timer 40 operation mode selection ^{Note 2} |
|------------------|--------|--------|---|
| 0 | 0 | 0 | Discrete mode |
| 1 | 0 | 1 | Cascade connection mode |
| 0 | 1 | 1 | Carrier generator mode |
| 0 | 1 | 0 | PWM output mode |
| Other than above | | | Setting prohibited |

Notes 1. The TCE30 setting will be ignored in cascade mode because in this case the count operation is controlled by TCE40 (bit 7 of TMC40).

2. The operation mode selection is made using a combination of TMC30 and TMC40 register settings.

Caution In cascade connection mode, the timer 40 output signal is forcibly selected for the count clock.

Remarks **1.** f_x : Main system clock oscillation frequency
2. The parenthesized values apply to operation at $f_x = 5.0$ MHz

(2) 8-bit timer mode control register 40 (TMC40)

This register is used to control the timer 40 count clock and operation mode settings.

TMC40 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-15. Format of 8-Bit Timer Mode Control Register 40

| Symbol | <7> | 6 | 5 | 4 | 3 | 2 | 1 | <0> | Address | After reset | R/W |
|--------|-------|---|--------|--------|--------|--------|--------|-------|---------|-------------|-----|
| TMC40 | TCE40 | 0 | TCL402 | TCL401 | TCL400 | TMD401 | TMD400 | TOE40 | FF69H | 00H | R/W |

| TCE40 | TM40 count control operation ^{Note 1} |
|-------|--|
| 0 | TM40 count value cleared and operation stopped (in cascade connection mode, the count value of TM30 is cleared at the same time) |
| 1 | Count operation starts (in cascade connection mode, the count operation of TM30 starts at the same time) |

| TCL402 | TCL401 | TCL400 | Timer 40 count clock selection |
|------------------|--------|--------|--------------------------------|
| 0 | 0 | 0 | f_x (5 MHz) |
| 0 | 0 | 1 | $f_x/2^2$ (1.25 MHz) |
| 0 | 1 | 0 | $f_x/2$ (2.5 MHz) |
| 0 | 1 | 1 | $f_x/2^2$ (1.25 MHz) |
| 1 | 0 | 0 | $f_x/2^3$ (625 kHz) |
| 1 | 0 | 1 | $f_x/2^4$ (313 kHz) |
| Other than above | | | Setting prohibited |

| TMD300 | TMD401 | TMD400 | Timer 30, timer 40 operation mode selection ^{Note 2} |
|------------------|--------|--------|---|
| 0 | 0 | 0 | Discrete mode |
| 1 | 0 | 1 | Cascade connection mode |
| 0 | 1 | 1 | Carrier generator mode |
| 0 | 1 | 0 | PWM output mode |
| Other than above | | | Setting prohibited |

| TOE40 | Timer output control |
|-------|-----------------------------|
| 0 | Output disabled (port mode) |
| 1 | Output enabled |

Notes 1. The TCE30 setting will be ignored in cascade mode because in this case the count operation is controlled by TCE40 (bit 7 of TMC40).

2. The operation mode selection is made using a combination of TMC30 and TMC40 register settings.

Remarks 1. f_x : Main system clock oscillation frequency

2. The parenthesized values apply to operation at $f_x = 5.0$ MHz

(3) Carrier generator output control register 40 (TCA40)

This register is used to set the timer output data in the carrier generator mode.
 TCA40 is set using a 1-bit or 8-bit memory manipulation instruction.
 RESET input sets this register to 00H.

Figure 5-16. Format of Carrier Generator Output Control Register 40

| Symbol | 7 | 6 | 5 | 4 | 3 | <2> | <1> | <0> | Address | After reset | R/W |
|--------|---|---|---|---|---|-------|--------|-------|---------|-------------|-----|
| TCA40 | 0 | 0 | 0 | 0 | 0 | RMC40 | NRZB40 | NRZ40 | FF6AH | 00H | W |

| | |
|-------|---|
| RMC40 | Remote controller output control |
| 0 | When NRZ40 = 1, a carrier pulse is output to the TO40/P60 pin |
| 1 | When NRZ40 = 1, a high level is output to the TO40/P60 pin |

| | |
|--------|--|
| NRZB40 | This bit stores the data that NRZ40 will output next. Data is transferred to NRZ40 upon the generation of a timer 30 match signal. |
|--------|--|

| | |
|-------|--|
| NRZ40 | No return, zero data |
| 0 | A low level is output (the carrier clock is stopped) |
| 1 | A carrier pulse is output |

Caution TCA40 cannot be set with a 1-bit memory manipulation instruction.
 Be sure to set it with an 8-bit memory manipulation instruction.

(4) Port mode register 6 (PM6)

This register is used to set port 6 to input or output in 1-bit units.
 When the TO40/P60 pin is used as a timer output, set the PM60 and P60 output latches to 0.
 PM6 is set using a 1-bit or 8-bit memory manipulation instruction.
 RESET input sets this register to FFH.

Figure 5-17. Format of Port Mode Register 6

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|---|---|---|---|------|------|---------|-------------|-----|
| PM6 | 1 | 1 | 1 | 1 | 1 | 1 | PM61 | PM60 | FF26H | FFH | R/W |

| | |
|------|---|
| PM6n | Input/output mode of pin P6n (n = 0, 1) |
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

5.4 Watch Timer

5.4.1 Watch timer functions

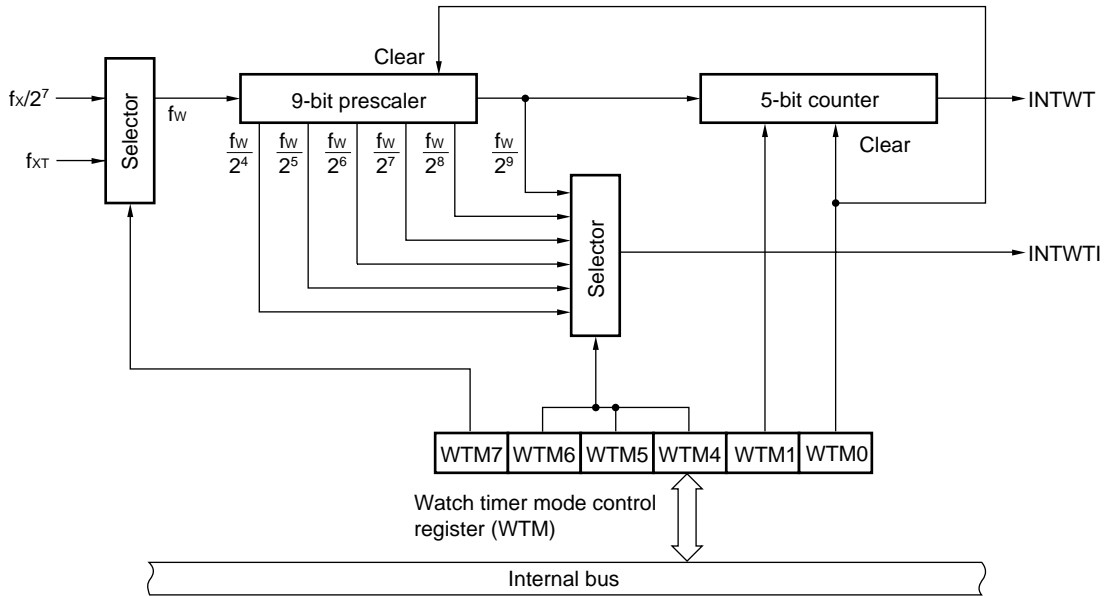
The watch timer has the following functions.

- Watch timer
- Interval timer

The watch and interval timers can be used at the same time.

Figure 5-18 shows a block diagram of the watch timer.

Figure 5-18. Watch Timer Block Diagram



(1) Watch timer

An interrupt request (INTWT) is generated at 0.5-second intervals using the 4.19-MHz main system clock or 32.768-kHz subsystem clock.

Caution When the main system clock is operating at 5.0 MHz, it cannot be used to generate a 0.5-second interval. In this case, the subsystem clock, which operates at 32.768 kHz, should be used instead.

(2) Interval timer

The interval timer is used to generate an interrupt request (INTWTI) at preset intervals.

Table 5-7. Interval Time of Interval Timer

| Interval Time | At $f_x = 5.0$ MHz Operation | At $f_x = 4.19$ MHz Operation | At $f_{XT} = 32.768$ kHz Operation |
|--------------------|------------------------------|-------------------------------|------------------------------------|
| $2^4 \times 1/f_w$ | 409.6 μs | 488 μs | 488 μs |
| $2^5 \times 1/f_w$ | 819.2 μs | 977 μs | 977 μs |
| $2^6 \times 1/f_w$ | 1.64 ms | 1.95 ms | 1.95 ms |
| $2^7 \times 1/f_w$ | 3.28 ms | 3.91 ms | 3.91 ms |
| $2^8 \times 1/f_w$ | 6.55 ms | 7.81 ms | 7.81 ms |
| $2^9 \times 1/f_w$ | 13.1 ms | 15.6 ms | 15.6 ms |

- Remarks**
1. f_w : Watch timer clock frequency ($f_x/2^7$ or f_{XT})
 2. f_x : Main system clock oscillation frequency
 3. f_{XT} : Subsystem clock oscillation frequency

5.4.2 Watch timer configuration

The watch timer consists of the following hardware.

Table 5-8. Watch Timer Configuration

| Item | Configuration |
|------------------|---|
| Counter | 5 bits × 1 |
| Prescaler | 9 bits × 1 |
| Control register | Watch timer mode control register (WTM) |

5.4.3 Watch timer control register

The following register controls the watch timer.

- Watch timer mode control register (WTM)

(1) Watch timer mode control register (WTM)

This register is used to enable/disable the count clock and operation of the watch timer and set the interval time of the prescaler and operation control of the 5-bit counter.

WTM is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-19. Format of Watch Timer Mode Control Register

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | <1> | <0> | Address | After reset | R/W |
|--------|------|------|------|------|---|---|------|------|---------|-------------|-----|
| WTM | WTM7 | WTM6 | WTM5 | WTM4 | 0 | 0 | WTM1 | WTM0 | FF4AH | 00H | R/W |

| WTM7 | Watch timer count clock (fw) selection |
|------|--|
| 0 | $f_x/2^7$ (39.1 kHz) |
| 1 | f_{XT} (32.768 kHz) |

| WTM6 | WTM5 | WTM4 | Prescaler interval time selection |
|------------------|------|------|-----------------------------------|
| 0 | 0 | 0 | $2^4/f_w$ |
| 0 | 0 | 1 | $2^5/f_w$ |
| 0 | 1 | 0 | $2^6/f_w$ |
| 0 | 1 | 1 | $2^7/f_w$ |
| 1 | 0 | 0 | $2^8/f_w$ |
| 1 | 0 | 1 | $2^9/f_w$ |
| Other than above | | | Setting prohibited |

| WTM1 | 5-bit counter operation control |
|------|---------------------------------|
| 0 | Cleared after operation stopped |
| 1 | Start |

| WTM0 | Watch timer operation enable |
|------|--|
| 0 | Operation stopped (both prescaler and timer cleared) |
| 1 | Operation enabled |

- Remarks**
1. f_w : Watch timer clock frequency ($f_x/2^7$ or f_{XT})
 2. f_x : Main system clock oscillation frequency
 3. f_{XT} : Subsystem clock oscillation frequency
 4. The parenthesized values apply to operation at $f_x = 5.0$ MHz or $f_{XT} = 32.768$ kHz.

5.5 Watchdog Timer

5.5.1 Watchdog timer functions

The watchdog timer has the following functions.

(1) Watchdog timer

The watchdog timer is used to detect a program runaway. If a runaway is detected, either a non-maskable interrupt or the $\overline{\text{RESET}}$ signal can be generated.

(2) Interval timer

The interval timer is used to generate interrupts at preset intervals.

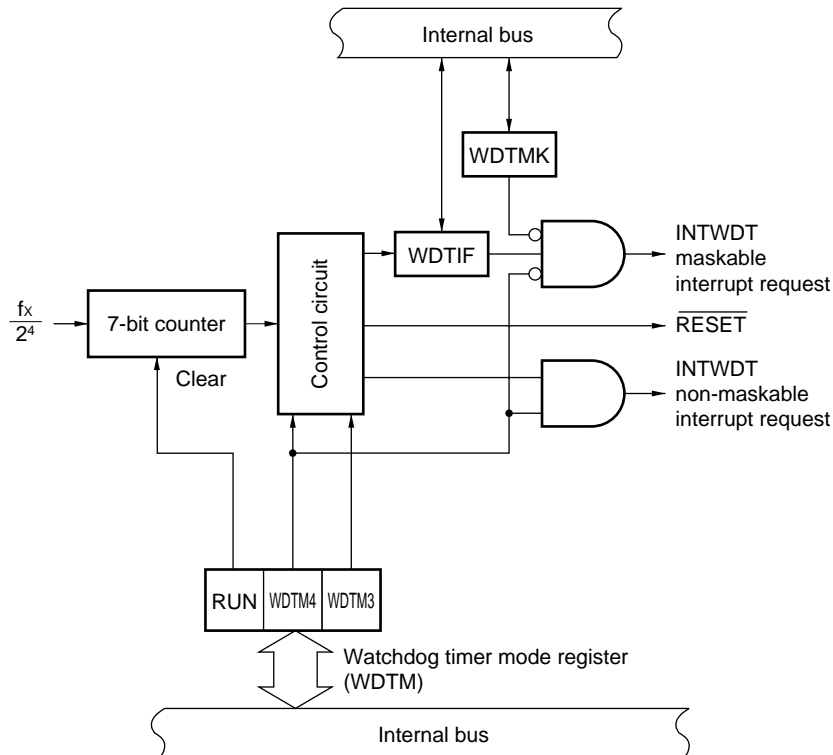
5.5.2 Watchdog timer configuration

The watchdog timer consists of the following hardware.

Table 5-9. Watchdog Timer Configuration

| Item | Configuration |
|------------------|-------------------------------------|
| Control register | Watchdog timer mode register (WDTM) |

Figure 5-20. Watchdog Timer Block Diagram



5.5.3 Watchdog timer control register

The watchdog timer is controlled by the following register.

- Watchdog timer mode register (WDTM)

(1) Watchdog timer mode register (WDTM)

This register is used to set the watchdog timer operation mode and whether to enable or disable counting.

WDTM is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-21. Format of Watchdog Timer Mode Register

| Symbol | <7> | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|-----|---|---|-------|-------|---|---|---|---------|-------------|-----|
| WDTM | RUN | 0 | 0 | WDTM4 | WDTM3 | 0 | 0 | 0 | FFF9H | 00H | R/W |

| RUN | Watchdog timer operation selection ^{Note 1} |
|-----|--|
| 0 | Counting stopped |
| 1 | Counter cleared and counting starts |

| WDTM4 | WDTM3 | Watchdog timer operation mode selection ^{Note 2} |
|-------|-------|--|
| 0 | 0 | Operation stopped |
| 0 | 1 | Interval timer mode (when an overflow occurs, a maskable interrupt is generated) ^{Note 3} |
| 1 | 0 | Watchdog timer mode 1 (when an overflow occurs, a non-maskable interrupt is generated) |
| 1 | 1 | Watchdog timer mode 2 (when an overflow occurs, a reset operation is activated) |

- Notes**
1. Once the RUN bit has been set (1), it is impossible to clear it (0) by software. Consequently, once counting begins, it cannot be stopped by any means other than $\overline{\text{RESET}}$ input.
 2. Once WDTM3 and WDTM4 have been set (1), it is impossible to clear them (0) by software.
 3. The interval timer starts operating as soon as the RUN bit is set to 1.

- Cautions**
1. When the RUN bit is set to 1, and the watchdog timer is cleared, the actual overflow time will be up to 0.8% shorter than the time specified by the watchdog timer clock selection register.
 2. To use watchdog timer mode 1 or 2, be sure to set WDTM4 to 1 after confirming that WDTIF (bit 0 of interrupt request flag 0 (IF0)) has been set to 0. If WDTIF is 1, selecting watchdog timer mode 1 or 2 causes a non-maskable interrupt to be generated the instant rewriting ends.

5.6 Serial Interface 10

5.6.1 Functions of serial interface 10

Serial interface 10 has the following two modes.

- Operation stopped mode
- 3-wire serial I/O mode

(1) Operation stopped mode

This mode is used to minimize power consumption when serial transfer is not performed.

(2) 3-wire serial I/O mode (switchable between MSB-first and LSB-first transmission)

This mode is used to transmit 8-bit data, using three lines: a serial clock line (SCK10) and two serial data lines (SI10 and SO10).

As 3-wire serial I/O mode supports simultaneous transmission and reception, the time required for data processing can be reduced.

In 3-wire serial I/O mode, it is possible to select whether 8-bit data transmission begins with the MSB or LSB, allowing serial interface 10 to be connected to any device regardless of whether that device is designed for MSB-first or LSB-first transmission.

3-wire serial I/O mode is effective for connecting peripheral I/O circuits and display controllers having conventional clock synchronous serial interfaces, such as those of the 75XL, 78K, and 17K Series devices.

5.6.2 Configuration of serial interface 10

Serial interface 10 consists of the following hardware.

Table 5-10. Configuration of Serial Interface 10

| Item | Configuration |
|------------------|--|
| Register | Transmission/reception shift register 10 (SIO10) |
| Control register | Serial operation mode register 10 (CSIM10) |

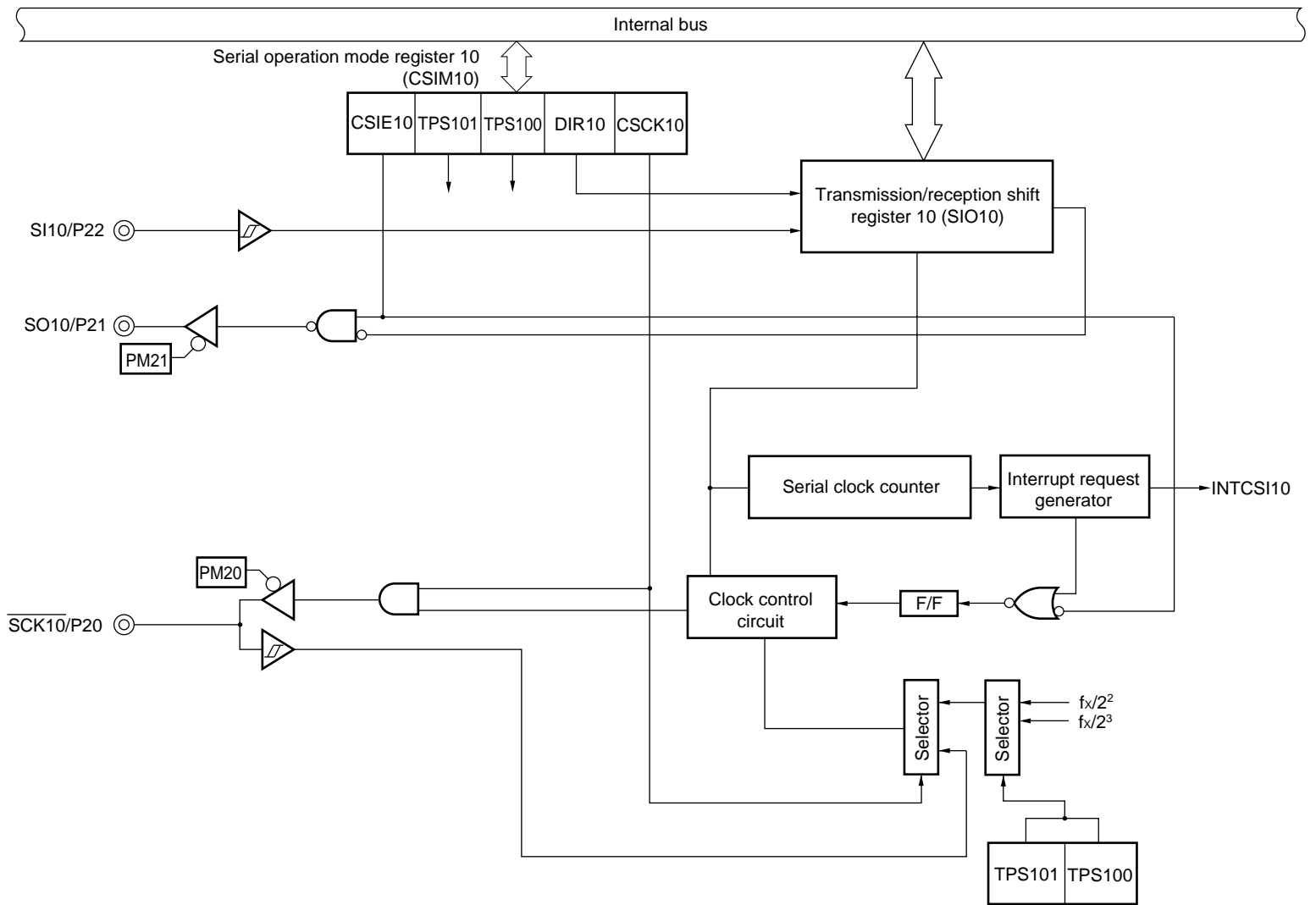
(1) Transmission/reception shift register 10 (SIO10)

This is an 8-bit register used for parallel/serial data conversion and for serial transmission or reception in synchronization with the serial clock.

SIO10 is set using an 8-bit memory manipulation instruction.

RESET input makes this register undefined.

Figure 5-22. Block Diagram of Serial Interface 10



5.6.3 Control register for serial interface 10

Serial interface 10 is controlled by the following register.

- Serial operation mode register 10 (CSIM10)

Figure 5-23. Format of Serial Operation Mode Register 10

| Symbol | <7> | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|--------|---|--------|--------|---|-------|--------|---|---------|-------------|-----|
| CSIM10 | CSIE10 | 0 | TPS101 | TPS100 | 0 | DIR10 | CSCK10 | 0 | FF72H | 00H | R/W |

| | |
|--------|--|
| CSIE10 | 3-wire serial I/O mode operation control |
| 0 | Operation stopped |
| 1 | Operation enabled |

| | | |
|------------------|--------|---|
| TPS101 | TPS100 | Selection of count clock when internal clock selected |
| 0 | 0 | $f_x/2^2$ (1.25 MHz) |
| 0 | 1 | $f_x/2^3$ (625 kHz) |
| Other than above | | Setting prohibited |

| | |
|-------|-------------------------|
| DIR10 | First-bit specification |
| 0 | MSB |
| 1 | LSB |

| | |
|--------|--|
| CSCK10 | SIO10 clock selection |
| 0 | External clock pulse input to the $\overline{SCK10}$ pin |
| 1 | Internal clock selected with TPS100, TPS101 |

Cautions 1. Bits 0, 3 and 6 must be fixed to 0.

2. Be sure to switch to operation mode after stopping the serial transmission/reception operation.

Remarks 1. f_x : Main system clock oscillation frequency

2. The parenthesized values apply to operation at $f_x = 5.0$ MHz.

Table 5-11. Operation Mode Settings for Serial Interface 10

(1) Operation stopped mode

| CSIM10 | | | PM22 | P22 | PM21 | P21 | PM20 | P20 | First Bit | Shift Clock | P22/SI10 Pin Function | P21/SO10 Pin Function | P20/ $\overline{\text{SCK10}}$ Pin Function |
|------------------|-------|-----------------------------|------|-----|------|-----|------|-----|--------------------|-------------|-----------------------|-----------------------|---|
| CSIE10 | DIR10 | C $\overline{\text{SCK10}}$ | | | | | | | | | | | |
| 0 | × | × | × | × | × | × | × | × | — | — | P22 | P21 | P20 |
| Other than above | | | | | | | | | Setting prohibited | | | | |

(2) 3-wire serial I/O mode

| CSIM10 | | | PM22 | P22 | PM21 | P21 | PM20 | P20 | First Bit | Shift Clock | P22/SI10 Pin Function | P21/SO10 Pin Function | P20/ $\overline{\text{SCK10}}$ Pin Function | | | |
|------------------|-------|-----------------------------|------|-----|------|-----|------|-----|--------------------|------------------------|-----------------------|---------------------------------|---|----------------------------------|----------------|---------------------------------|
| CSIE10 | DIR10 | C $\overline{\text{SCK10}}$ | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | × | 0 | 1 | 1 | × | MSB | SI10 ^{Note 2} | SO10 (CMOS output) | $\overline{\text{SCK10}}$ input | | | | |
| | | 1 | | | | | | | | | | 0 | 1 | $\overline{\text{SCK10}}$ output | | |
| | 1 | 0 | | | | | 1 | × | | | | 1 | × | LSB | External clock | $\overline{\text{SCK10}}$ input |
| | | 1 | | | | | | | | | | | | | 0 | 1 |
| Other than above | | | | | | | | | Setting prohibited | | | | | | | |

- Notes**
1. Can be used freely as a port
 2. Can be used as P22 (CMOS I/O) only when transmitting

Remark ×: don't care

5.7 LCD Controller/Driver

5.7.1 LCD controller/driver functions


The LCD controller/driver incorporated in the μPD789322, 789324, 789326, and 789327 has the following features.

- (1) Segment and common signals based on the automatic reading of the display data memory can be automatically output
- (2) Four types of frame frequencies are selectable
- (3) 24 segment signal outputs (S0 to S23), 4 common signal outputs (COM0 to COM3)
- (4) Operation with a subsystem clock is possible

The maximum number of displayable pixels is shown in Table 5-12 below.

Table 5-12. Maximum Number of Display Pixels

| Bias Method | Time Division | Common Signals Used | Maximum Number of Display Pixels |
|-------------|---------------|---------------------|----------------------------------|
| 1/3 | 4 | COM0 to COM3 | 96 (24 segments × 4 commons) |

Note The LCD panel of the figure  consists of 12 rows with 2 segments per row.

5.7.2 LCD controller/driver configuration

The LCD controller/driver consists of the following hardware.

Table 5-13. Configuration of LCD Controller/Driver

| Item | Configuration |
|-------------------|---|
| Display outputs | Segment signals: 24 Common signals: 4 |
| Control registers | LCD display mode register 0 (LCDM0) LCD clock control register 0 (LCDC0) Port function register 8 (PF8) |

The correspondence with the LCD display RAM is shown in Figure 5-24 below.

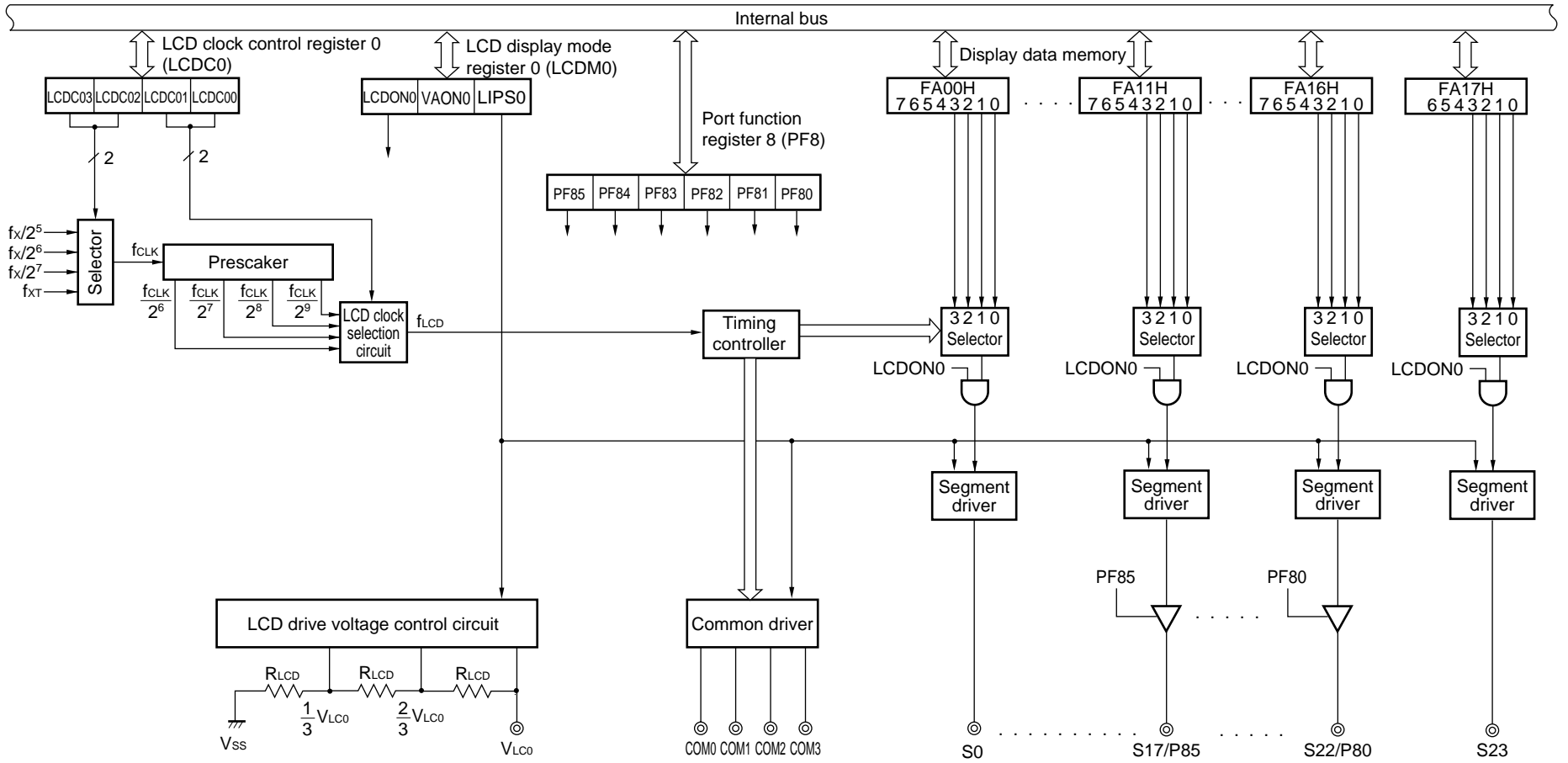
Figure 5-24. Correspondence with LCD Display RAM

| Address | Bit | | | | | | | | Segment |
|---------|-----|---|---|---|---|---|---|---|---------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| FA17H | 0 | 0 | 0 | 0 | | | | | → S23 |
| FA16H | 0 | 0 | 0 | 0 | | | | | → S22 |
| FA15H | 0 | 0 | 0 | 0 | | | | | → S21 |
| FA14H | 0 | 0 | 0 | 0 | | | | | → S20 |
| FA13H | 0 | 0 | 0 | 0 | | | | | → S19 |
| FA12H | 0 | 0 | 0 | 0 | | | | | → S18 |
| FA11H | 0 | 0 | 0 | 0 | | | | | → S17 |
| FA10H | 0 | 0 | 0 | 0 | | | | | → S16 |
| FA0FH | 0 | 0 | 0 | 0 | | | | | → S15 |
| FA0EH | 0 | 0 | 0 | 0 | | | | | → S14 |
| FA0DH | 0 | 0 | 0 | 0 | | | | | → S13 |
| FA0CH | 0 | 0 | 0 | 0 | | | | | → S12 |
| FA0BH | 0 | 0 | 0 | 0 | | | | | → S11 |
| FA0AH | 0 | 0 | 0 | 0 | | | | | → S10 |
| FA09H | 0 | 0 | 0 | 0 | | | | | → S9 |
| FA08H | 0 | 0 | 0 | 0 | | | | | → S8 |
| FA07H | 0 | 0 | 0 | 0 | | | | | → S7 |
| FA06H | 0 | 0 | 0 | 0 | | | | | → S6 |
| FA05H | 0 | 0 | 0 | 0 | | | | | → S5 |
| FA04H | 0 | 0 | 0 | 0 | | | | | → S4 |
| FA03H | 0 | 0 | 0 | 0 | | | | | → S3 |
| FA02H | 0 | 0 | 0 | 0 | | | | | → S2 |
| FA01H | 0 | 0 | 0 | 0 | | | | | → S1 |
| FA00H | 0 | 0 | 0 | 0 | | | | | → S0 |

↑ ↑ ↑ ↑
 Common COM3 COM2 COM1 COM0

Remark Bits 4 to 7 are fixed to 0.

Figure 5-25. LCD Controller/Driver Block Diagram



5.7.3 LCD controller/driver control registers

The LCD controller/driver is controlled by the following three registers.

- LCD display mode register 0 (LCDM0)
- LCD clock control register 0 (LCDC0)
- Port function register 8 (PF8)

(1) LCD display mode register 0 (LCDM0)

This register is used to enable/disable operation, and set the operation mode and the supply of power for LCD drive. LCDM0 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-26. Format of LCD Display Mode Register 0

| Symbol | <7> | <6> | 5 | <4> | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|--------|-------|---|-------|---|---|---|---|---------|-------------|-----|
| LCDM0 | LCDON0 | VAON0 | 0 | LIPS0 | 0 | 0 | 0 | 0 | FFB0H | 00H | R/W |

| | |
|--------|--|
| LCDON0 | LCD display enable/disable |
| 0 | Display off (all segment outputs are unselected for signal output) |
| 1 | Display on |

| | |
|-------|--|
| VAON0 | LCD controller/driver operation mode ^{Note} |
| 0 | No internal booster (for 2.7- to 5.5-V display) |
| 1 | Internal booster enabled (for 1.8- to 5.5-V display) |

| | |
|-------|---|
| LIPS0 | Supply of power for LCD drive ^{Note} |
| 0 | Power not supplied for LCD drive |
| 1 | Power supplied for LCD drive |

Note To reduce power consumption when the LCD display is not being used, set VAON0 and LIPS0 to 0.

Cautions 1. Always set bits 0 to 3 and 5 to 0.

2. When manipulating VAON0, observe following procedure.

A. When internal booster is stopped after changing to the display off condition from the display on condition

- 1) Set the display off condition by setting LCDON0 = 0.
- 2) Set all segment buffers and common buffers to output disabled by setting LIPS0 = 0.
- 3) Stop the booster by setting VAON0 = 0.

B. When the booster is stopped in the display on condition

This is prohibited. Be sure to stop the booster after changing to the display off condition.

C. When the display is turned on from the booster-stoped condition

- 1) Wait about 500 ms after starting the booster by setting VAON0 = 1.
- 2) Set all segment buffers and common buffers to signal output unselected by setting LIPS0 = 1.
- 3) Set the display on condition by setting LCDON0 = 1.

(2) LCD clock control register (LCDC0)

This register is used to set the internal and LCD clocks. The frame frequency is determined by the number of LCD clock time divisions.

LCDC0 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-27. Format of LCD Clock Control Register 0

| | | | | | | | | | | | |
|--------|---|---|---|---|--------|--------|--------|--------|---------|-------------|-----|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
| LCDC0 | 0 | 0 | 0 | 0 | LCDC03 | LCDC02 | LCDC01 | LCDC00 | FFB2H | 00H | R/W |

| LCDC03 | LCDC02 | Internal clock (f _{CLK}) selection ^{Note} |
|--------|--------|--|
| 0 | 0 | f _{XT} (32.768 kHz) |
| 0 | 1 | f _X /2 ⁵ (156.3 kHz) |
| 1 | 0 | f _X /2 ⁶ (78.1 kHz) |
| 1 | 1 | f _X /2 ⁷ (39.1 kHz) |

| LCDC01 | LCDC00 | LCD clock (f _{LCB}) selection |
|--------|--------|---|
| 0 | 0 | f _{CLK} /2 ⁶ |
| 0 | 1 | f _{CLK} /2 ⁷ |
| 1 | 0 | f _{CLK} /2 ⁸ |
| 1 | 1 | f _{CLK} /2 ⁹ |

Note Select f_X so that a clock of at least 32 kHz is set for the internal clock f_{CLK}.

- Remarks**
1. f_X: Main system clock oscillation frequency
 2. f_{XT}: Subsystem clock oscillation frequency
 3. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz

Caution Always set bits 4 to 7 to 0.

Examples of the frame frequencies when the internal clock is f_{XT} (32.768 kHz) are shown in Table 5-14 below.

Table 5-14. Frame Frequency (Hz)

| LCD Clock (f _{LCB}) \ Time Division | f _{XT} /2 ⁹ (64 Hz) | f _{XT} /2 ⁸ (128 Hz) | f _{XT} /2 ⁷ (256 Hz) | f _{XT} /2 ⁶ (512 Hz) |
|---|--|---|---|---|
| 4 | 16 | 32 | 64 | 128 |

(3) Port function register 8 (PF8)

This register is used to select whether S17/P85 to S22/P80 are used as LCD segment signal outputs or general-purpose ports.

PF8 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 5-28. Format of Port Function Register 8

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|------|------|------|------|------|------|---------|-------------|-----|
| PF8 | 0 | 0 | PF85 | PF84 | PF83 | PF82 | PF81 | PF80 | FF58H | 00H | R/W |

| PF8n | Port function of P8n (n = 0 to 5) |
|------|--|
| 0 | Operates as a general-purpose port |
| 1 | Operates as an LCD segment signal output |

6. INTERRUPT FUNCTION

6.1 Interrupt Types

Two types of interrupts are supported.

(1) Non-maskable interrupts

Non-maskable interrupt requests are acknowledged unconditionally, i.e. even when interrupts are disabled.

These interrupts take precedence over all other interrupts and are not subject to interrupt priority control.

A non-maskable interrupt causes the generation of the standby release signal.

An interrupt from the watchdog timer is the only non-maskable interrupt source supported in the μ PD789322, 789324, 789326, and 789327.

(2) Maskable interrupts

Maskable interrupts are subject to mask control. If two or more maskable interrupts occur simultaneously, the default priority listed in Table 6-1 applies.

A maskable interrupt causes the generation of the standby release signal.

Maskable interrupts from 2 external and 6 internal sources are supported in the μ PD789322, 789324, 789326, and 789327.

6.2 Interrupt Sources and Configuration

The μ PD789322, 789324, 789326, and 789327 support a total of 9 maskable and non-maskable interrupt sources (see **Table 6-1**).

Table 6-1. Interrupt Sources

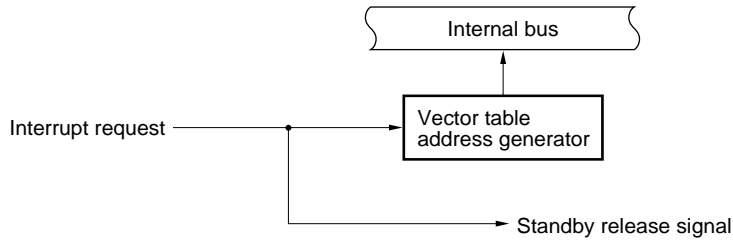
| Interrupt Type | Default Priority ^{Note 1} | Interrupt Source | | Internal/ External | Vector Table Address | Basic Configuration Type ^{Note 2} |
|----------------|------------------------------------|--------------------------------------|---|--------------------|----------------------|--|
| | | Name | Trigger | | | |
| Non-maskable | – | INTWDT | Watchdog timer overflow (with watchdog timer mode 1 selected) | Internal | 0004H | (A) |
| Maskable | 0 | INTWDT | Watchdog timer overflow (with interval timer mode selected) | | | |
| | 1 | INTP0 | Pin input edge detection | External | 0006H | (C) |
| | 2 | INTCSI10 | End of serial interface 10 3-wire SIO transfer reception | Internal | 0008H | (B) |
| | 3 | INTWT | Watch timer interrupt | | 000AH | |
| | 4 | INTTM30 | Generation of 8-bit timer 30 matching signal | | 000CH | |
| | 5 | INTTM40 | Generation of 8-bit timer 40 matching signal | | 000EH | |
| | 6 | INTKR00 | Key return signal detection | External | 0010H | (C) |
| 7 | INTWTI | Watch timer interval timer interrupt | Internal | 0012H | (B) | |

- Notes**
1. Default priority is the priority order when more than one maskable interrupt request is generated at the same time. 0 is the highest priority and 7 is the lowest.
 2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in **Figure 6-1**.

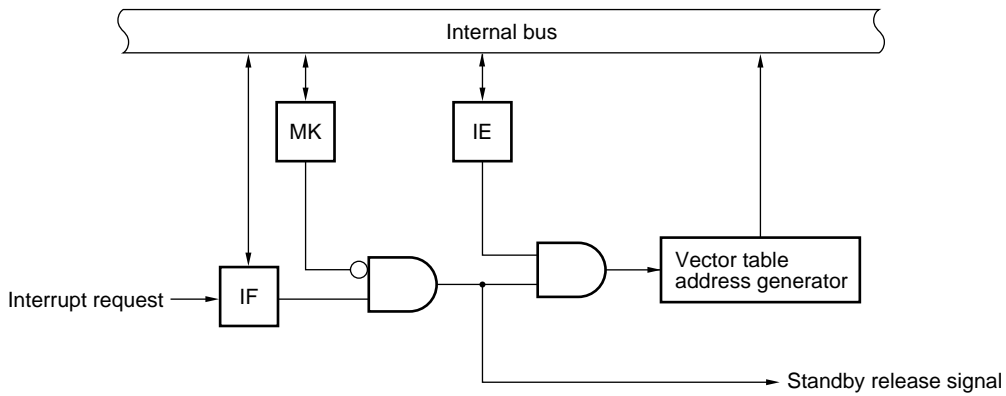
Remark Only one of the two watchdog timer interrupt sources, non-maskable or maskable (internal), can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

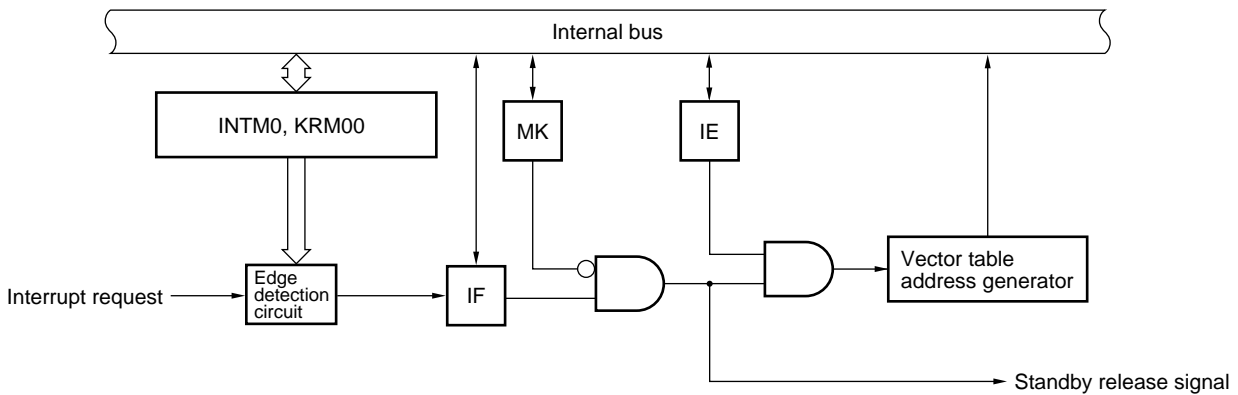
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



INTM0: External interrupt mode register 0

KRM00: Key return mode register 00

IF: Interrupt request flag

IE: Interrupt enable flag

MK: Interrupt mask flag

6.3 Interrupt Function Control Registers

Interrupts are controlled by the following five registers.

- Interrupt request flag register 0 (IF0)
- Interrupt mask flag register 0 (MK0)
- External interrupt mode register 0 (INTM0)
- Program status word (PSW)
- Key return mode register 00 (KRM00)

Table 6-2 lists the interrupt requests and the corresponding interrupt request and interrupt mask flags.

Table 6-2. Interrupt Request Signals and Corresponding Flags

| Interrupt Request Signal | Interrupt Request Flag | Interrupt Mask Flag |
|--------------------------|------------------------|---------------------|
| INTWDT | WDTIF | WDTMK |
| INTP0 | PIF0 | PMK0 |
| INTCSI0 | CSIIF0 | CSIMK0 |
| INTWT | WTIF | WTMK |
| INTTM30 | TMIF30 | TMMK30 |
| INTTM40 | TMIF40 | TMMK40 |
| INTKR00 | KRIF00 | KRMK00 |
| INTWTI | WTIIF | WTIMK |

(1) Interrupt request flag register 0 (IF0)

An interrupt request flag is set (1) when the corresponding interrupt request is generated, or when an instruction is executed. It is cleared (0) when the interrupt request is acknowledged, when the $\overline{\text{RESET}}$ signal is input, or when an instruction is executed.

IF0 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-2. Format of Interrupt Request Flag Register 0

| Symbol | <7> | <6> | <5> | <4> | <3> | <2> | <1> | <0> | Address | After reset | R/W |
|--------|-------|--------|--------|--------|------|--------|------|-------|---------|-------------|-----|
| IF0 | WTIIF | KRIF00 | TMIF40 | TMIF30 | WTIF | CSIIF0 | PIF0 | WDTIF | FFE0H | 00H | R/W |

| xxIFx | Interrupt request flag |
|-------|--|
| 0 | No interrupt request signal generated |
| 1 | An interrupt request signal is generated and an interrupt request made |

Cautions 1. The WDTIF flag can be read/written only when the watchdog timer is being used as an interval timer. It must be cleared to 0 if the watchdog timer is used in watchdog timer mode 1 or 2.

2. Because P61 functions alternately as an external interrupt, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) before using the port in output mode.

(2) Interrupt mask flag register 0 (MK0)

Interrupt mask flags are used to enable and disable the corresponding maskable interrupts.

MK0 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to FFH.

Figure 6-3. Format of Interrupt Mask Flag Register 0

| Symbol | <7> | <6> | <5> | <4> | <3> | <2> | <1> | <0> | Address | After reset | R/W |
|--------|-------|--------|--------|--------|------|--------|------|-------|---------|-------------|-----|
| MK0 | WTIMK | KRMK00 | TMMK40 | TMMK30 | WTMK | CSIMK0 | PMK0 | WDTMK | FFE4H | FFH | R/W |

| xxMK | Interrupt servicing control |
|------|------------------------------|
| 0 | Interrupt servicing enabled |
| 1 | Interrupt servicing disabled |

- Cautions**
1. When the watchdog timer is being used in watchdog timer mode 1 or 2, any attempt to read the WDTMK flag results in an undefined value being detected.
 2. Because P61 functions alternately as an external interrupt, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) before using the port in output mode.

(3) External interrupt mode register 0 (INTM0)

This register is used to specify the valid edge for INTP0.

INTM0 is set using an 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 6-4. Format of External Interrupt Mode Register 0

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|---|---|------|------|---|---|---------|-------------|-----|
| INTM0 | 0 | 0 | 0 | 0 | ES01 | ES00 | 0 | 0 | FFECH | 00H | R/W |

| ES01 | ES00 | INTP0 valid edge selection |
|------|------|-------------------------------|
| 0 | 0 | Falling edge |
| 0 | 1 | Rising edge |
| 1 | 0 | Setting prohibited |
| 1 | 1 | Both rising and falling edges |

Cautions 1. Always set bits 0, 1, and 4 to 7 to 0.

2. Before setting INTM0, set (1) the interrupt mask flag (PMK0) to disable interrupts.

To enable interrupts, clear (0) the interrupt request flag (PIF0), then clear (0) the interrupt mask flag (PMK0).

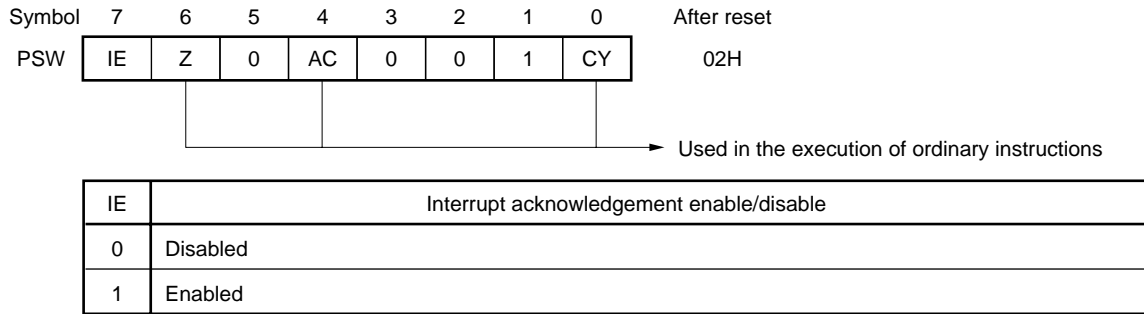
(4) Program status word (PSW)

The program status word is used to hold the instruction execution results and the current status of the interrupt requests. The IE flag, used to enable and disable maskable interrupts, is mapped to the PSW.

The PSW can be read and written in 8-bit units, as well as in 1-bit units by using bit manipulation instructions and dedicated instructions (EI and DI). When a vector interrupt is acknowledged, the PSW is automatically saved to the stack, and the IE flag is reset (0).

RESET input sets the PSW to 02H.

Figure 6-5. Program Status Word Configuration



(5) Key return mode register 00 (KRM00)

This register is used to set the pin that is to detect the key return signal (rising edge of port 4).

KRM00 is set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

Figure 6-6. Format of Key Return Mode Register 00

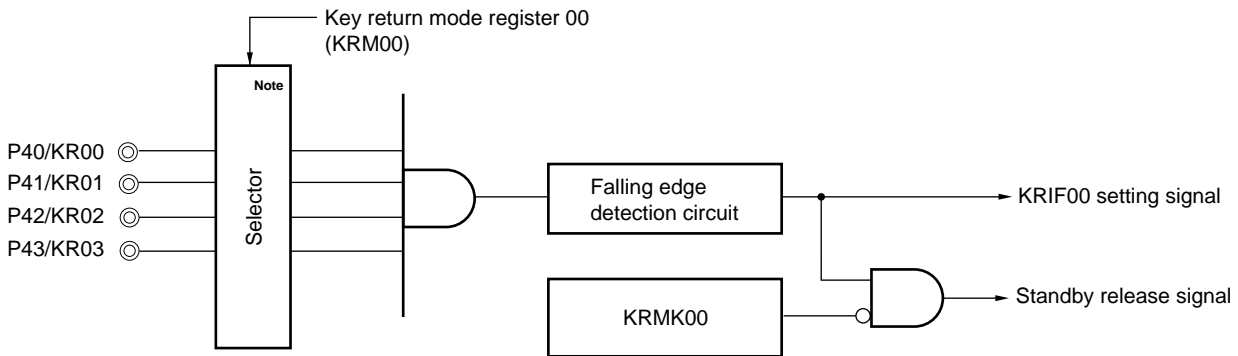
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|---|---|---|---|---|--------|---------|-------------|-----|
| KRM00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRM000 | FFF5H | 00H | R/W |

| | |
|--------|--|
| KRM000 | Key return signal detection control |
| 0 | Key return signal not detected |
| 1 | Key return signal detected (port 4 falling edge detection) |

Cautions 1. Always set bits 1 to 7 to 0.

2. Before setting KRM00, set (1) bit 6 (KRMK00) of MK0 to disable interrupts. To enable interrupts, clear (0) KRMK00 after clearing (0) bit 6 (KRIF00) of IF0.
3. On-chip pull-up resistors are automatically connected in input mode to the pins specified for key return signal detection (P40 to P43). Although these resistors are disconnected when the mode changes to output, key return signal detection continues unchanged.

Figure 6-7. Block Diagram of Falling Edge Detection Circuit



Note For selecting the pin to be used as falling edge input.

7. STANDBY FUNCTION

7.1 Standby Function

A standby function is incorporated to minimize the system's power consumption. There are two standby modes: HALT and STOP.

The HALT and STOP modes are selected using the HALT and STOP instructions.

(1) HALT mode

In this mode, the CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation combining this mode with the normal operation mode.

(2) STOP mode

In this mode, main system clock oscillation is stopped. All operations performed with the main system clock are suspended, thus minimizing power consumption.

Caution When shifting to STOP mode, execute the STOP instruction after first stopping the operation of the hardware.

Table 7-1. Operation Statuses in HALT Mode

| Item | HALT Mode Operation Status During Main System Clock Operation | | HALT Mode Operation Status During Subsystem Clock Operation | |
|------------------------|---|--------------------------------|---|--------------------------------|
| | Subsystem Clock Operating | Subsystem Clock Stopped | Main System Clock Operating | Main System Clock Stopped |
| Main system clock | Can be oscillated | | | Oscillation stopped |
| CPU | Operation stopped | | | |
| Ports (output latches) | Status before HALT mode setting retained | | | |
| 8-bit timer 30, 40 | Operable | | | Operation stopped |
| Watch timer | Operable | Operable ^{Note 1} | Operable | Operable ^{Note 2} |
| Watchdog timer | Operable | | Operation stopped | |
| Power-on-clear circuit | Operable | | | |
| Key return circuit | Operable | | | |
| Serial interface 10 | Operable | | | Operable ^{Note 3} |
| LCD controller/driver | Operable ^{Note 4} | Operable ^{Notes 1, 4} | Operable ^{Note 4} | Operable ^{Notes 2, 4} |
| External interrupts | Operable ^{Note 5} | | | |

- Notes**
1. Operation is enabled when the main system clock is selected
 2. Operation is enabled when the subsystem clock is selected
 3. Operation is enabled only when an external clock is selected
 4. The HALT instruction can be set after display instruction execution
 5. Operation is enabled only for a maskable interrupt that is not masked

Table 7-2. Operation Statuses in STOP Mode

| Item | STOP Mode Operation Status During Main System Clock Operation | |
|------------------------|---|-------------------------|
| | Subsystem Clock Operating | Subsystem Clock Stopped |
| Main system clock | Oscillation stopped | |
| CPU | Operation stopped | |
| Ports (output latches) | Status before STOP mode setting retained | |
| 8-bit timer 30, 40 | Operation stopped | |
| Watch timer | Operable ^{Note 1} | Operation stopped |
| Watchdog timer | Operation stopped | |
| Power-on-clear circuit | Operable | |
| Key return circuit | Operable | |
| Serial interface 10 | Operable ^{Note 2} | |
| LCD controller/driver | Operable ^{Note 1} | Operation stopped |
| External interrupts | Operable ^{Note 3} | |

- Notes**
1. Operation is enabled when the subsystem clock is selected.
 2. Operation is enabled only when an external clock is selected.
 3. Operation is enabled only for a maskable interrupt that is not masked

7.2 Standby Function Control Register

The oscillation stabilization time selection register (OSTS) is used to control the wait time from the time STOP mode is released by an interrupt request until oscillation stabilizes.

OSTS is set using an 8-bit memory manipulation instruction.

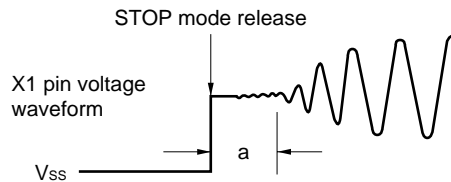
RESET input sets this register to 04H. Note that the time required for oscillation to stabilize after RESET input or the release of STOP mode by POC will be taken as the time selected by mask option ($2^{15}/f_x$, or $2^{17}/f_x$) (refer to 9. MASK OPTION for mask option details).

Figure 7-1. Format of Oscillation Stabilization Time Selection Register

| | | | | | | | | | | | |
|--------|---|---|---|---|---|-------|-------|-------|---------|-------------|-----|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
| OSTS | 0 | 0 | 0 | 0 | 0 | OSTS2 | OSTS1 | OSTS0 | FFFAH | 04H | R/W |

| OSTS2 | OSTS1 | OSTS0 | Oscillation stabilization time selection |
|------------------|-------|-------|--|
| 0 | 0 | 0 | $2^{12}/f_x$ (819 μs) |
| 0 | 1 | 0 | $2^{15}/f_x$ (6.55 ms) |
| 1 | 0 | 0 | $2^{17}/f_x$ (26.2 ms) |
| Other than above | | | Setting prohibited |

Caution The wait time required after releasing STOP mode does not include the time (“a” in the following figure) required for the clock oscillation to restart after STOP mode is released, regardless of whether STOP mode is released by RESET input or interrupt.



- Remarks**
1. f_x : Main system clock oscillation frequency
 2. The parenthesized values apply to operation at $f_x = 5.0$ MHz.

8. RESET FUNCTION

8.1 Reset Function

The μPD789322, 789324, 789326, and 789327 can be reset using the following three signals.

- (1) External reset signal input via $\overline{\text{RESET}}$ pin
- (2) Internal reset by watchdog timer runaway time detection
- (3) Internal reset using power-on-clear circuit (POC)

The external and internal reset signals are functionally equivalent. When $\overline{\text{RESET}}$ is input, program execution begins from the addresses written at addresses 0000H and 0001H.

If a low-level signal is applied to the $\overline{\text{RESET}}$ pin, or if the watchdog timer overflows, a reset occurs, causing each item of the hardware to enter the states listed in Table 8-1. While a reset is being applied, or while the oscillation frequency is stabilizing immediately after the end of a reset sequence, each pin remains in the high-impedance state.

If a high-level signal is applied to the $\overline{\text{RESET}}$ pin, the reset sequence is terminated, and program execution begins once the oscillation stabilization time has elapsed. A reset sequence caused by a watchdog timer overflow is terminated automatically and again program execution begins upon the elapse of the oscillation stabilization time. Reset by power-ON clear is cleared if the supply voltage rises beyond a specific level, and the program execution is started after the oscillation stabilization time has elapsed.

- Cautions**
1. To use an external reset sequence, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 μs.
 2. When a reset is used to release STOP mode, the data of when STOP mode was entered is retained during the reset sequence, except for the port pins, which are in the high-impedance state.
 3. The oscillation stabilization time after $\overline{\text{RESET}}$ input or the release of STOP mode by POC can be selected from $2^{15}/f_x$ or $2^{17}/f_x$ by mask option (refer to 9. MASK OPTION).

Figure 8-1. Reset Function Block Diagram

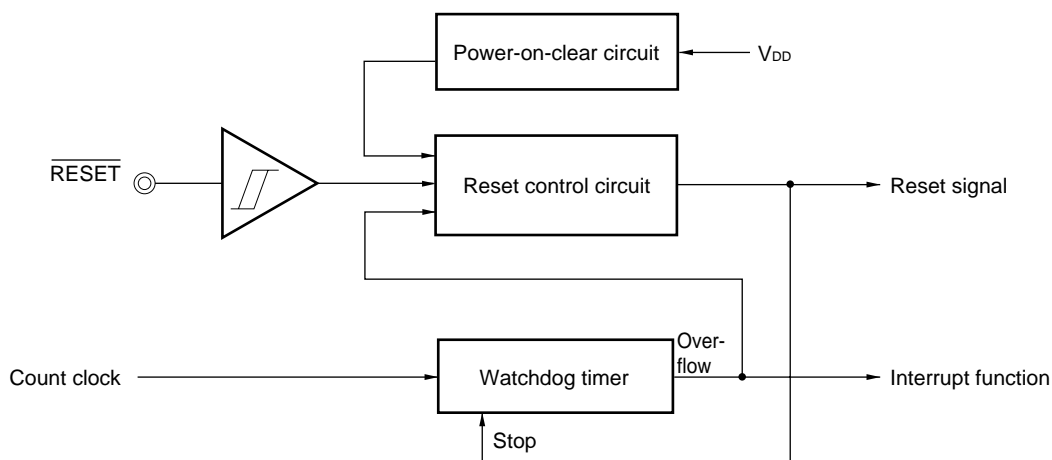


Table 8-1. Status of Hardware After Reset

| Hardware | | Status After Reset |
|--|---|---|
| Program counter (PC) ^{Note 1} | | Contents of reset vector table (0000H, 0001H) set |
| Stack pointer (SP) | | Undefined |
| Program status word (PSW) | | 02H |
| RAM | Data memory | Undefined ^{Note 2} |
| | General-purpose registers | Undefined ^{Note 2} |
| Ports (P0 to P2, P4, P6, P8) (output latches) | | 00H |
| Port mode registers (PM0 to PM2, PM4, PM6, PM8) | | FFH |
| Port function register 8 (PF8) | | 00H |
| Pull-up resistor option registers (PU0, PUB2) | | 00H |
| Processor clock control register (PCC) | | 02H |
| Subclock oscillation mode register (SCKM) | | 00H |
| Subclock control register (CSS) | | 00H |
| Oscillation stabilization time selection register (OSTS) | | 04H |
| 8-bit timer 30, 40 | Timer counters (TM30, TM40) | 00H |
| | Compare registers (CR30, CR40, CRH40) | Undefined |
| | Mode control registers (TMC30, TMC40) | 00H |
| | Carrier generator output control register (TCA40) | 00H |
| Watch timer | Mode control register (WTM) | 00H |
| Watchdog timer | Mode register (WDTM) | 00H |
| Serial interface 10 | Serial operation mode register 10 (CSIM10) | 00H |
| | Transmission/reception shift register 10 (SIO10) | Undefined |
| LCD controller/driver | Display mode register 0 (LCDM0) | 00H |
| | Clock control register 0 (LCDC0) | 00H |
| Power-on-clear circuit | Power-on-clear register 1 (POCF1) | 00H ^{Note 3} |
| Interrupts | Request flag register 0 (IF0) | 00H |
| | Mask flag register 0 (MK0) | FFH |
| | External interrupt mode register 0 (INTM0) | 00H |
| | Key return mode register 00 (KRM00) | 00H |

- Notes**
1. While a reset signal is being input, and during the oscillation stabilization period, only the contents of the PC will be undefined; the remainder of the hardware will be the same state as after reset.
 2. In standby mode, RAM enters the hold state after reset.
 3. The value is 04H only after a power-on-clear reset.

8.2 Power Failure Detection Function

When a reset is generated via the power-on-clear circuit, bit 2 (POCOF1) of the power-on-clear register (POCF1) is set (1). This bit is then cleared (0) by an instruction written to POCF1. After a power-on-clear reset (i.e. after program execution has started from address 0000H), a power failure can be detected by detecting POCOF1.

Figure 8-2. Format of Power-on-Clear Register 1

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|--------|---|---|---|---|---|--------|---|---|---------|---------------------|-----|
| POCF1 | 0 | 0 | 0 | 0 | 0 | POCOF1 | 0 | 0 | FFDDH | 00H ^{Note} | R/W |

| | |
|--------|---|
| POCOF1 | Power-on-clear generation status detection |
| 0 | Power-on-clear not generated, or cleared by write operation |
| 1 | Power-on-clear reset generated |

Note The value is 04H only after a power-on-clear reset.

9. MASK OPTION

The μ PD789322, 789324, 789326, and 789327 have the following mask option.

- Oscillation stabilization wait time

The oscillation stabilization wait time after the release of STOP mode by $\overline{\text{RESET}}$ or POC can be selected.

<1> $2^{15}/f_x$

<2> $2^{17}/f_x$

10. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789322, 789324, 789326, and 789327 are listed in this section.

10.1 Conventions

10.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform to the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, \$, and brackets [] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- \$: Relative address specification
- !: Absolute address specification
- []: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, \$, or [].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 5-1 below).

Table 10-1. Operand Formats and Descriptions

| Format | Description |
|---------------------|---|
| r rp sfr | X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol |
| saddr saddrp | FE20H to FF1FH Immediate data or label FE20H to FF1FH Immediate data or label (even addresses only) |
| addr16 addr5 | 0000H to FFFFH Immediate data or label (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or label (even addresses only) |
| word byte bit | 16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label |

Remark For details concerning special function register symbols, refer to **Table 4-1 Special Function Registers**.

10.1.2 Operation field definitions

| | |
|-----------------------------------|---|
| A: | A register (8-bit accumulator) |
| X: | X register |
| B: | B register |
| C: | C register |
| D: | D register |
| E: | E register |
| H: | H register |
| L: | L register |
| AX: | AX register pair (16-bit accumulator) |
| BC: | BC register pair |
| DE: | DE register pair |
| HL: | HL register pair |
| PC: | Program counter |
| SP: | Stack pointer |
| PSW: | Program status word |
| CY: | Carry flag |
| AC: | Auxiliary carry flag |
| Z: | Zero flag |
| IE: | Interrupt request enable flag |
| NMIS: | Flag to indicate that a non-maskable interrupt is being processed |
| (): | Contents of a memory location indicated by a parenthesized address or register name |
| X _H , X _L : | Higher and lower 8 bits of a 16-bit register |
| ∧: | Logical product (AND) |
| ∨: | Logical sum (OR) |
| ⊕: | Exclusive OR |
| —: | Inverted data |
| addr16: | 16-bit immediate data or label |
| jdisp8: | Signed 8-bit data (displacement value) |

10.1.3 Flag operation field definitions

| | |
|----------|--------------------------------------|
| (Blank): | No change |
| 0: | Clear to 0 |
| 1: | Set to 1 |
| ×: | Set or clear according to the result |
| R: | Restore to the previous value |

10.2 Operations

| Mnemonic | Operand | Byte | Clock | Operation | Flag | | |
|----------|------------------------------|------|-------|---|------|----|----|
| | | | | | Z | AC | CY |
| MOV | r, #byte | 3 | 6 | $r \leftarrow \text{byte}$ | | | |
| | saddr, #byte | 3 | 6 | $(\text{saddr}) \leftarrow \text{byte}$ | | | |
| | sfr, #byte | 3 | 6 | $\text{sfr} \leftarrow \text{byte}$ | | | |
| | A, r <small>Note 1</small> | 2 | 4 | $A \leftarrow r$ | | | |
| | r, A <small>Note 1</small> | 2 | 4 | $r \leftarrow A$ | | | |
| | A, saddr | 2 | 4 | $A \leftarrow (\text{saddr})$ | | | |
| | saddr, A | 2 | 4 | $(\text{saddr}) \leftarrow A$ | | | |
| | A, sfr | 2 | 4 | $A \leftarrow \text{sfr}$ | | | |
| | sfr, A | 2 | 4 | $\text{sfr} \leftarrow A$ | | | |
| | A, !addr16 | 3 | 8 | $A \leftarrow (\text{addr16})$ | | | |
| | !addr16, A | 3 | 8 | $(\text{addr16}) \leftarrow A$ | | | |
| | PSW, #byte | 3 | 6 | $\text{PSW} \leftarrow \text{byte}$ | x | x | x |
| | A, PSW | 2 | 4 | $A \leftarrow \text{PSW}$ | | | |
| | PSW, A | 2 | 4 | $\text{PSW} \leftarrow A$ | x | x | x |
| | A, [DE] | 1 | 6 | $A \leftarrow (\text{DE})$ | | | |
| | [DE], A | 1 | 6 | $(\text{DE}) \leftarrow A$ | | | |
| | A, [HL] | 1 | 6 | $A \leftarrow (\text{HL})$ | | | |
| | [HL], A | 1 | 6 | $(\text{HL}) \leftarrow A$ | | | |
| | A, [HL + byte] | 2 | 6 | $A \leftarrow (\text{HL} + \text{byte})$ | | | |
| | [HL + byte], A | 2 | 6 | $(\text{HL} + \text{byte}) \leftarrow A$ | | | |
| XCH | A, X | 1 | 4 | $A \leftrightarrow X$ | | | |
| | A, r <small>Note 2</small> | 2 | 6 | $A \leftrightarrow r$ | | | |
| | A, saddr | 2 | 6 | $A \leftrightarrow (\text{saddr})$ | | | |
| | A, sfr | 2 | 6 | $A \leftrightarrow (\text{sfr})$ | | | |
| | A, [DE] | 1 | 8 | $A \leftrightarrow (\text{DE})$ | | | |
| | A, [HL] | 1 | 8 | $A \leftrightarrow (\text{HL})$ | | | |
| | A, [HL + byte] | 2 | 8 | $A \leftrightarrow (\text{HL} + \text{byte})$ | | | |
| MOVW | rp, #word | 3 | 6 | $\text{rp} \leftarrow \text{word}$ | | | |
| | AX, saddrp | 2 | 6 | $\text{AX} \leftarrow (\text{saddrp})$ | | | |
| | saddrp, AX | 2 | 8 | $(\text{saddrp}) \leftarrow \text{AX}$ | | | |
| | AX, rp <small>Note 3</small> | 1 | 4 | $\text{AX} \leftarrow \text{rp}$ | | | |
| | rp, AX <small>Note 3</small> | 1 | 4 | $\text{rp} \leftarrow \text{AX}$ | | | |
| XCHW | AX, rp <small>Note 3</small> | 1 | 8 | $\text{AX} \leftrightarrow \text{rp}$ | | | |

- Notes**
1. Except when $r = A$.
 2. Except when $r = A$ or X .
 3. Only when $\text{rp} = \text{BC}, \text{DE},$ or HL .

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag | | |
|----------|----------------|------|-------|---|------|----|----|
| | | | | | Z | AC | CY |
| ADD | A, #byte | 2 | 4 | $A, CY \leftarrow A + \text{byte}$ | x | x | x |
| | saddr, #byte | 3 | 6 | $(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte}$ | x | x | x |
| | A, r | 2 | 4 | $A, CY \leftarrow A + r$ | x | x | x |
| | A, saddr | 2 | 4 | $A, CY \leftarrow A + (\text{saddr})$ | x | x | x |
| | A, !addr16 | 3 | 8 | $A, CY \leftarrow A + (\text{addr16})$ | x | x | x |
| | A, [HL] | 1 | 6 | $A, CY \leftarrow A + (\text{HL})$ | x | x | x |
| | A, [HL + byte] | 2 | 6 | $A, CY \leftarrow A + (\text{HL} + \text{byte})$ | x | x | x |
| ADDC | A, #byte | 2 | 4 | $A, CY \leftarrow A + \text{byte} + CY$ | x | x | x |
| | saddr, #byte | 3 | 6 | $(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte} + CY$ | x | x | x |
| | A, r | 2 | 4 | $A, CY \leftarrow A + r + CY$ | x | x | x |
| | A, saddr | 2 | 4 | $A, CY \leftarrow A + (\text{saddr}) + CY$ | x | x | x |
| | A, !addr16 | 3 | 8 | $A, CY \leftarrow A + (\text{addr16}) + CY$ | x | x | x |
| | A, [HL] | 1 | 6 | $A, CY \leftarrow A + (\text{HL}) + CY$ | x | x | x |
| | A, [HL + byte] | 2 | 6 | $A, CY \leftarrow A + (\text{HL} + \text{byte}) + CY$ | x | x | x |
| SUB | A, #byte | 2 | 4 | $A, CY \leftarrow A - \text{byte}$ | x | x | x |
| | saddr, #byte | 3 | 6 | $(\text{saddr}), CY \leftarrow (\text{saddr}) - \text{byte}$ | x | x | x |
| | A, r | 2 | 4 | $A, CY \leftarrow A - r$ | x | x | x |
| | A, saddr | 2 | 4 | $A, CY \leftarrow A - (\text{saddr})$ | x | x | x |
| | A, !addr16 | 3 | 8 | $A, CY \leftarrow A - (\text{addr16})$ | x | x | x |
| | A, [HL] | 1 | 6 | $A, CY \leftarrow A - (\text{HL})$ | x | x | x |
| | A, [HL + byte] | 2 | 6 | $A, CY \leftarrow A - (\text{HL} + \text{byte})$ | x | x | x |
| SUBC | A, #byte | 2 | 4 | $A, CY \leftarrow A - \text{byte} - CY$ | x | x | x |
| | saddr, #byte | 3 | 6 | $(\text{saddr}), CY \leftarrow (\text{saddr}) - \text{byte} - CY$ | x | x | x |
| | A, r | 2 | 4 | $A, CY \leftarrow A - r - CY$ | x | x | x |
| | A, saddr | 2 | 4 | $A, CY \leftarrow A - (\text{saddr}) - CY$ | x | x | x |
| | A, !addr16 | 3 | 8 | $A, CY \leftarrow A - (\text{addr16}) - CY$ | x | x | x |
| | A, [HL] | 1 | 6 | $A, CY \leftarrow A - (\text{HL}) - CY$ | x | x | x |
| | A, [HL + byte] | 2 | 6 | $A, CY \leftarrow A - (\text{HL} + \text{byte}) - CY$ | x | x | x |
| AND | A, #byte | 2 | 4 | $A \leftarrow A \wedge \text{byte}$ | x | | |
| | saddr, #byte | 3 | 6 | $(\text{saddr}) \leftarrow (\text{saddr}) \wedge \text{byte}$ | x | | |
| | A, r | 2 | 4 | $A \leftarrow A \wedge r$ | x | | |
| | A, saddr | 2 | 4 | $A \leftarrow A \wedge (\text{saddr})$ | x | | |
| | A, !addr16 | 3 | 8 | $A \leftarrow A \wedge (\text{addr16})$ | x | | |
| | A, [HL] | 1 | 6 | $A \leftarrow A \wedge (\text{HL})$ | x | | |
| | A, [HL + byte] | 2 | 6 | $A \leftarrow A \wedge (\text{HL} + \text{byte})$ | x | | |

Remark The instruction clock cycle is based on the CPU clock (f_{cpu}) specified by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag | | |
|----------|----------------|------|-------|---|------|----|----|
| | | | | | Z | AC | CY |
| OR | A, #byte | 2 | 4 | $A \leftarrow A \vee \text{byte}$ | | x | |
| | saddr, #byte | 3 | 6 | $(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$ | | x | |
| | A, r | 2 | 4 | $A \leftarrow A \vee r$ | | x | |
| | A, saddr | 2 | 4 | $A \leftarrow A \vee (\text{saddr})$ | | x | |
| | A, !addr16 | 3 | 8 | $A \leftarrow A \vee (\text{addr16})$ | | x | |
| | A, [HL] | 1 | 6 | $A \leftarrow A \vee (\text{HL})$ | | x | |
| | A, [HL + byte] | 2 | 6 | $A \leftarrow A \vee (\text{HL} + \text{byte})$ | | x | |
| XOR | A, #byte | 2 | 4 | $A \leftarrow A \nabla \text{byte}$ | | x | |
| | saddr, #byte | 3 | 6 | $(\text{saddr}) \leftarrow (\text{saddr}) \nabla \text{byte}$ | | x | |
| | A, r | 2 | 4 | $A \leftarrow A \nabla r$ | | x | |
| | A, saddr | 2 | 4 | $A \leftarrow A \nabla (\text{saddr})$ | | x | |
| | A, !addr16 | 3 | 8 | $A \leftarrow A \nabla (\text{addr16})$ | | x | |
| | A, [HL] | 1 | 6 | $A \leftarrow A \nabla (\text{HL})$ | | x | |
| | A, [HL + byte] | 2 | 6 | $A \leftarrow A \nabla (\text{HL} + \text{byte})$ | | x | |
| CMP | A, #byte | 2 | 4 | $A - \text{byte}$ | x | x | x |
| | saddr, #byte | 3 | 6 | $(\text{saddr}) - \text{byte}$ | x | x | x |
| | A, r | 2 | 4 | $A - r$ | x | x | x |
| | A, saddr | 2 | 4 | $A - (\text{saddr})$ | x | x | x |
| | A, !addr16 | 3 | 8 | $A - (\text{addr16})$ | x | x | x |
| | A, [HL] | 1 | 6 | $A - (\text{HL})$ | x | x | x |
| | A, [HL + byte] | 2 | 6 | $A - (\text{HL} + \text{byte})$ | x | x | x |
| ADDW | AX, #word | 3 | 6 | $\text{AX}, \text{CY} \leftarrow \text{AX} + \text{word}$ | x | x | x |
| SUBW | AX, #word | 3 | 6 | $\text{AX}, \text{CY} \leftarrow \text{AX} - \text{word}$ | x | x | x |
| CMPW | AX, #word | 3 | 6 | $\text{AX} - \text{word}$ | x | x | x |
| INC | r | 2 | 4 | $r \leftarrow r + 1$ | x | x | |
| | saddr | 2 | 4 | $(\text{saddr}) \leftarrow (\text{saddr}) + 1$ | x | x | |
| DEC | r | 2 | 4 | $r \leftarrow r - 1$ | x | x | |
| | saddr | 2 | 4 | $(\text{saddr}) \leftarrow (\text{saddr}) - 1$ | x | x | |
| INCW | rp | 1 | 4 | $\text{rp} \leftarrow \text{rp} + 1$ | | | |
| DECW | rp | 1 | 4 | $\text{rp} \leftarrow \text{rp} - 1$ | | | |
| ROR | A, 1 | 1 | 2 | $(\text{CY}, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$ | | | x |
| ROL | A, 1 | 1 | 2 | $(\text{CY}, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$ | | | x |
| RORC | A, 1 | 1 | 2 | $(\text{CY} \leftarrow A_0, A_7 \leftarrow \text{CY}, A_{m-1} \leftarrow A_m) \times 1$ | | | x |
| ROLC | A, 1 | 1 | 2 | $(\text{CY} \leftarrow A_7, A_0 \leftarrow \text{CY}, A_{m+1} \leftarrow A_m) \times 1$ | | | x |

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag | | |
|----------|-----------|------|-------|--|------|----|----|
| | | | | | Z | AC | CY |
| SET1 | saddr.bit | 3 | 6 | (saddr.bit) ← 1 | | | |
| | sfr.bit | 3 | 6 | sfr.bit ← 1 | | | |
| | A.bit | 2 | 4 | A.bit ← 1 | | | |
| | PSW.bit | 3 | 6 | PSW bit ← 1 | × | × | × |
| | [HL].bit | 2 | 10 | (HL).bit ← 1 | | | |
| CLR1 | saddr.bit | 3 | 6 | (saddr.bit) ← 0 | | | |
| | sfr.bit | 3 | 6 | sfr.bit ← 0 | | | |
| | A.bit | 2 | 4 | A.bit ← 0 | | | |
| | PSW.bit | 3 | 6 | PSW.bit ← 0 | × | × | × |
| | [HL].bit | 2 | 10 | (HL).bit ← 0 | | | |
| SET1 | CY | 1 | 2 | CY ← 1 | | | 1 |
| CLR1 | CY | 1 | 2 | CY ← 0 | | | 0 |
| NOT1 | CY | 1 | 2 | CY ← \overline{CY} | | | × |
| CALL | !addr16 | 3 | 6 | (SP - 1) ← (PC + 3) _H , (SP - 2) ← (PC + 3) _L , PC ← addr16, SP ← SP - 2 | | | |
| CALLT | [addr5] | 1 | 8 | (SP - 1) ← (PC + 1) _H , (SP - 2) ← (PC + 1) _L , PC _H ← (00000000, addr5 + 1), PC _L ← (00000000, addr5), SP ← SP - 2 | | | |
| RET | | 1 | 6 | PC _H ← (SP + 1), PC _L ← (SP), SP ← SP + 2 | | | |
| RETI | | 1 | 8 | PC _H ← (SP + 1), PC _L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0 | R | R | R |
| PUSH | PSW | 1 | 2 | (SP - 1) ← PSW, SP ← SP - 1 | | | |
| | rp | 1 | 4 | (SP - 1) ← rp _H , (SP - 2) ← rp _L , SP ← SP - 2 | | | |
| POP | PSW | 1 | 4 | PSW ← (SP), SP ← SP + 1 | R | R | R |
| | rp | 1 | 6 | rp _H ← (SP + 1), rp _L ← (SP), SP ← SP + 2 | | | |
| MOVW | SP, AX | 2 | 8 | SP ← AX | | | |
| | AX, SP | 2 | 6 | AX ← SP | | | |
| BR | !addr16 | 3 | 6 | PC ← addr16 | | | |
| | \$addr16 | 2 | 6 | PC ← PC + 2 + jdisp8 | | | |
| | AX | 1 | 6 | PC _H ← A, PC _L ← X | | | |

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag | | |
|----------|---------------------|------|-------|---|------|----|----|
| | | | | | Z | AC | CY |
| BC | \$addr16 | 2 | 6 | $PC \leftarrow PC + 2 + jdisp8$ if $CY = 1$ | | | |
| BNC | \$addr16 | 2 | 6 | $PC \leftarrow PC + 2 + jdisp8$ if $CY = 0$ | | | |
| BZ | \$addr16 | 2 | 6 | $PC \leftarrow PC + 2 + jdisp8$ if $Z = 1$ | | | |
| BNZ | \$addr16 | 2 | 6 | $PC \leftarrow PC + 2 + jdisp8$ if $Z = 0$ | | | |
| BT | saddr.bit, \$addr16 | 4 | 10 | $PC \leftarrow PC + 4 + jdisp8$ if (saddr.bit) = 1 | | | |
| | sfr.bit, \$addr16 | 4 | 10 | $PC \leftarrow PC + 4 + jdisp8$ if sfr.bit = 1 | | | |
| | A.bit, \$addr16 | 3 | 8 | $PC \leftarrow PC + 3 + jdisp8$ if A.bit = 1 | | | |
| | PSW.bit, \$addr16 | 4 | 10 | $PC \leftarrow PC + 4 + jdisp8$ if PSW.bit = 1 | | | |
| BF | saddr.bit, \$addr16 | 4 | 10 | $PC \leftarrow PC + 4 + jdisp8$ if (saddr.bit) = 0 | | | |
| | sfr.bit, \$addr16 | 4 | 10 | $PC \leftarrow PC + 4 + jdisp8$ if sfr.bit = 0 | | | |
| | A.bit, \$addr16 | 3 | 8 | $PC \leftarrow PC + 3 + jdisp8$ if A.bit = 0 | | | |
| | PSW.bit, \$addr16 | 4 | 10 | $PC \leftarrow PC + 4 + disp8$ if PSW.bit = 0 | | | |
| DBNZ | B, \$addr16 | 2 | 6 | $B \leftarrow B - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $B \neq 0$ | | | |
| | C, \$addr16 | 2 | 6 | $C \leftarrow C - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $C \neq 0$ | | | |
| | saddr, \$addr16 | 3 | 8 | (saddr) \leftarrow (saddr) - 1, then $PC \leftarrow PC + 3 + jdisp8$ if (saddr) $\neq 0$ | | | |
| NOP | | 1 | 2 | No Operation | | | |
| EI | | 3 | 6 | $IE \leftarrow 1$ (Enable Interrupt) | | | |
| DI | | 3 | 6 | $IE \leftarrow 0$ (Disable Interrupt) | | | |
| HALT | | 1 | 2 | Set HALT Mode | | | |
| STOP | | 1 | 2 | Set STOP Mode | | | |

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------|------------------|---|--|------|
| Supply voltage | V _{DD} | | -0.3 to +6.5 | V |
| | V _{LC0} | | -0.3 to +6.5 | V |
| Input voltage | V _I | | -0.3 to V _{DD} + 0.3 ^{Note} | V |
| Output voltage | V _{O1} | P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61 | -0.3 to V _{DD} + 0.3 ^{Note} | V |
| | V _{O2} | COM0 to COM3, S0 to S16, P80/S22 to P85/S17, S23 | -0.3 to V _{LC0} + 0.3 ^{Note} | V |
| Output current, high | I _{OH} | Pin P60/TO40 | -30 | mA |
| | | Per pin (except P60/TO40) | -10 | mA |
| | | Total for all pins (except P60/TO40) | -30 | mA |
| Output current, low | I _{OL} | Per pin | 30 | mA |
| | | Total for all pins | 80 | mA |
| Operating ambient temperature | T _A | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | -65 to +150 | °C |

Note 6.5 V or lower

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (TA = -40 to +85°C, VDD = 1.8 to 5.5 V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---------------------|--|--|------|------|------|------|
| Ceramic resonator | | Oscillation frequency (fx) ^{Note 1} | | 1.0 | | 5.0 | MHz |
| | | Oscillation stabilization time ^{Note 2} | After VDD has reached the MIN. oscillation voltage range | | | 4 | ms |
| Crystal resonator | | Oscillation frequency (fx) ^{Note 1} | | 1.0 | | 5.0 | MHz |
| | | Oscillation stabilization time ^{Note 2} | | | | 30 | ms |
| External clock | | X1 input frequency (fx) ^{Note 1} | | 1.0 | | 5.0 | MHz |
| | | X1 input high-/low-level width (txH, txL) | | 85 | | 500 | ns |

- Notes**
1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as Vss.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---------------------|--|--------------------------------|------|--------|------|------|
| Crystal resonator | | Oscillation frequency (f _{XT}) ^{Note 1} | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time ^{Note 2} | V _{DD} = 4.5 to 5.5 V | | 1.2 | 2 | s |
| External clock | | XT1 input frequency (f _{XT}) ^{Note 1} | | 32 | | 35 | kHz |
| | | XT1 input high-/low-level width (t _{XTH} , t _{XTL}) | | 14.3 | | 15.6 | μs |

- Notes**
1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
 2. The time required for oscillation to stabilize after V_{DD} reaches the MIN. oscillation voltage range. Use a resonator to stabilize oscillation during the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|----------------------|-------------------|--|--|------------------------|-----------------|---------------------|----|
| Output current, low | I _{OL} | Per pin | | | 10 | mA | |
| | | Total for all pins | | | 80 | mA | |
| Output current, high | I _{OH} | Per pin (except P60/TO40) | | | -1 | mA | |
| | | P60/TO40 | V _{DD} = 3.0 V, V _{OH} = 1.0 V | -7 | -15 | -24 | mA |
| | | Total for all pins (except P60/TO40) | | | -15 | mA | |
| Input voltage, high | V _{IH1} | P00 to P03, P10, P11, P21, P22, P60 | V _{DD} = 2.7 to 5.5 V | 0.7 V _{DD} | | V _{DD} | V |
| | | | | 0.9 V _{DD} | | V _{DD} | V |
| | V _{IH2} | RESET, P20, P40 to P43, P61 | V _{DD} = 2.7 to 5.5 V | 0.8 V _{DD} | | V _{DD} | V |
| | | | | 0.9 V _{DD} | | V _{DD} | V |
| V _{IH3} | X1, X2 | | V _{DD} - 0.1 | | V _{DD} | V | |
| V _{IH4} | XT1, XT2 | | V _{DD} - 0.1 | | V _{DD} | V | |
| Input voltage, low | V _{IL1} | P00 to P03, P10, P11, P21, P22, P60 | V _{DD} = 2.7 to 5.5 V | 0 | | 0.3 V _{DD} | V |
| | | | | 0 | | 0.1 V _{DD} | V |
| | V _{IL2} | RESET, P20, P40 to P43, P61 | V _{DD} = 2.7 to 5.5 V | 0 | | 0.2 V _{DD} | V |
| | | | | 0 | | 0.1 V _{DD} | V |
| V _{IL3} | X1, X2 | | 0 | | 0.1 | V | |
| V _{IL4} | XT1, XT2 | | 0 | | 0.1 | V | |
| Output voltage, high | V _{OH11} | P00 to P03, P10, P11, P20 to P22, P40 to P43, P61 | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OH} = -100 μA | V _{DD} - 0.5 | | | V |
| | | | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OH} = -500 μA | V _{DD} - 0.7 | | | V |
| | V _{OH21} | P60/TO40 | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OH} = -400 μA | V _{DD} - 0.5 | | | V |
| | | | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OH} = -2 mA | V _{DD} - 0.7 | | | V |
| | V _{OH31} | P80/S22 to P85/S17 | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OH} = -100 μA | V _{LC0} - 0.5 | | | V |
| | | | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OH} = -500 μA | V _{LC0} - 0.7 | | | V |
| Output voltage, low | V _{OL11} | P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61 | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OL} = 400 μA | | | 0.5 | V |
| | | | 1.8 ≤ V _{DD} ≤ 5.5 V, I _{OL} = 2 mA | | | 0.7 | V |
| | V _{OL21} | P80/S22 to P85/S17 | 1.8 ≤ V _{LC0} ≤ 5.5 V, I _{OL} = 400 μA | | | 0.5 | V |
| | | | 1.8 ≤ V _{LC0} ≤ 5.5 V, I _{OL} = 2 mA | | | 0.7 | V |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|-------------------|--|---|------|------|------|------|
| Input leakage current, high | I _{LIH1} | V _{IN} = V _{DD} | P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61, $\overline{\text{RESET}}$ | | | 3 | μA |
| | I _{LIH2} | | X1, X2, XT1, XT2 | | | 20 | μA |
| Input leakage current, low | I _{LIL1} | V _{IN} = 0 V | P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61, $\overline{\text{RESET}}$ | | | -3 | μA |
| | I _{LIL2} | | X1, X2, XT1, XT2 | | | -20 | μA |
| Output leakage current, high | I _{LOH} | V _{OUT} = V _{DD} | | | | 3 | μA |
| Output leakage current, low | I _{LOL} | V _{OUT} = 0 V | | | | -3 | μA |
| Software pull-up resistors | R ₁ | V _{IN} = 0 V | P00 to P03, P10, P11, P20 to P22, P40 to P43 | 50 | 100 | 200 | kΩ |
| Supply current ^{Note 1} Ceramic/crystal oscillation | I _{DD1} | 5.0-MHz crystal oscillation operating mode | V _{DD} = 5.5 V ^{Note 2} | | 2.0 | 4.0 | mA |
| | | | V _{DD} = 3.3 V ^{Note 3} | | 0.6 | 1.2 | mA |
| | I _{DD2} | 5.0-MHz crystal oscillation HALT mode | V _{DD} = 5.5 V | | 1.1 | 2.2 | mA |
| | | | V _{DD} = 3.3 V | | 0.4 | 0.8 | mA |
| | I _{DD3} | 32.768-kHz crystal oscillation HALT mode ^{Note 4} | V _{DD} = 5.5 V | | 25 | 55 | μA |
| | | | V _{DD} = 3.3 V | | 5 | 25 | μA |
| | I _{DD4} | STOP mode | V _{DD} = 5.5 V | | 1 | 10 | μA |
| | | | V _{DD} = 3.3 V | | 1 | 5 | μA |

Notes 1. Current flowing through ports (including current flowing through on-chip pull-up resistors) is not included.

2. High-speed operation (when the processor clock control register (PCC) is set to 00H).

3. Low-speed operation (when PCC is set to 02H)

4. When the main system clock is stopped.

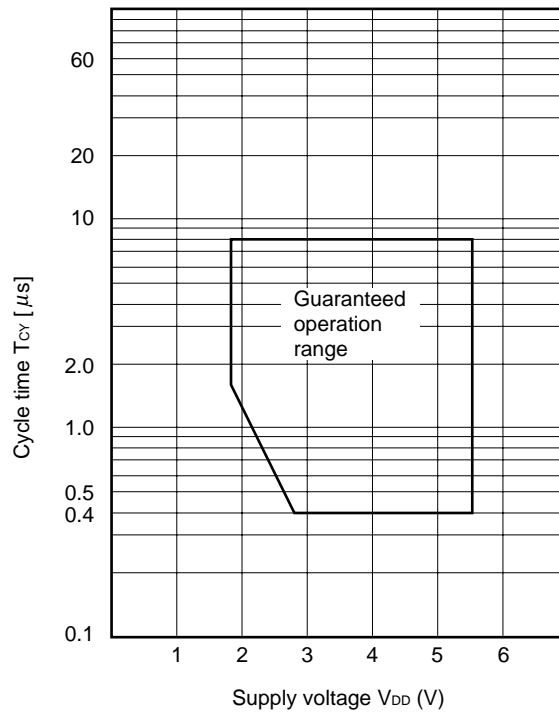
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|----------------------------|---------------------------|------|------|------|---------------|
| Cycle time (Min. instruction execution time) | T_{CY} | $V_{DD} = 2.7$ to 5.5 V | 0.4 | | 8.0 | μs |
| | | | 1.6 | | 8.0 | μs |
| Interrupt input high-/low-level width | t_{INTH} , t_{INTL} | INT | 10 | | | μs |
| Key return pin low-level width | t_{KRIL} | KR00 to KR03 | 10 | | | μs |
| $\overline{\text{RESET}}$ low-level width | t_{RSL} | | 10 | | | μs |

T_{CY} vs. V_{DD} (Main System Clock)



(2) Serial interface 10 (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (Internal clock output)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--|--|----------------------------|------|-------|------|
| SCK10 cycle time | t _{KCY1} | V _{DD} = 2.7 to 5.5 V | 800 | | | ns |
| | | | 3,200 | | | ns |
| SCK10 high-/low-level width | t _{KH1} , t _{KL1} | V _{DD} = 2.7 to 5.5 V | t _{KCY1} /2 - 50 | | | ns |
| | | | t _{KCY1} /2 - 150 | | | ns |
| SI10 setup time (to SCK10 ↑) | t _{SIK1} | V _{DD} = 2.7 to 5.5 V | 150 | | | ns |
| | | | 500 | | | ns |
| SI10 hold time (from SCK10 ↑) | t _{KSI1} | V _{DD} = 2.7 to 5.5 V | 400 | | | ns |
| | | | 800 | | | ns |
| SO10 output delay time from SCK10 ↓ | t _{KSO1} | R = 1 kΩ, C = 100 pF ^{Note} V _{DD} = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | 250 | | 1,000 | ns |

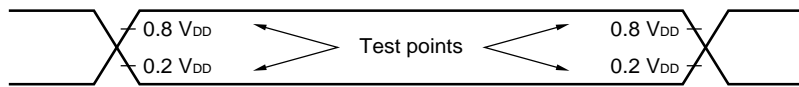
Note R and C are the load resistance and load capacitance of the SO10 output line.

(b) 3-wire serial I/O mode (External clock input)

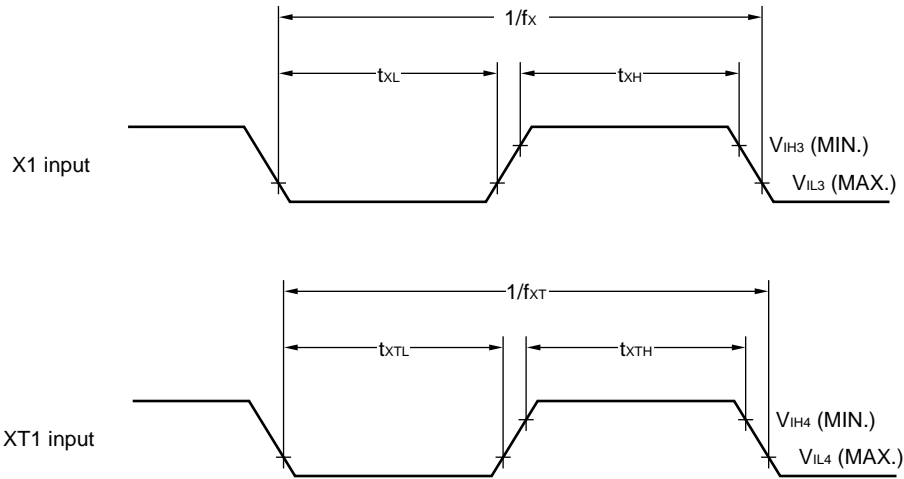
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--|--|-------|------|-------|------|
| SCK10 cycle time | t _{KCY2} | V _{DD} = 2.7 to 5.5 V | 900 | | | ns |
| | | | 3,500 | | | ns |
| SCK10 high-/low-level width | t _{KH2} , t _{KL2} | V _{DD} = 2.7 to 5.5 V | 400 | | | ns |
| | | | 1,600 | | | ns |
| SI10 setup time (to SCK10 ↑) | t _{SIK2} | V _{DD} = 2.7 to 5.5 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI10 hold time (from SCK10 ↑) | t _{KSI2} | V _{DD} = 2.7 to 5.5 V | 400 | | | ns |
| | | | 600 | | | ns |
| SO10 output delay time from SCK10 ↓ | t _{KSO2} | R = 1 kΩ, C = 100 pF ^{Note} V _{DD} = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | 250 | | 1,000 | ns |

Note R and C are the load resistance and load capacitance of the SO10 output line.

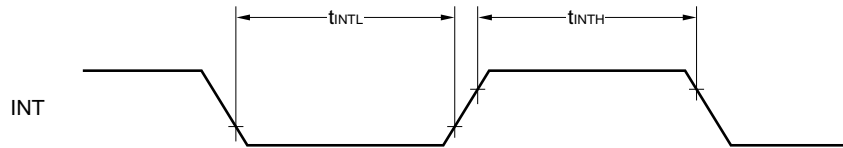
AC Timing Measurement Point (excluding X1, XT1 input)



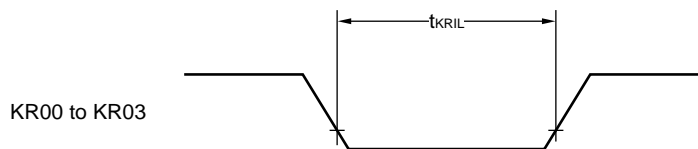
Clock Timing



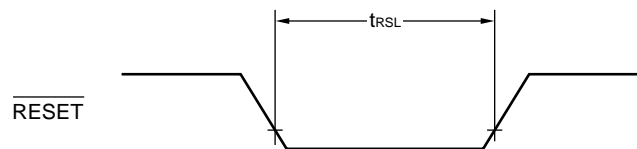
Interrupt Input Timing



Key Return Input Timing

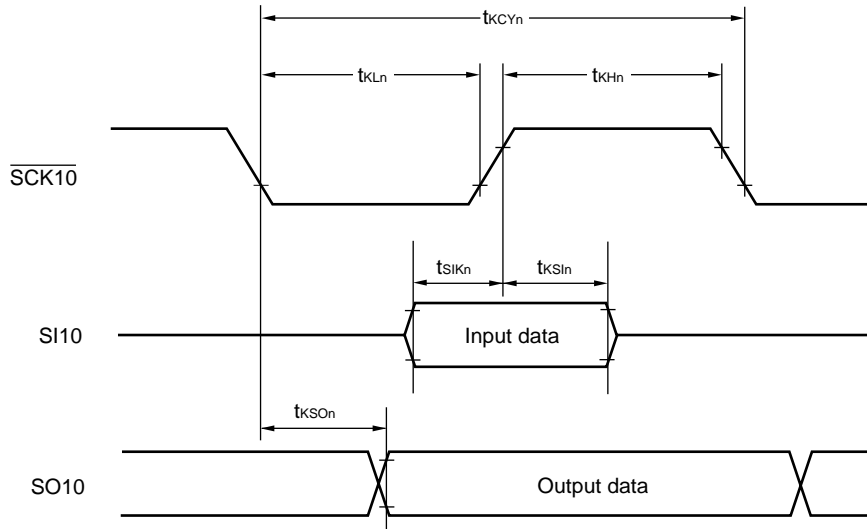


RESET Input Timing



Serial Transfer Timing

3-wire serial I/O mode:



Remark n = 1, 2

LCD Characteristics (T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|------------------|-----------------------------|----------|------|------|------|------|
| LCD drive voltage | V _{LCO} | VAON0 ^{Note 1} = 1 | | 1.8 | | 5.5 | V |
| | | VAON0 ^{Note 1} = 0 | | 2.7 | | 5.5 | V |
| LCD division resistance | R _{LCD} | | | 50 | 100 | 200 | kΩ |
| LCD output voltage differential ^{Note 2} (common) | V _{ODC} | I _o = ±5 μA | 1/3 bias | 0 | | ±0.2 | V |
| LCD output voltage differential ^{Note 2} (segment) | V _{ODS} | I _o = ±1 μA | 1/3 bias | 0 | | ±0.2 | V |

- Notes**
1. Bit 6 of LCD display mode register 0 (LCDM0)
 2. The voltage differential is the difference between the output voltage and the ideal value of the segment and common signal outputs.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

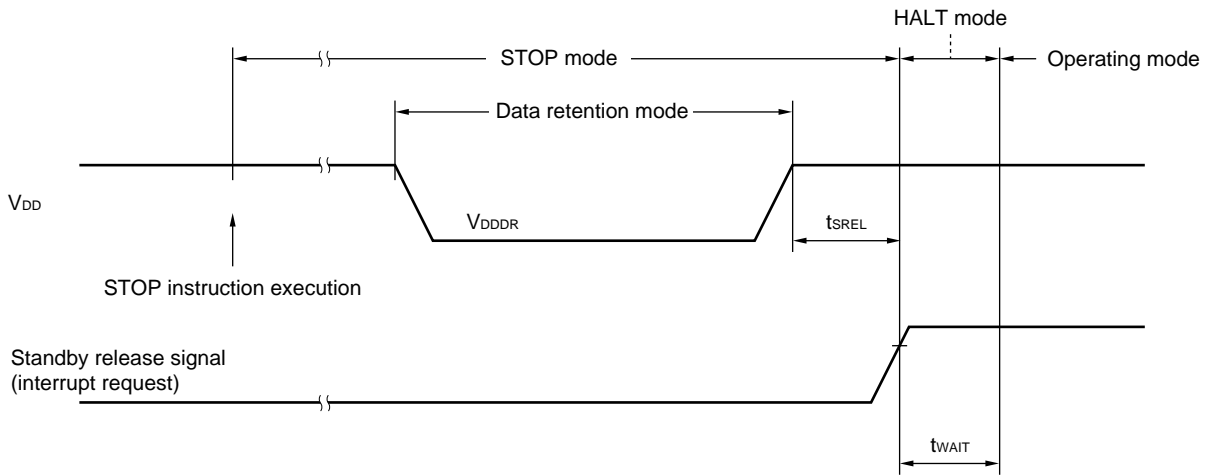
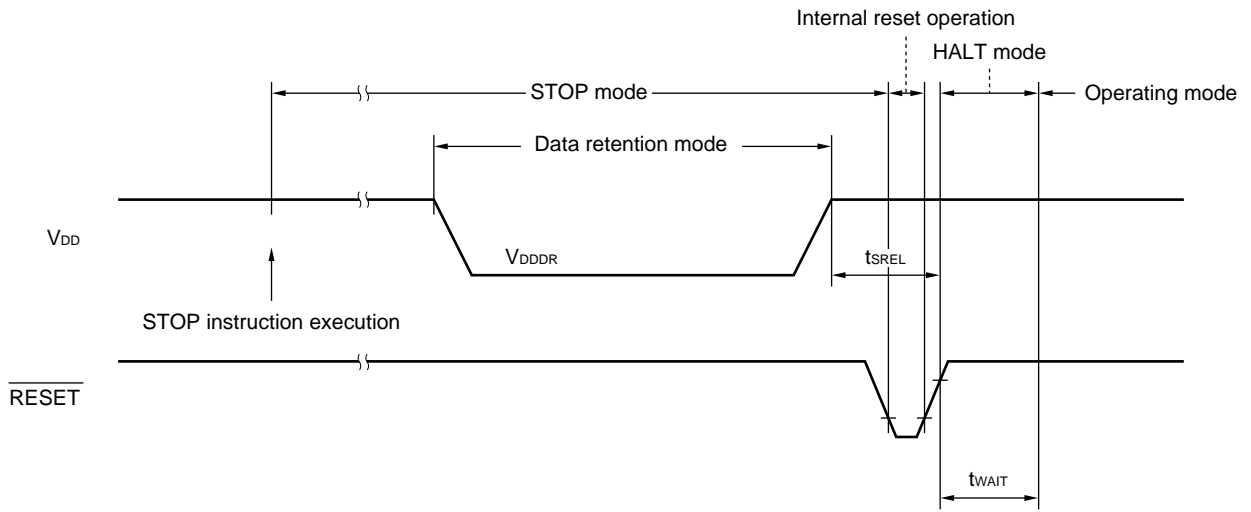
(T_A = -40 to +85°C, V_{DD} = 1.8 to 5.5 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|---|------|---------------|------|------|
| Data retention supply voltage | V _{DDDR} | | 1.8 | | 3.6 | V |
| Low voltage detection (POC) voltage | V _{POC} | Response time: 2 ms ^{Note 1} | 1.8 | 1.9 | 2.0 | V |
| Power supply rise time | t _{PH} | V _{DD} : 0 V → 1.8 V | 0.01 | | 100 | ms |
| Release signal set time | t _{SREL} | STOP cancelled by $\overline{\text{RESET}}$ | 10 | | | μs |
| Oscillation stabilization wait time ^{Note 2} | t _{WAIT} | Cancelled by $\overline{\text{RESET}}$ | | Note 3 | | s |
| | | Cancelled by interrupt request | | Note 4 | | s |

- Notes**
1. The response time is the time until the output is inverted following detection of voltage by POC, or the time until operation stabilizes after the shift from the operation stopped state to the operating state.
 2. The oscillation stabilization time is the amount of time the CPU operation is stopped in order to avoid unstable operation at the start of oscillation. Program operation does not start until both the oscillation stabilization time and the time until oscillation starts have elapsed.
 3. 2¹⁵/f_x or 2¹⁷/f_x can be selected using the mask option (refer to **9. MASK OPTION**).
 4. 2¹²/f_x, 2¹⁵/f_x, or 2¹⁷/f_x can be selected using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS) (refer to **7.2 Standby Function Control Register**).

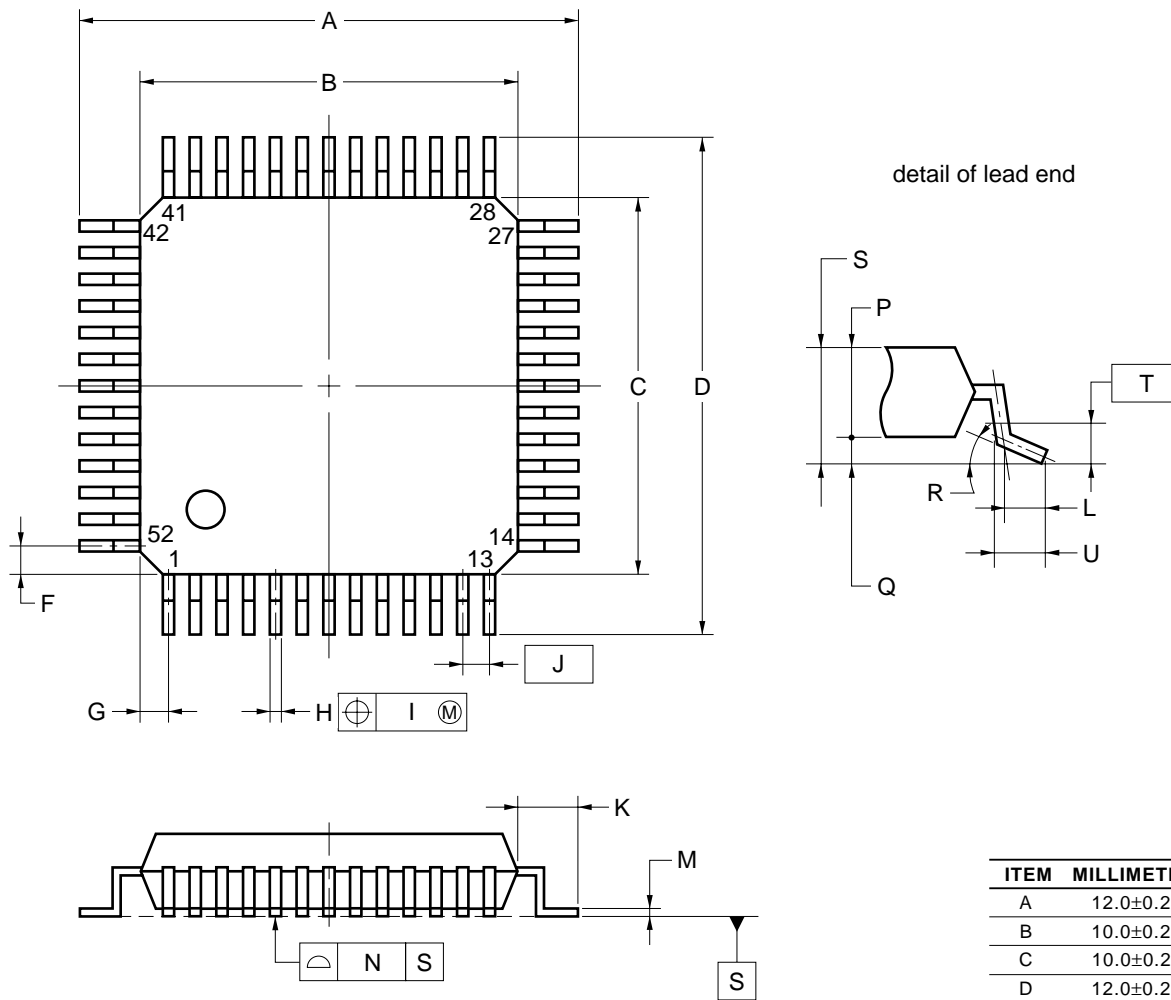
Remark fx: Main system clock oscillation frequency

Data Retention Timing



12. PACKAGE DRAWING

52-PIN PLASTIC LQFP (10x10)



| ITEM | MILLIMETERS |
|------|--|
| A | 12.0±0.2 |
| B | 10.0±0.2 |
| C | 10.0±0.2 |
| D | 12.0±0.2 |
| F | 1.1 |
| G | 1.1 |
| H | 0.32±0.06 |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5 |
| M | 0.17 ^{+0.03} _{-0.05} |
| N | 0.10 |
| P | 1.4 |
| Q | 0.1±0.05 |
| R | 3° ^{+4°} _{-3°} |
| S | 1.5±0.1 |
| T | 0.25 |
| U | 0.6±0.15 |

S52GB-65-8ET-1

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789322, 789324, 789326, and 789327.

Language Processing Software

| | |
|--------------------------------------|--|
| RA78K0S ^{Notes 1, 2, 3} | Assembler package common to 78K/0S Series |
| CC78K0S ^{Notes 1, 2, 3} | C compiler package common to 78K/0S Series |
| DF789328 ^{Notes 1, 2, 3, 5} | Device file for μPD789327 Subseries |
| CC78K/0S-L ^{Notes 1, 2, 3} | C compiler library source file common to 78K/0S Series |

Flash Memory Writing Tools

| | |
|--|--|
| Flashpro III (Part number: FL-PR3 ^{Note 4} , PG-FP3) | Dedicated flash memory programmer |
| FA-52GB ^{Notes 4, 5} | Adapter for writing to flash memory designed for 52-pin plastic LQFP (GB-8ET type) |

Debugging Tools

| | |
|---|---|
| IE-78K0S-NS In-circuit emulator | In-circuit emulator to debug hardware or software when application systems using the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine. |
| IE-70000-MC-PS-B AC adapter | AC adapter to supply power from a 100- to 240-V AC outlet. |
| IE-70000-98-IF-C Interface adapter | Interface adapter required when using a PC-9800 Series computer (except notebook type) as the host machine for the IE-78K0S-NS (C bus supported). |
| IE-70000-CD-IF-A PC card interface | PC card and interface cable required when a notebook PC is used as the host machine for the IE-78K0S-NS (PCMCIA socket supported). |
| IE-70000-PC-IF-C Interface adapter | Interface adapter required when using an IBM PC/AT™ or compatible as the host machine for the IE-78K0S-NS (ISA bus supported). |
| IE-70000-PCI-IF Interface adapter | Interface adapter required when using a PC incorporating a PCI bus as the host machine for the IE-78K0S-NS. |
| IE-789328-NS-EM1 ^{Note 5} Emulation board | Emulation board to emulate the peripheral hardware specific to the device. The IE-789328-NS-EM1 is used in combination with the in-circuit emulator. |
| NP-52GB ^{Notes 4, 5} | Board to connect an in-circuit emulator to the target system. This board is dedicated for a 52-pin plastic LQFP (GB-8ET type). |
| SM78K0S ^{Notes 1, 2} | System simulator common to 78K/0S Series |
| ID78K0S-NS ^{Notes 1, 2} | Integrated debugger common to 78K/0S Series |
| DF789328 ^{Notes 1, 2, 5} | Device file for μPD789327 Subseries |

- Notes**
1. Based on the PC-9800 series (Japanese Windows™)
 2. Based on IBM PC/AT or compatibles (Japanese/English Windows)
 3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)
 4. Manufactured by Naito Densai Machida Mfg. Co, Ltd. (+81-44-822-3813).
 5. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789328 device file.

Real-Time OS

| | |
|-------------------------------|----------------------|
| MX78K0S ^{Notes 1, 2} | OS for 78K/0S Series |
|-------------------------------|----------------------|

- Notes**
1. Based on the PC-9800 series (Japanese Windows)
 2. Based on IBM PC/AT or compatibles (Japanese/English Windows)

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

| Document Name | Document No. | |
|---|----------------|----------------|
| | Japanese | English |
| μPD789322, 789324, 789326, 789327 Preliminary Product Information | U14673J | This document |
| μPD78F9328 Preliminary Product Information | U14411J | U14411E |
| μPD789327, 789467 Subseries User's Manual | To be prepared | To be prepared |
| 78K/0S Series User's Manual Instructions | U11047J | U11047E |

Documents Related to Development Tools (User's Manual)

| Document Name | | Document No. | |
|--|--|----------------|----------------|
| | | Japanese | English |
| RA78K0S Assembler Package | Operation | U11622J | U11622E |
| | Assembly Language | U11599J | U11599E |
| | Structured Assembly Language | U11623J | U11623E |
| CC78K0S C Compiler | Operation | U11816J | U11816E |
| | Language | U11817J | U11817E |
| SM78K0S System Simulator Windows Based | Reference | U11489J | U11489E |
| SM78K Series System Simulator | External Part User Open Interface Specifications | U10092J | U10092E |
| ID78K0S-NS Integrated Debugger Windows Based | Reference | U12901J | U12901E |
| IE-78K0S-NS In-circuit Emulator | | U13549J | U13549E |
| IE-789328-NS-EM1 Emulation Board | | To be prepared | To be prepared |

Documents Related to Embedded Software (User's Manual)

| Document Name | | Document No. | |
|--------------------------|-------------|--------------|---------|
| | | Japanese | English |
| 78K/0S Series OS MX78K0S | Fundamental | U12938J | U12938E |

Other Documents

| Document Name | Document No. | |
|--|--------------|----------|
| | English | Japanese |
| SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM) | X13769X | |
| Semiconductor Device Mounting Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892J | C11892E |
| Guide to Microcontroller-Related Products by Third Parties | U11416J | - |

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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